DC–40 GHz GaAs High–Gain MMIC Amplifier

MMA085AA

Product Overview

The MMA085AA is a DC-40 GHz Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) Pseudomorphic High–Electron Mobility Transistor (pHEMT) distributed amplifier. It is ideal for test instrumentation, A&D, and space applications. The amplifier provides 16 dB of gain, 20 dBm of P1dB, and -45 dBc of IM3 at 5 dBm per tone with a nominal bias condition of 200 mA from a 7V supply. Noise Figure (NF) is typically 3.5 dB. The amplifier features compact die size with RF I/O's that are internally matched to 50Ω. The MMA085AA can receive up to 29 dBm (CW) of RF input power.

Key Features

- Frequency range: DC to 40 GHz
- Gain: 16 dB
- Positive gain slope
- High IM3: –45 dBc (at 5 dBm per tone)
- Output level detector
- Die input power handling: up to 29dBm (CW)
- Supply voltage: 5V – 9V. Typical voltage: 7V at 200 mA
- ESD Protection on RF and DC ports
- 50 Ohm Matched Input/Output
- Die: 2.05mm × 1. 43 mm × 0.1 mm

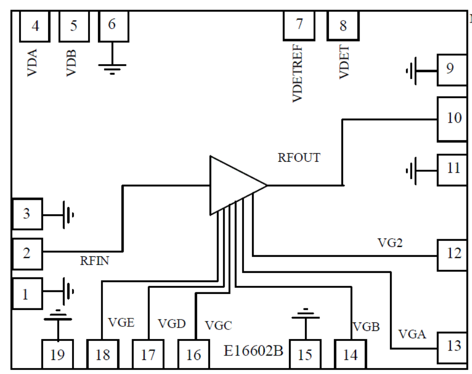
Applications

- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military, A&D, space, SATCOM
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter–wave communications systems

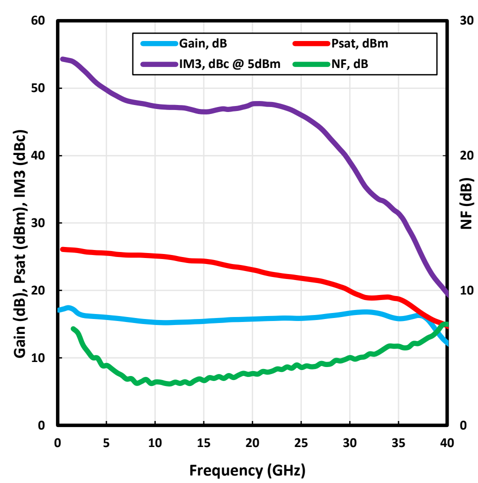
Performance Overview

Parameter	Typ.	Units
Operationalf requency range	DC–40	GHz
Gain	16	dB
Noise figure	3.5	dB
P1dB	20	dBm
IM3 at 5 dBm per Tone	–45	dBc

Functional Block Diagram



Performance Curves



Export Classification: 3A001.b.2.d

Table of Contents

1. Electrical Specifications

1.1 Typical Electrical Performance

The following table shows the typical electrical performance of the MMA085AA device at 25 °C, V_{DD} = 7V, and I_{DD} = 200 mA, unless otherwise specified.

Table 1-1. Typical Electrical Performance

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		0		40	GHz
Gain	DC – 10 GHz	15	16	18	dB
	10 GHz – 30 GHz	15	16	17	
	30 GHz – 40 GHz	12	16	17	
Gain flatness	DC – 10 GHz		±1		dB
	10 GHz – 30 GHz		±0.5		
	30 GHz – 40 GHz		±1.5		
Noise figure	DC – 10 GHz		5	7	dB
	10 GHz – 30 GHz		3.5	5	
	30 GHz – 40 GHz		6	7.5	
Input return loss	DC – 10 GHz	14	17		dB
	10 GHz – 30 GHz	9	12		
	30 GHz – 40 GHz	8	9		
Output return loss	DC – 10 GHz	13	14		dB
	10 GHz – 30 GHz	10	12		
	30 GHz – 40 GHz	8	9		
P1dB	DC – 10 GHz	21	23		dBm
	10 GHz – 30 GHz	18	20		
	30 GHz – 40 GHz	12	16		
P_{sat}	DC – 10 GHz	23	25		dBm
	10 GHz – 30 GHz	19	22		
	30 GHz – 40 GHz	14	18		
IM3, at 5 dBm per tone	DC – 10 GHz		– 48		dBc
	10 GHz – 30 GHz		– 45		
	30 GHz – 40 GHz		– 30		
Input power survivability (CW)	6 GHz – 12 GHz			29	dBm
V_{DD} (drain voltage supply)			7		V
I_{DD} (drain current)			200		mA

1.2 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA085AA device at 25 °C, unless otherwise specified. Exceeding any of the maximum ratings could cause damage and/or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameters	Rating
Drain bias voltage (V_{DD})	12V
Drain bias current (I_{DD})	300 mA
Gate bias voltage (V_G)	–2V to 0.5V
RF input power (Pin)	+29 dBm (CW)
Channel temperature	175 °C
Thermal resistance	19 °C/W
Storage temperature	–65 °C to 150 °C
Operating temperature	–55 °C to 85 °C

ESD Sensitive Device

1.3 Typical Performance Curves

1.3.1 Typical Performances vs. Temperature

The graphs shown in figures 1–1 through 1–31 represent the Typical Performance versus Temperature curves of the MMA085AA device under specific bias conditions. All measurements were taken using the test circuit shown in Figure 3–2.

Figure 1-1. Gain vs. Temperature at 6V/150 mA

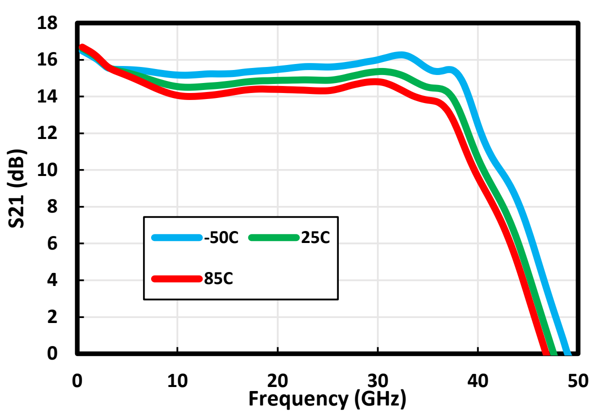


Figure 1-2. Gain vs. Temperature at 7V/200 mA

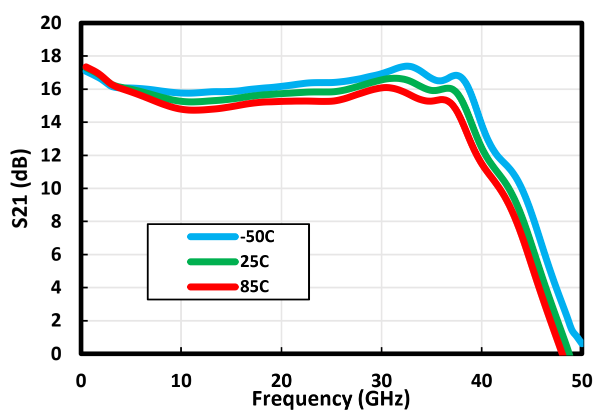


Figure 1-3. Gain vs. Temperature at 8V/250 mA

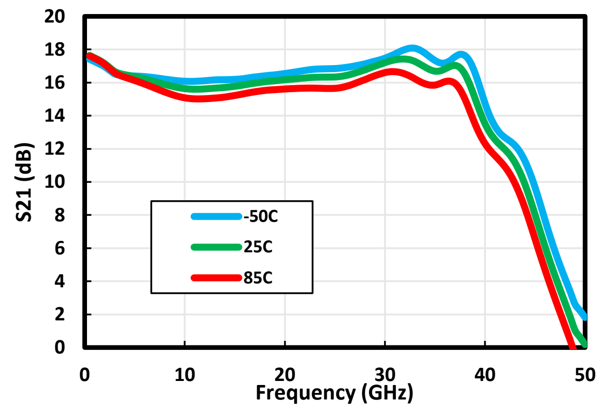


Figure 1-4. S11 vs. Temperature at 6V/150mA

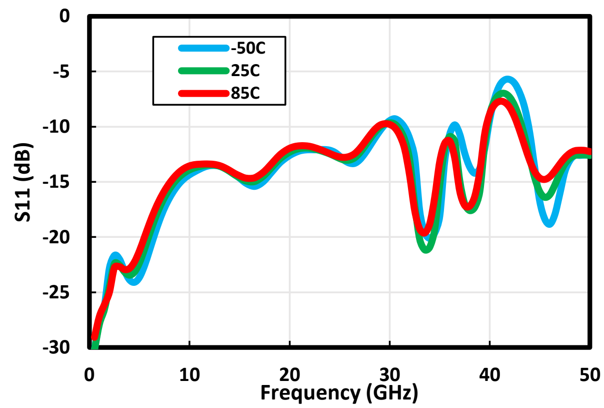


Figure 1-5. S11 vs. Temperature at 7V/200 mA

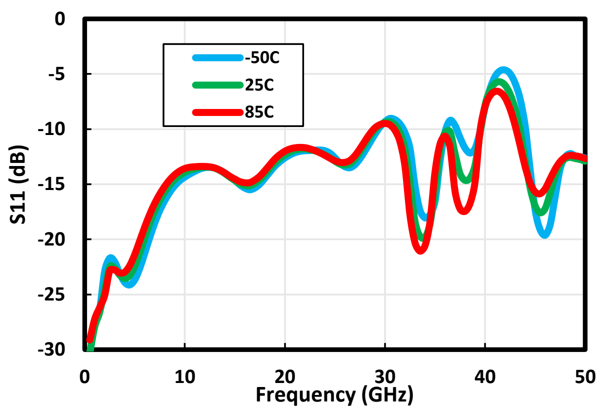


Figure 1-6. S11 vs. Temperature at 8V/250 mA

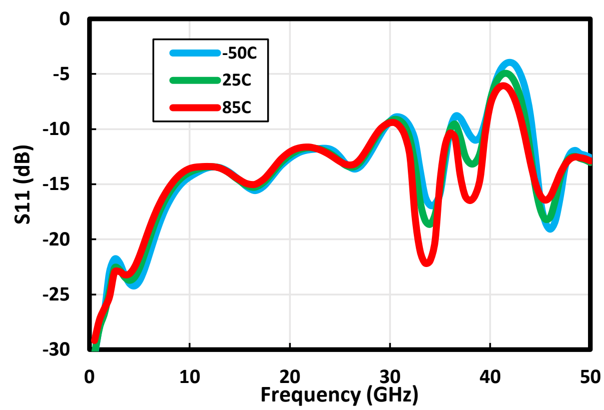


Figure 1-7. S22 vs. Temperature at 6V/150 mA

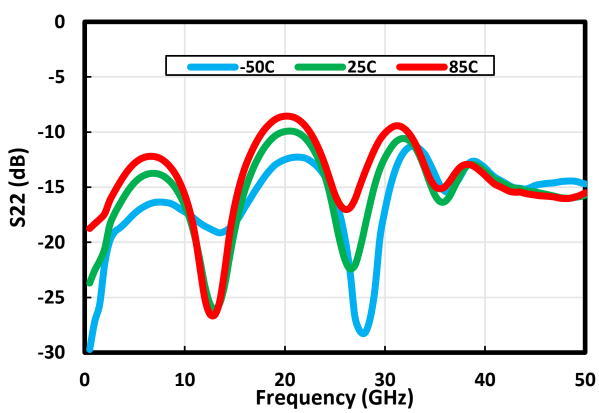


Figure 1-8. S22 vs. Temperature at 7V/200 mA

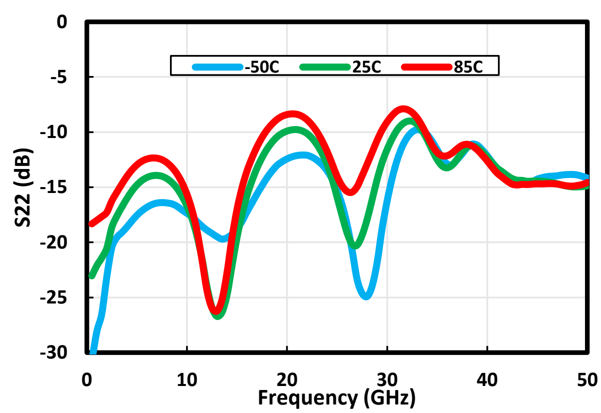


Figure 1-9. S22 vs. Temperature at 8V/250 mA

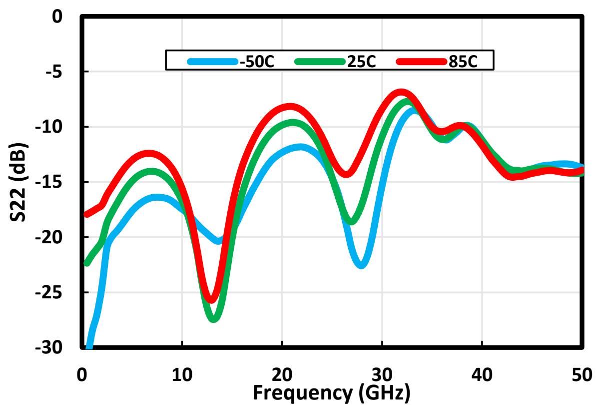


Figure 1-10. S12 vs. Temperature at 6V/150 mA

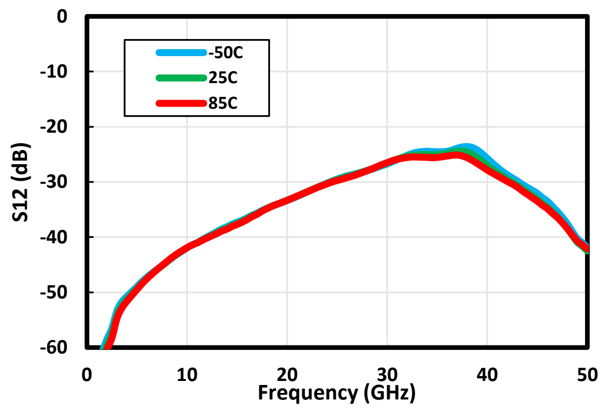


Figure 1-11. S12 vs. Temperature at 7V/200 mA

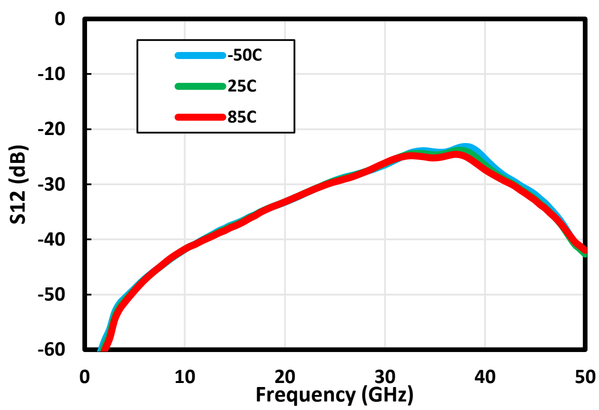


Figure 1-12. S12 vs. Temperature at 8V/250 mA

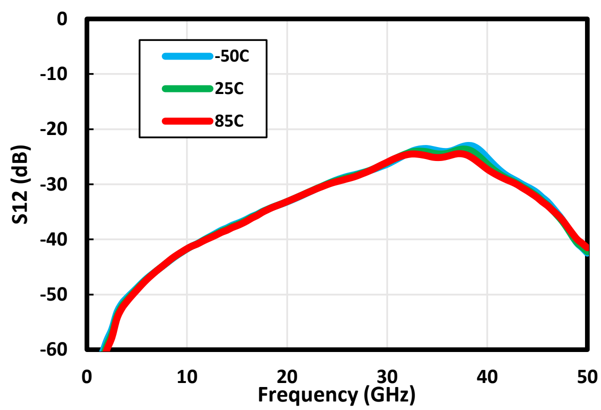


Figure 1-13. NF vs. Temperature at 6V/150 mA

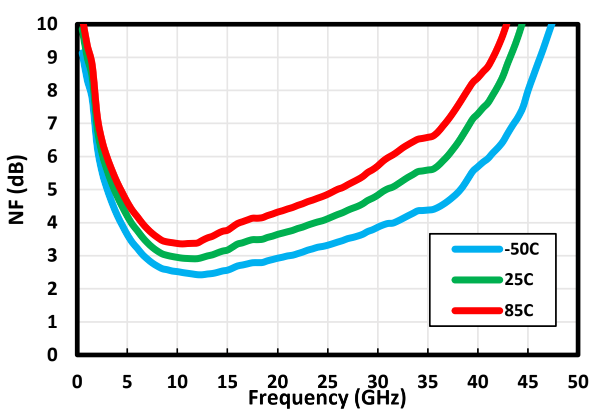


Figure 1-14. NF vs. Temperature at 7V/200 mA

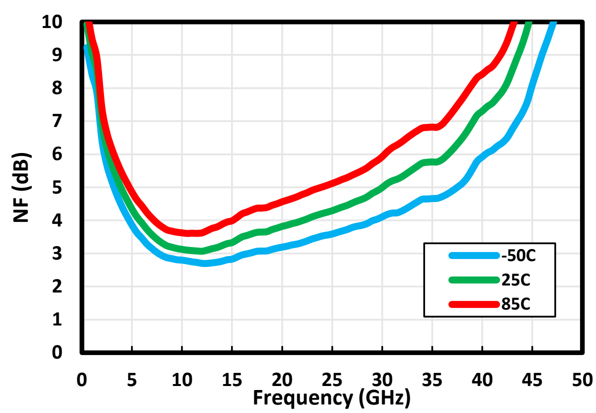


Figure 1-15. NF vs. Temperature at 8V/250 mA

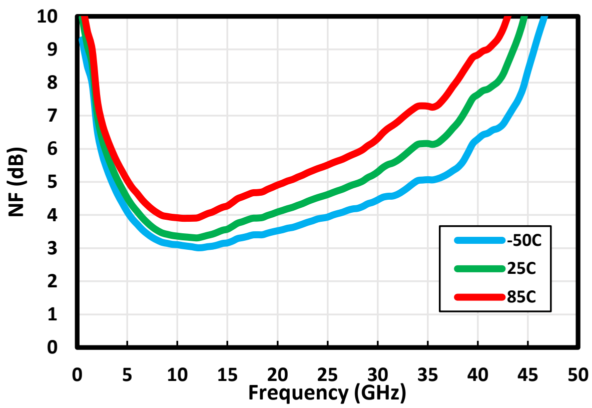


Figure 1-16. P1dB vs. Temperature at 5V/120 mA

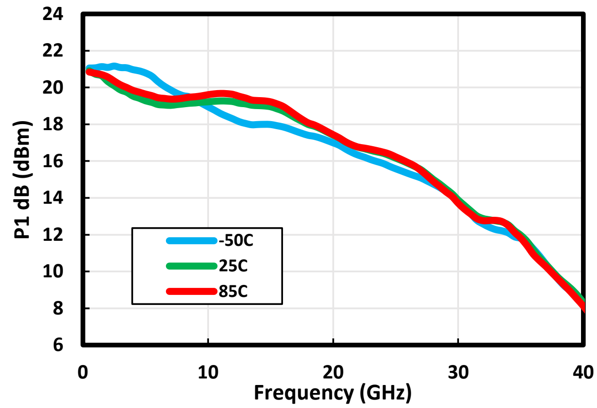


Figure 1-17. P1dB vs. Temperature at 6V/150 mA

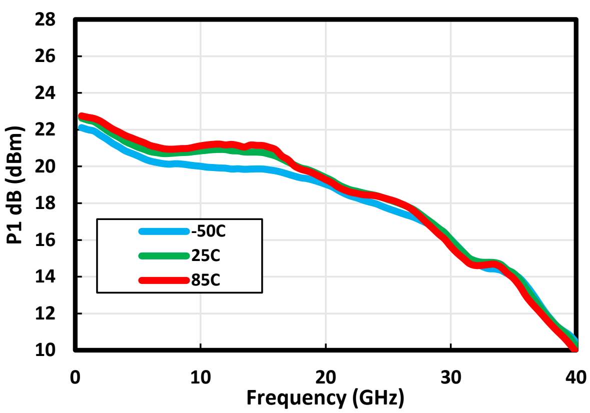


Figure 1-18. P1dB vs. Temperature at 7V/200 mA

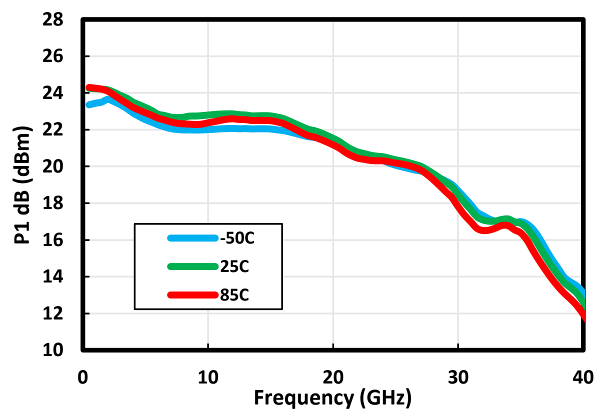


Figure 1-19. P1dB vs. Temperature at 8V/250 mA

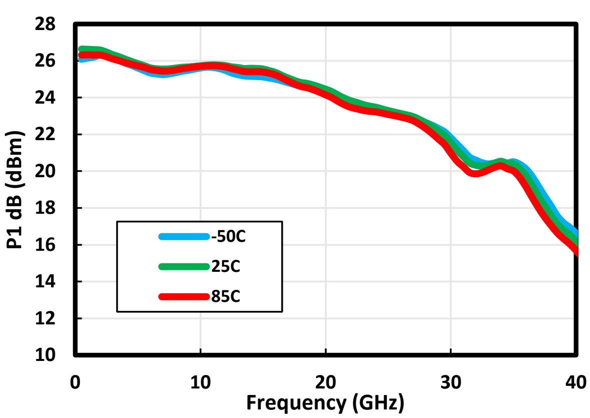


Figure 1-20. Psat vs. Temperature at 5V/120 mA

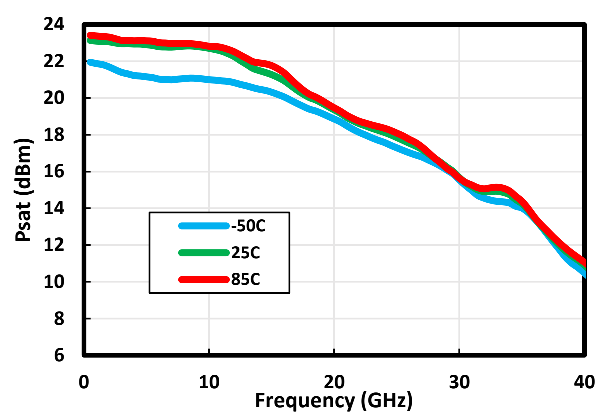


Figure 1-21. Psat vs. Temperature at 6V/150 mA

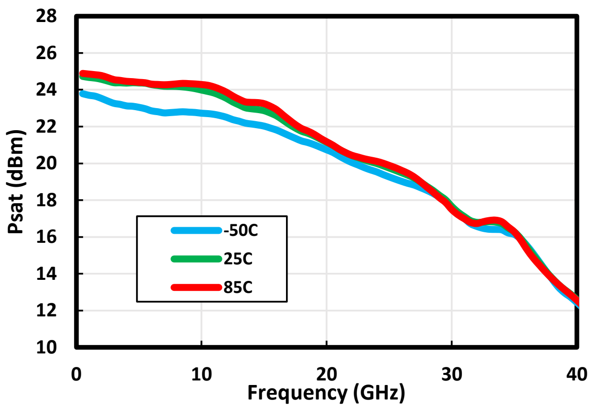


Figure 1-22. Psat vs. Temperature at 7V/200 mA

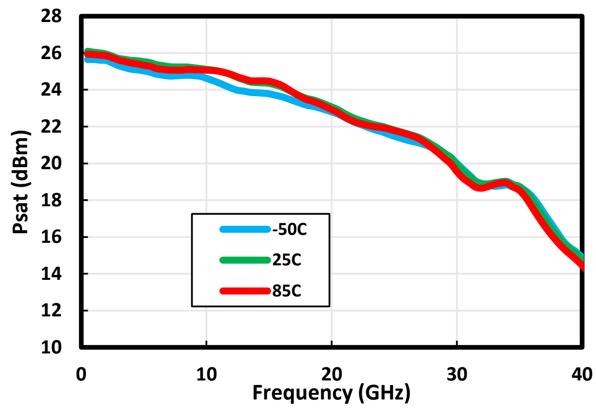


Figure 1-23. Psat vs. Temperature at 8V/250 mA

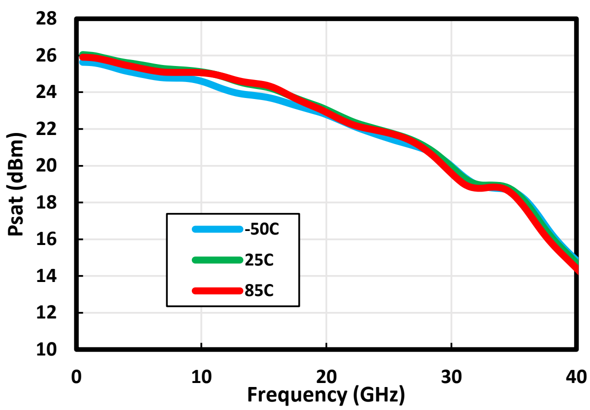


Figure 1-24. IM2 (low) vs. Temperature at 5V/120 mA[1]

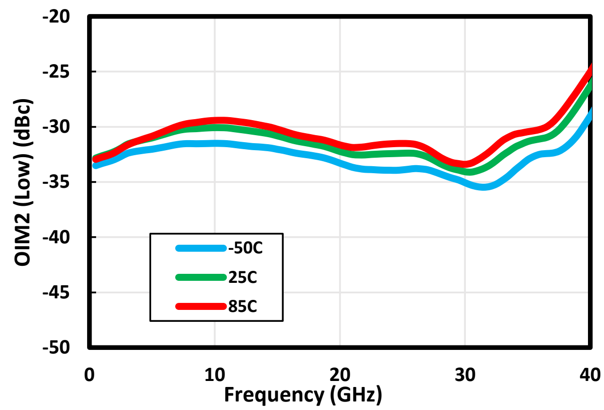


Figure 1-25. IM2 (low) vs. Temperature at 6V/150 mA[1]

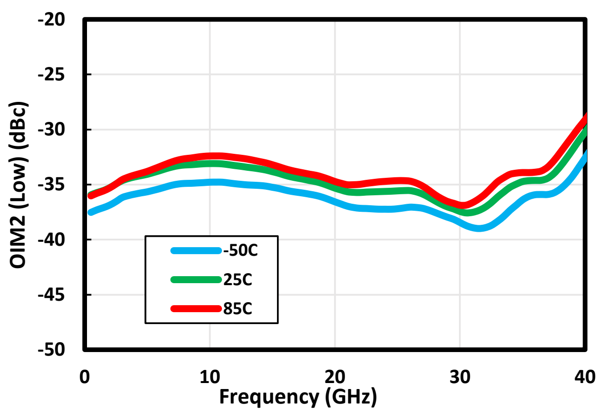


Figure 1-26. IM2 (low) vs. Temperature at 7V/200 mA[1]

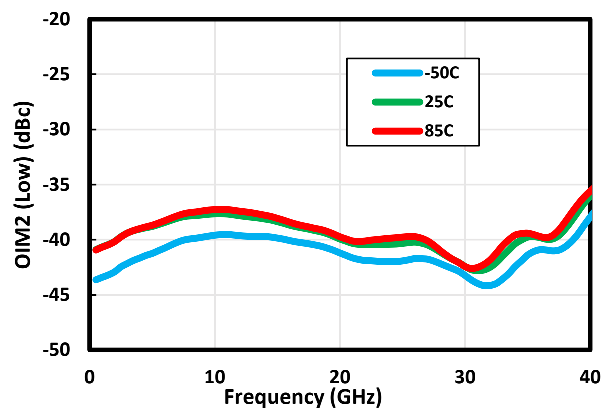


Figure 1-27. IM2 (low) vs. Temperature at 8V/250 mA[1]

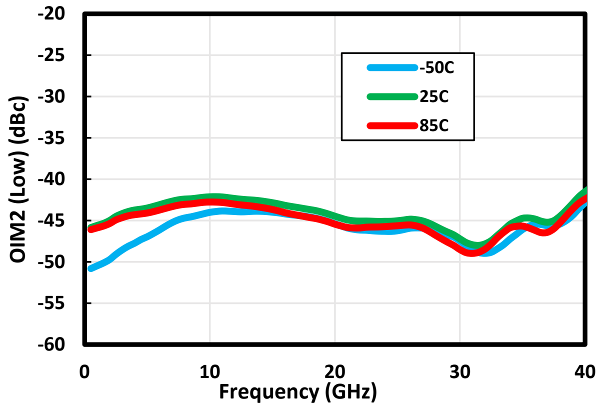


Figure 1-28. IM3 vs. Temperature at 5V/120 mA[1]

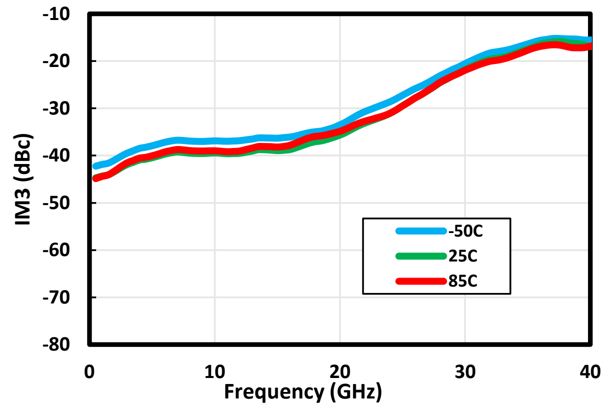


Figure 1-29. IM3 vs. Temperature at 6V/150 mA[1]

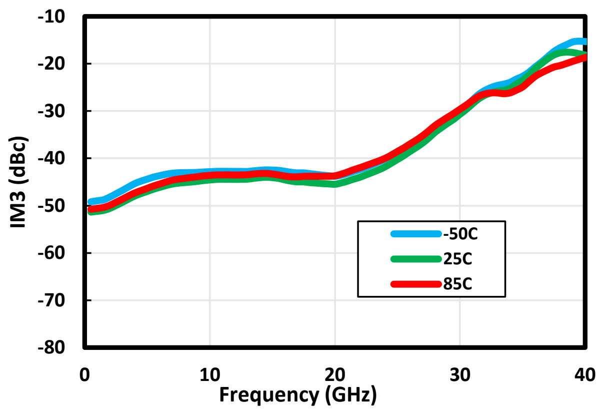


Figure 1-30. IM3 vs. Temperature at 7V/200 mA[1]

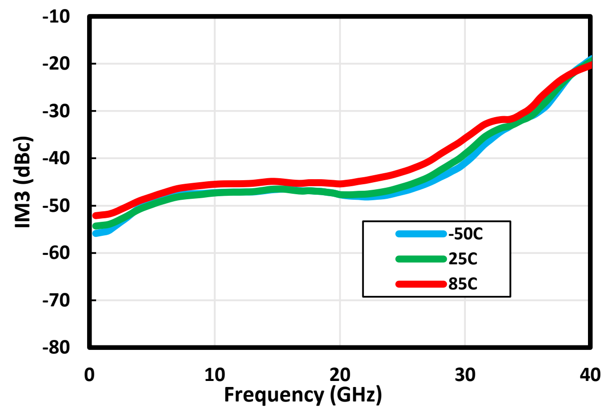
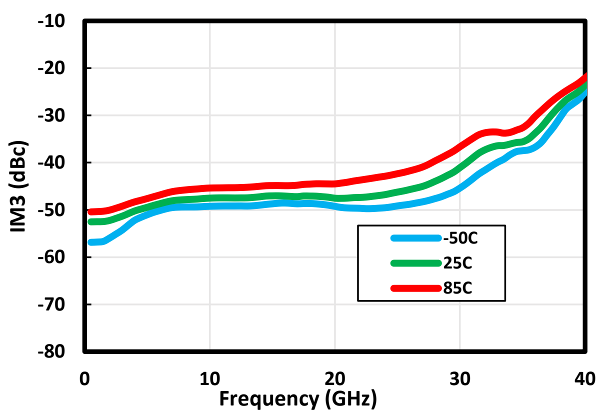


Figure 1-31. IM3 vs. Temperature at 8V/250 mA[1]



Note:

1. At 5 dBm per tone.

1.3.2 Typical Performances vs. Bias

The graphs shown in figures 1–32 through 1–44 represent the Typical Performance versus Bias curves of the MMA085AA under constant temperature of 25 °C. All measurements were taken using the test circuit shown in Figure 3–2.

Figure 1-32. Gain vs. V_{DD} at 120 mA

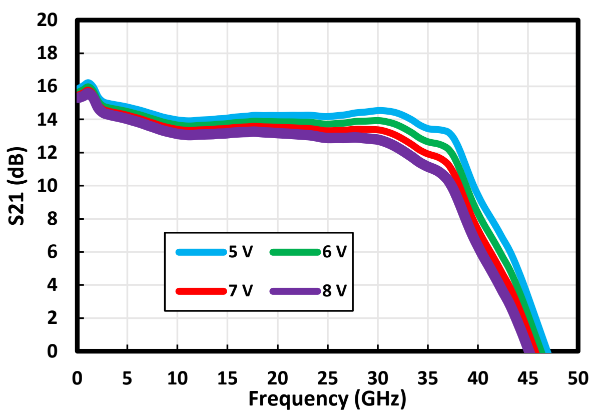


Figure 1-33. Gain vs. V_{DD} at 150 mA

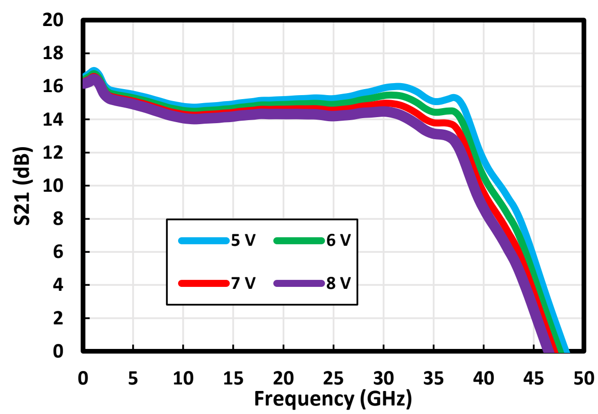


Figure 1-34. Gain vs. V_{DD} at 200 mA

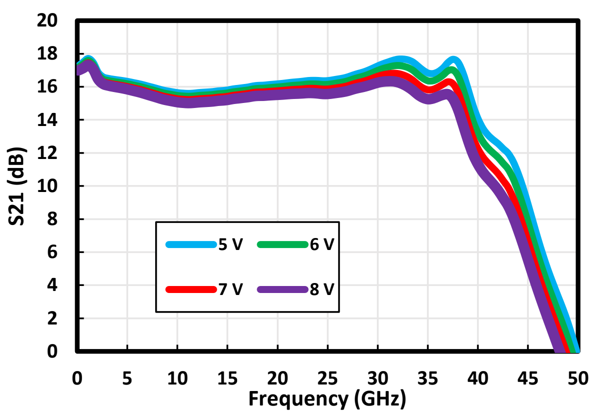


Figure 1-35. Gain vs. V_{DD} at 250 mA

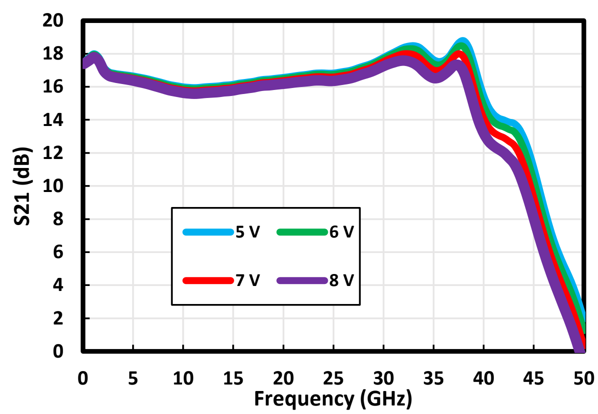


Figure 1-36. NF vs. V_{DD} at 120 mA

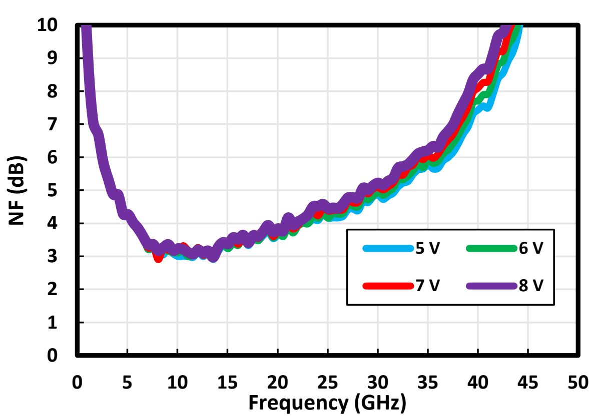


Figure 1-37. NF vs. V_{DD} at 150 mA

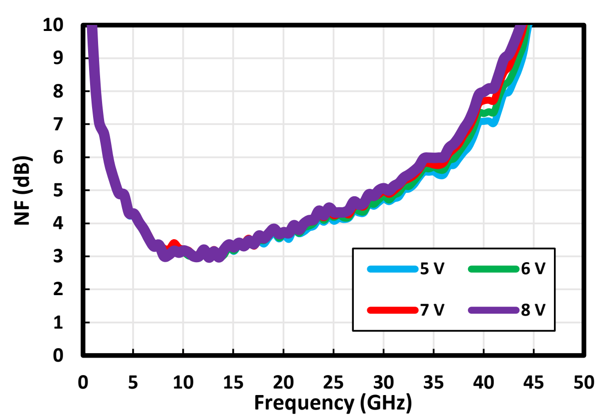


Figure 1-38. NF vs. V_{DD} at 200 mA

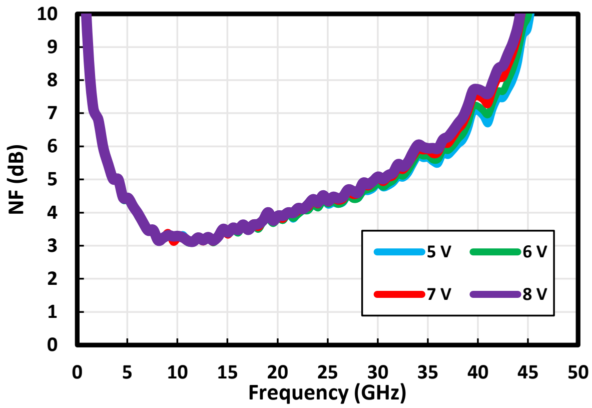


Figure 1-39. NF vs. V_{DD} at 250 mA

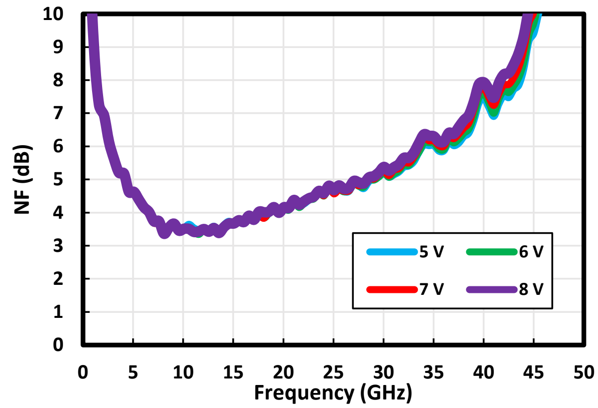


Figure 1-40. P1dB Bias

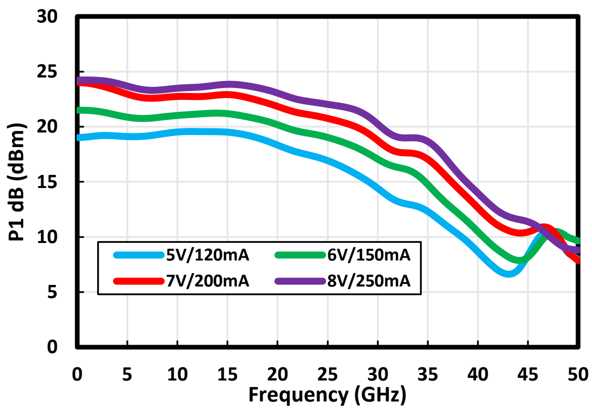


Figure 1-41. P_{sat} vs. Bias

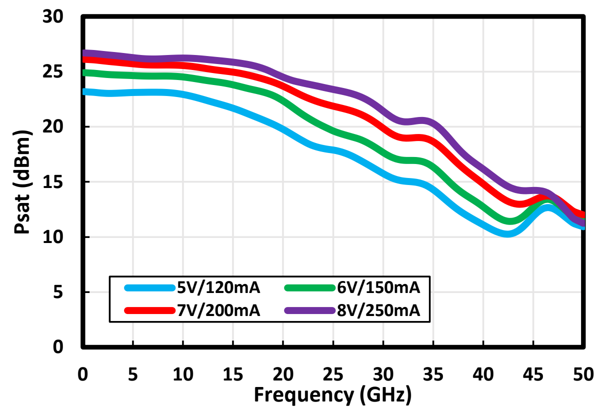


Figure 1-42. OIP3 vs. Bias

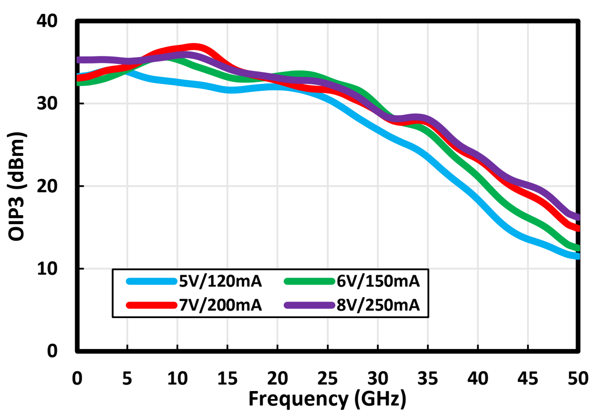


Figure 1-43. IM3 vs. Bias at 10 dBm per tone

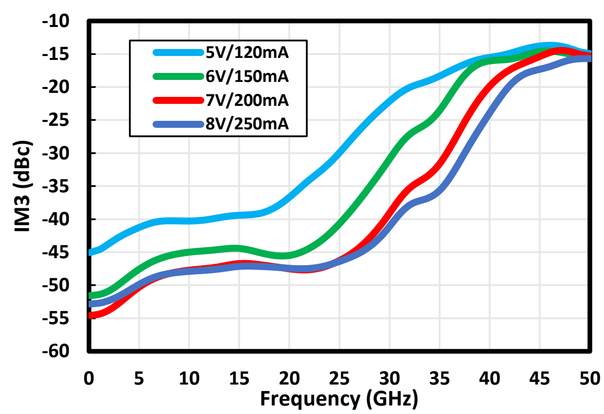
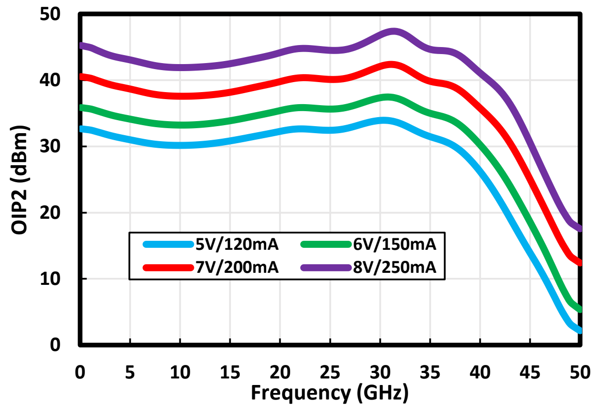


Figure 1-44. OIP2 (Low at Δ = 10 MHz) vs. Bias



1.3.3 Typical Performances vs. Output Power

The graphs shown in figures 1–45 through 1–56 represent the Typical Performance versus Output power curves of the MMA085AA under constant temperature of 25 °C. All measurements were taken using the test circuit shown in Figure 3–2.

Figure 1-45. IM2 vs. Power at 5V/120 mA

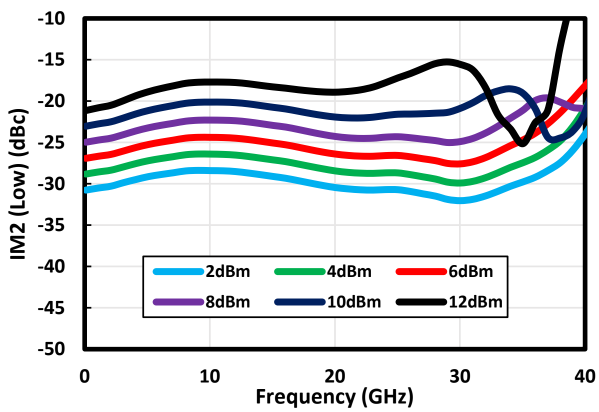


Figure 1-46. IM2 vs. Power at 6V/150 mA

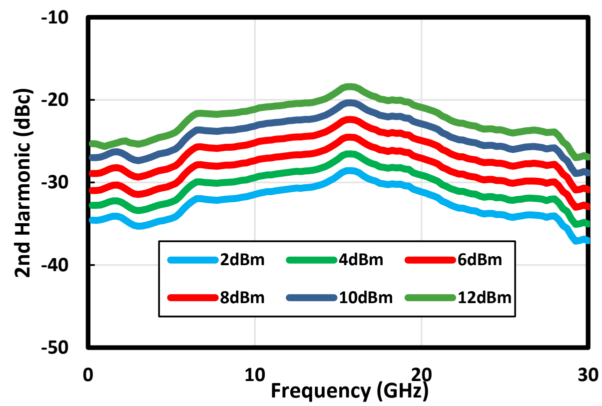


Figure 1-47. IM2 vs. Power at 7V/200 mA

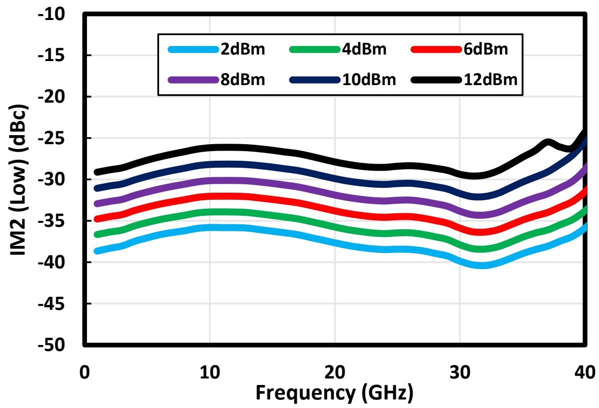


Figure 1-48. IM2 vs. Power at 8V/250 mA

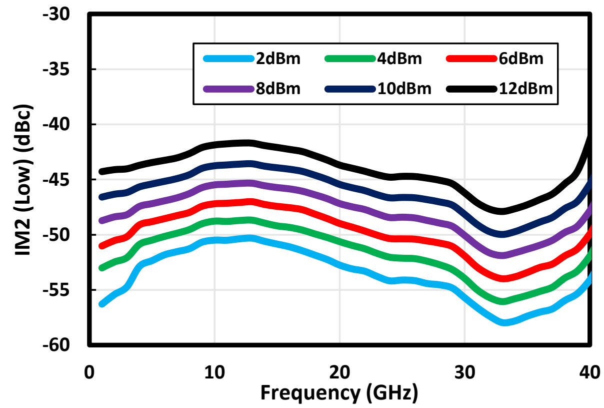


Figure 1-49. IM3 vs. Power at 5V/120 mA

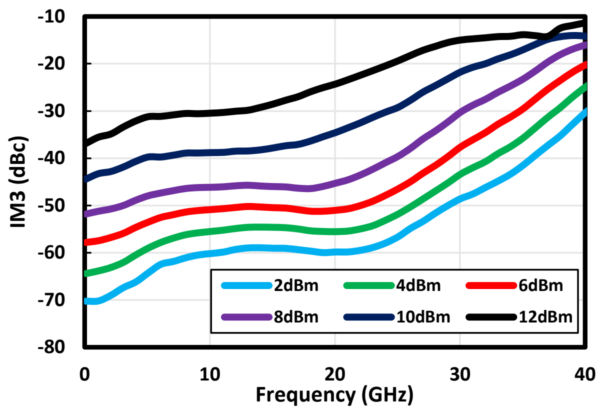


Figure 1-50. IM3 vs. Power at 6V/150 mA

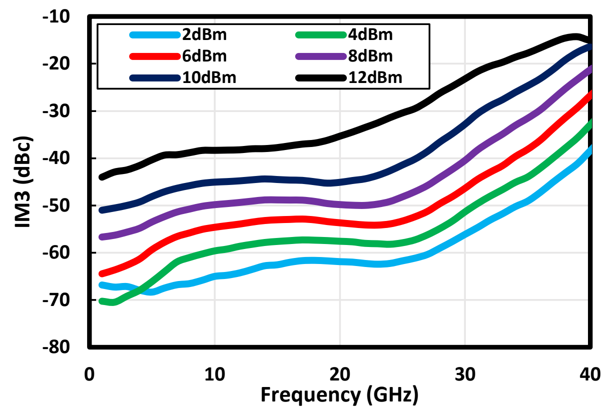


Figure 1-51. IM3 vs. Power at 7V/200 mA

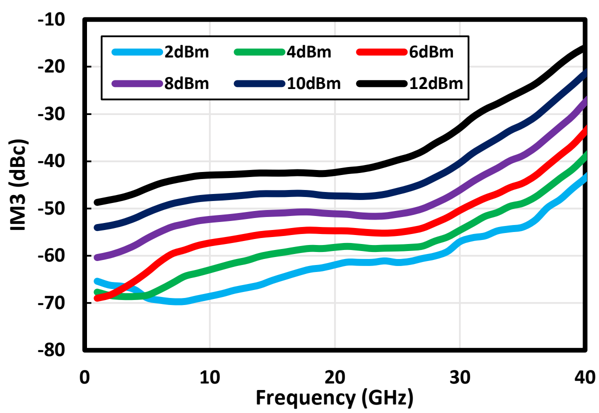


Figure 1-52. IM3 vs. Power at 8V/250 mA

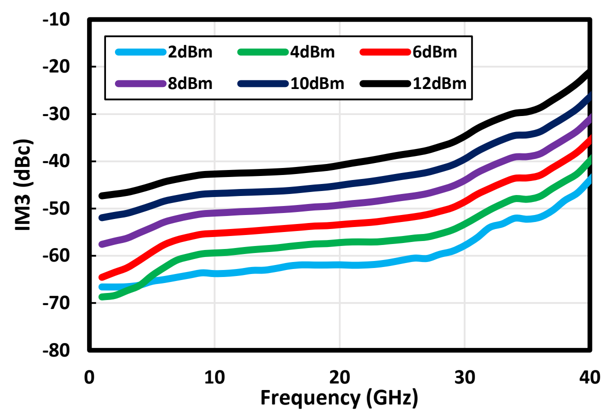


Figure 1-53. 2nd Harmonic vs. Power at 5V/120 mA

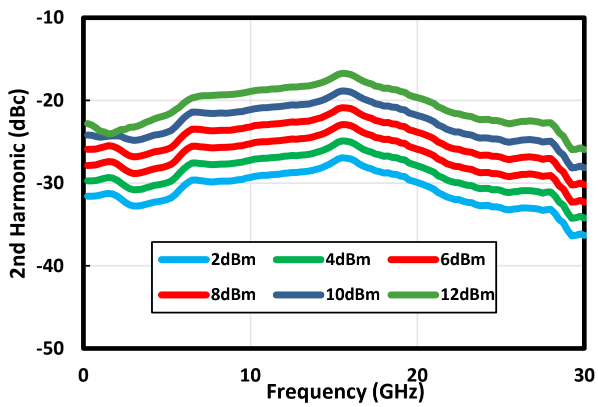


Figure 1-54. 2nd Harmonic vs. Power at 6V/150 mA

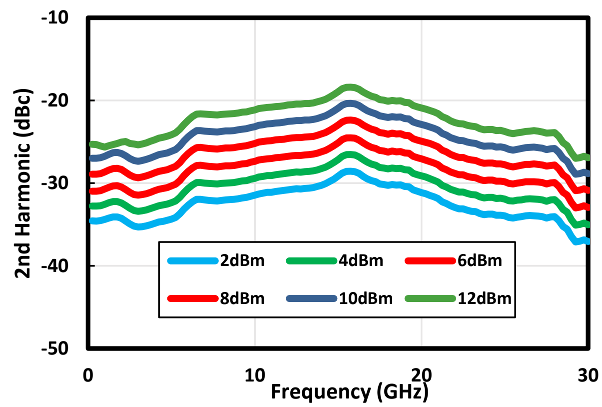


Figure 1-55. 2nd Harmonic vs. Power at 7V/200 mA

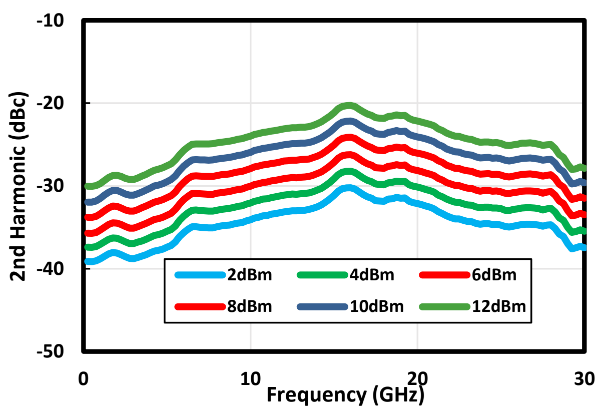
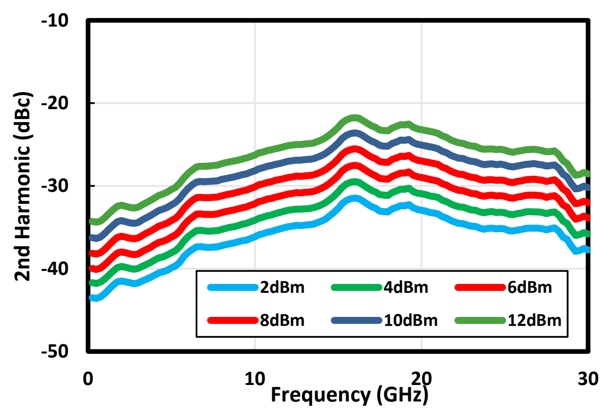


Figure 1-56. 2nd Harmonic vs. Power at 8V/250 mA

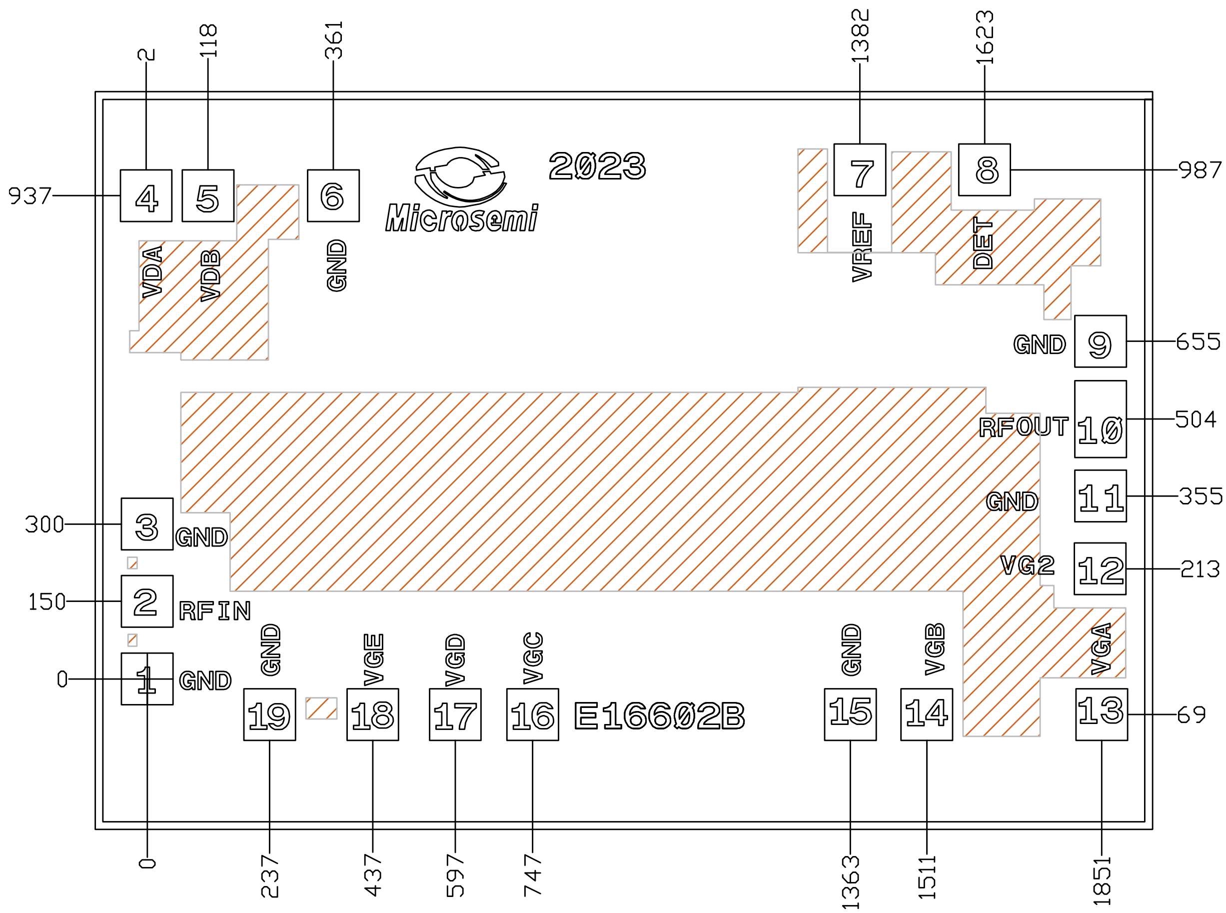


2. Die Specifications

Figure 2–1 shows the chip outline of the MMA085AA device. Pad offsets are shown in microns relative to the zero datum location centered on pad 1.

Nominal die dimensions are 2.05 mm × 1.43 mm × 0.1 mm. The minimum bond pad size is 0.1 mm × 0.1 mm. The bond pad surface and the backside metal have 3 µm thick gold. The die thickness is 0.1 mm. The backside is the DC/RF ground. The airbridge keep-out polygon region is shown inside.

Figure 2-1. Die Outline Drawing (µm)



The following table shows the PAD descriptions for the MMA085AA device.

Table 2-1. PAD Description

PAD Number	Description	PAD Size (µm)
1	GND	95 × 95
2	RFIN	95 × 95
3	GND	95 × 95
4	VDA drain termination bypass	95 × 95
5	VDB drain termination bypass	95 × 95
6	GND	95 × 95
7	DC Det. Ref.	95 × 95
8	RF Det	95 × 95
9	GND	95 × 95
10	RFOUT	95 × 140
11	GND	95 × 95
12	VG2	95 × 95
13	VGA gate termination bypass	95 × 95
14	VGB gate termination bypass	95 × 95
15	GND	95 × 95
16	VGC gate termination bypass	95 × 95
17	VGD gate termination bypass	95 × 95
18	VGE gate termination bypass	95 × 95
19	GND	95 × 95

The following table shows the I/O description for the MMA085AA device.

Table 2-2. I/O Description

Pad Number	Pad Name	Pad Description
2	RF_{IN}	This pad RF/DC coupled to the FET gates and matched to 50Ω.
10	RF_{OUT}	This pad is RF/DC coupled to the FET drains and matched to 50Ω; this terminal used for V_{DD} bias
4, 5	V_{DDA}, V_{DDB}	V_{DDA} ,V_{DDB} low-frequency termination for drain ballast, DC coupled to the FET drains (this pads **ARE NOT** designed for V_{DD} bias)
7	V_{DREF}	Detector DC reference
8	V_{DET}	Detector output
12	V_{G2}	Access to gate 2 bias
13, 14	V_{GA}, V_{GB}	First gate low-frequency terminations DC Coupled to the gate 1 and used to set the die bias current
16, 17, 18	V_{GC}, V_{GD}, V_{GE}	Complementary low-frequency terminations for the gate 1, used to control low–frequency response slope
1, 3, 6, 9, 11, 15, 19	Ground	Ground connections used for die test purposes; DC/RF ground is using die backside metal

3. Application Circuit

The following diagram shows the application circuit schematic for the MMA085AA device.

Figure 3-1. Application Circuit Schematic

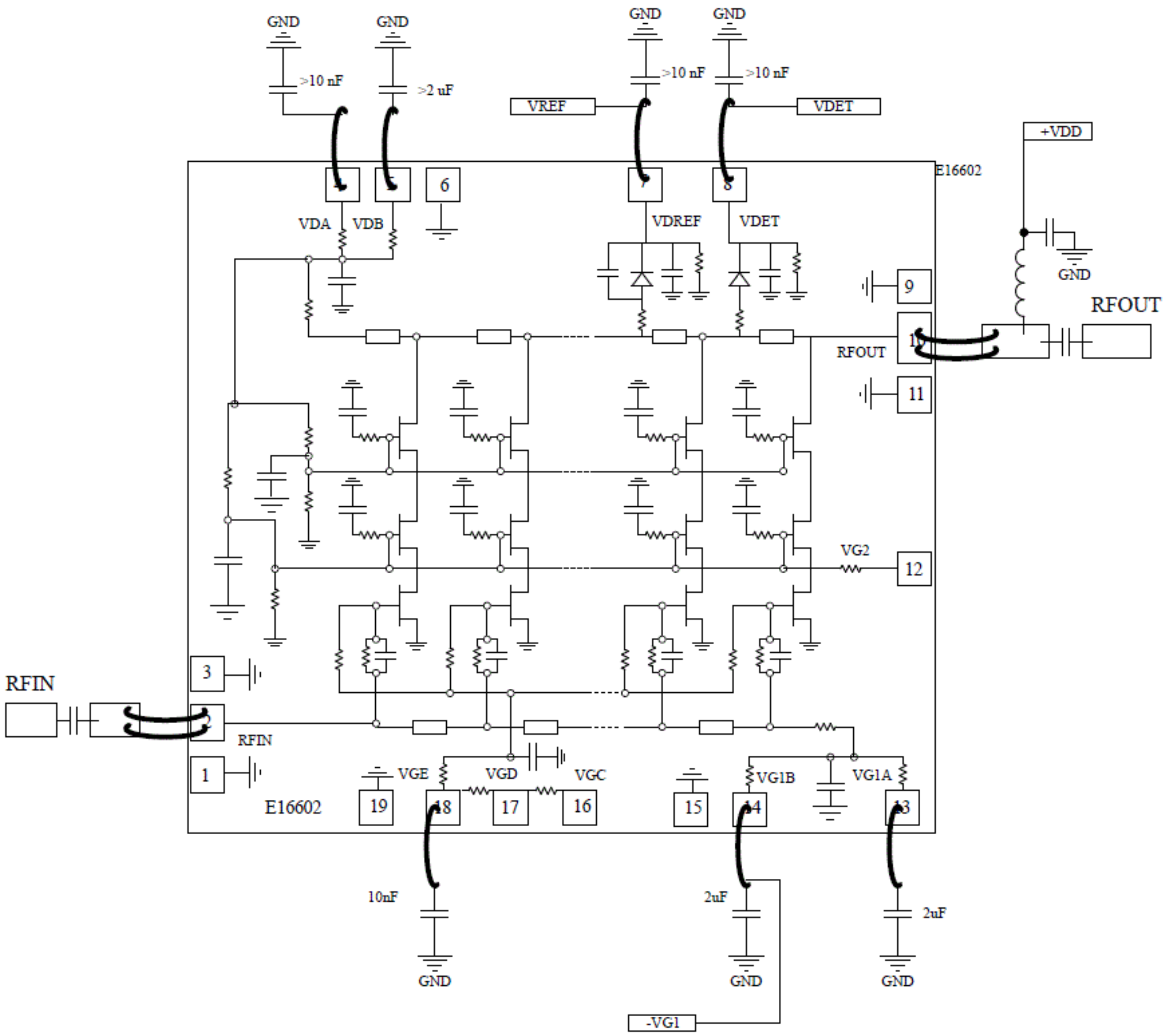
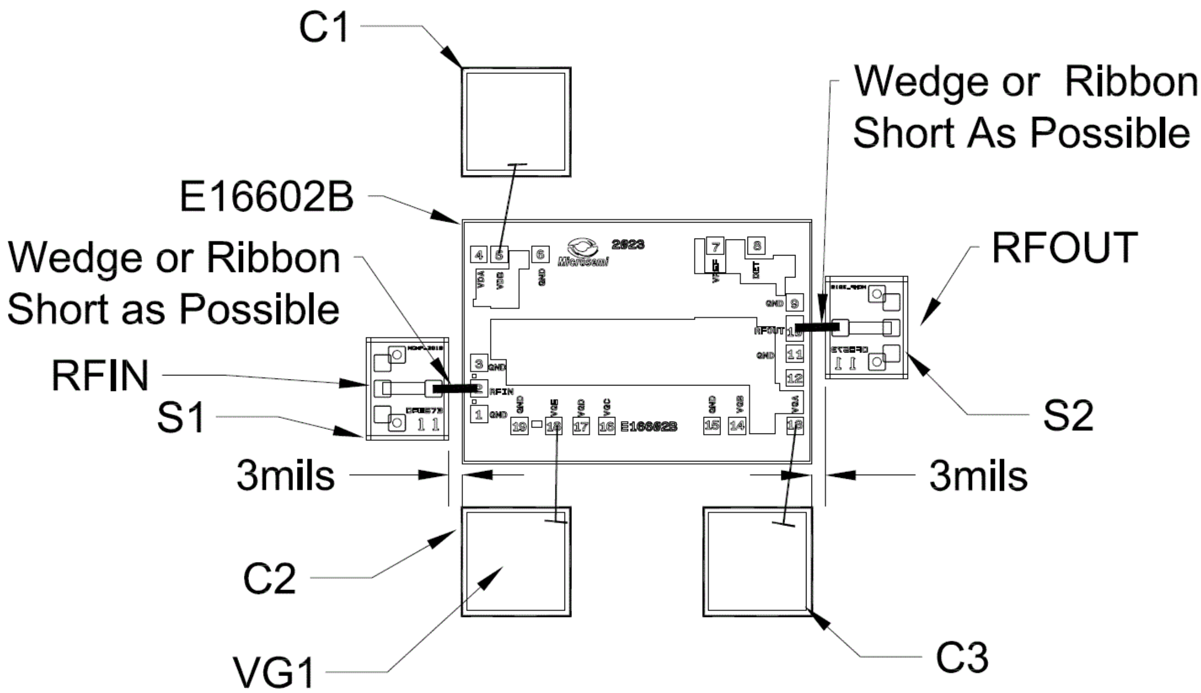


Figure 3-2. Die Test Circuit: Assembly Drawing



The following table shows the list of materials for the MMA085AA test circuit.

Table 3-1. List of Materials for Test Circuit

Reference	Part Number	Description
E16602B	MMA085AA	MMA085AA amplifier die
C1, C2, C3	160U02A102MT4W	Johnson dielectric, Cer. Cap 1 nF
S1, S2	E57311, E57312	Probe launchers

4. Ordering, Shipping, and Handling

4.1 Handling Recommendations

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Mircochip application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA085AA	Die

4.3 Packing Information

Standard Format
Gel Pack
50 Pieces per Pack

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	09/2024	Document created.

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