PECL, LVDS, CMOS Output Low Jitter SMD Crystal Oscillator

7.0 x 5.0 x 1.8mm

ABNM SERIES

RoHS/RoHS II Compliant

Moisture Sensitivity Level (MSL) – This product is Hermetically Sealed and not Moisture Sensitive - MSL = N/A: Not Applicable

FEATURES:

- Low Jitter <1ps phase jitter RMS
- PECL, LVDS, CMOS Output

APPLICATIONS:

- SONET, PCI Express, SERDES, Video
- Anywhere Low Jitter is required

STANDARD SPECIFICATIONS:

Common Key Electrical Specifications

Parameters		Minimum	Typical	Maximum	Units	Notes
Frequency Range:	CMOS	1.000		39.999	MHz	Fundamental
		40.000		156.999		3-Overtone
	LVDS	65.000		156.999		3-Overtone
	PECL	50.000		160.000		3-Overtone
Operating Temperature:		0		+70	°C	See options
Storage Temperature:		-55		+155	°C	
Overall Frequency Stability*:		-50		+50	ppm	See options
Supply Voltage (Vdd):	V_{dd} = 3.3V	2.97	3.3	3.63	V	Standard
	V_{dd} = 2.5V	2.25	2.5	2.75	V	Option 1
Tri-state function :		"1" (VIH≥0.7*Vdd) or Open: Oscillation "0" (VIH<0.3*Vdd) : Hi Z				CMOS, LVDS, PECL 1
		"0" (VIH<0.3*Vdd) or Open: Oscillation "1" (VIH≥0.7*Vdd) : Hi Z				PECL (Option P)
Aging:		-3.0		+3.0	ppm	@+25°C First year

* Inclusive of calibration @25°C, operating temperature range, input voltage variation, load variation, aging, shock, and vibration.
** Transition times are measured between 10% and 90% of Vdd with an output load of 15 pF.

Key Electrical Specifications for PECL

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{dd}):			50	65	mA	50.000~79.999 MHz
			50	65		80.000~124.999 MHz
			55	70		125.000~156.999 MHz
Output Voltage:	V_{OH}	Vdd-1.025		Vdd-0.880	V	Vdd=3.3V, 2.5V
	V_{OL}	Vdd-1.810		Vdd-1.620	V	
Symmetry:		45		55	%	
Start-up Time :			2	5	ms	50.000~79.999 MHz
			2	5		80.000~124.999 MHz
			2	5		125.000~156.999 MHz
Rise/Fall Time (Tr/Tf):			0.3	0.6	ns	1.000~15.999 MHz
			0.4	0.5		90.000~124.999 MHz
			0.4	0.5		125.000~156.999 MHz
Phase jitter RMS (12kHz to 20MHz):			0.5	1.5	ps	50.000~79.999 MHz
			0.5	1.0		80.000~124.999 MHz
			0.5	1.0		125.000~156.999 MHz

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ABRACON LLC
The Power of Linking Together

5101 Hidden Creek Lane Spicewood TX 78669
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RoHS/RoHS II Compliant

STANDARD SPECIFICATIONS:

(Continued)

Parameters		Minimum	Typical	Maximum	Units	Notes
Period jitter RMS			3.0	5.0	ps	50.000~79.999 MHz
			3.0	5.0		80.000~124.999 MHz
			3.0	5.0		125.000~156.999 MHz
Phase Noise (Typical value):	Offset	1kHz	10kHz	100kHz	dBc	
	66.660 MHz carrier	-128	-141	-145		
	100.000 MHz carrier	-130	-140	-141		
	125.000 MHz carrier	-130	-140	-141		
	156.250 MHz carrier	-127	-138	-140		

Key Electrical Specifications for LVDS

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{dd})			10	20	mA	65.000~79.999 MHz
			40	50		80.000~124.999 MHz
			45	55		125.000~156.999 MHz
Output Differential Voltage (V_{OD})		247	355	454	mV	
Vod Magnitude Change (ΔVod)		-50		50	mV	
Offset Voltage [RL=100Ω] (V_{Os})		1.125	1.200	1.375	mV	
Offset Magnitude Change [RL=100Ω] (ΔV_{Os})		0	3	25	mV	
Output Voltage:	V_{OH}		1.40	1.60	mV	
	V_{OL}	0.90	1.10		mV	
Power-off Leakage (Ioxd) [Vout=Vdd or GND, Vdd=0V]			±1.0	±10.0	uA	
Symmetry		45	50	55	%	
Start-up Time			2	5	ms	65.000~79.999 MHz
			2	5		80.000~124.999 MHz
			2	5		125.000~156.999 MHz
Rise/Fall Time [RL=100Ω, CL=10pF] (Tr/Tf):			0.4	0.7	ns	65.000~79.999 MHz
			0.4	0.5		80.000~124.999 MHz
			0.3	0.5		125.000~156.999 MHz
Phase jitter RMS (12kHz to 20MHz)			0.2	1.0	ps	65.000~79.999 MHz
			0.5	1.0		80.000~124.999 MHz
			0.5	1.0		125.000~156.999 MHz
Period jitter RMS			3.0	5.0	ps	65.000~79.999 MHz
			3.0	5.0		80.000~124.999 MHz
			3.0	5.0		125.000~156.999 MHz

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STANDARD SPECIFICATIONS:

(Continued)

Parameters		Minimum	Typical	Maximum	Units	Notes
Phase Noise (Typical value):	Offset	1kHz	10kHz	100kHz		
	66.660 MHz carrier	-128	-141	-145	dBc	
	100.000 MHz carrier	-130	-140	-141		
	125.000 MHz carrier	-130	-140	-141		
	156.250 MHz carrier	-127	-138	-140		

Key Electrical Specifications for CMOS

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{dd}):			1.5	5	mA	1.000~15.999 MHz
			2.5	8		16.000~39.999 MHz
			5	12		40.000~65.999 MHz
			10	15		66.000~89.999 MHz
			25	35		90.000~124.999 MHz
			30	40		125.000~156.999 MHz
Output Load :			-----	30	pF	
Start-up Time :			4	8	ms	1.000~15.999 MHz
			4	8		16.000~39.999 MHz
			4	8		40.000~65.999 MHz
			5	10		66.000~89.999 MHz
			5	10		90.000~124.999 MHz
			5	10		125.000~156.999 MHz
Output Voltage:	V_{OH}	0.9*Vdd			V	
	V_{OL}			0.1*Vdd	V	
Output Drive Current – 30pF load (IOSD) [VOL = 0.4V, VOH = 2.4V]		10			mA	
Symmetry:		45	50	55	%	
Rise/Fall Time (Tr/Tf)			3	8	ns	1.000~15.999 MHz
			2.5	6		16.000~39.999 MHz
			2	5		40.000~65.999 MHz
			2	4		66.000~89.999 MHz
			2	3.5		90.000~124.999 MHz
			1.5	3		125.000~156.999 MHz

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STANDARD SPECIFICATIONS:

(Continued)

Parameters		Minimum	Typical	Maximum	Units	Notes
Phase jitter RMS (12kHz to 20MHz)			0.3	1.0	ps	1.000~15.999 MHz
			0.3	1.0		16.000~39.999 MHz
			0.2	1.0		40.000~65.999 MHz
			0.2	1.0		66.000~89.999 MHz
			0.2	1.0		90.000~124.999 MHz
			0.2	1.0		125.000~156.999 MHz
Period jitter RMS			3.0	5.0	ps	1.000~15.999 MHz
			3.0	5.0		16.000~39.999 MHz
			3.0	5.0		40.000~65.999 MHz
			3.0	5.0		66.000~89.999 MHz
			3.0	5.0		90.000~124.999 MHz
			3.0	5.0		125.000~156.999 MHz
Phase Noise (Typical value):	Offset	1kHz	10kHz	100kHz	dBc	
	10.000 MHz carrier	-130	-148	-158		
	25.000 MHz carrier	-137	-153	-158		
	50.000 MHz carrier	-135	-150	-158		
	100.000 MHz carrier	-133	-148	-156		

OPTIONS AND PART IDENTIFICATION:

(Left Blank If Standard)

ABNM[ ] - [ ] MHz - [ ][ ] - [ ] - [ ]

Supply Voltage
- Blank: 3.3V
- 2: 2.5V

Frequency in MHz
Please specify the frequency in MHz. e.g. 14.31818MHz

Operating Temp.
- Blank: 0°C ~ +70°C
- D: -10°C ~ +60°C
- E: -20°C ~ +70°C
- F: -30°C ~ +70°C
- N: -30°C ~ +85°C
- L: -40°C ~ +85°C

Overall Freq. Stability
- Blank: ±50ppm
- R: ±25ppm
- K: ±30ppm
- H: ±35ppm

Output
- P1: PECL1
- V: LVDS
- C: CMOS

Packaging
- Blank: Bulk
- T: Tape & Reel

TRI-STATE PIN OPERATION:

Output Type Option		PIN 1 logic level*	Output State
P1	PECL1	1	Enabled
		0	Tri-state
V,C	LVDS,CMOS	0	Tri-state
		1(Default)	Enabled

*Connect to VDD for logic level "1", connect to ground for logic level "0".

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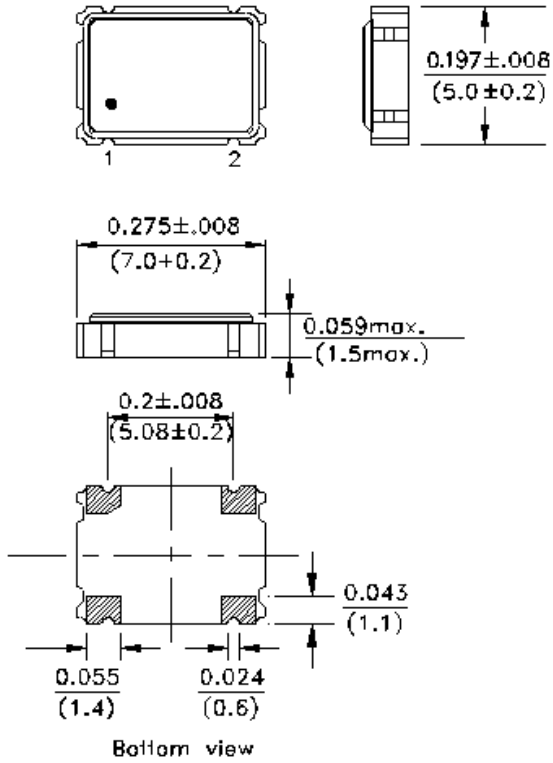
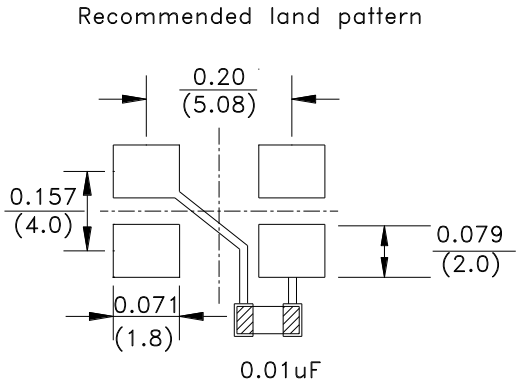
OUTLINE DRAWING:

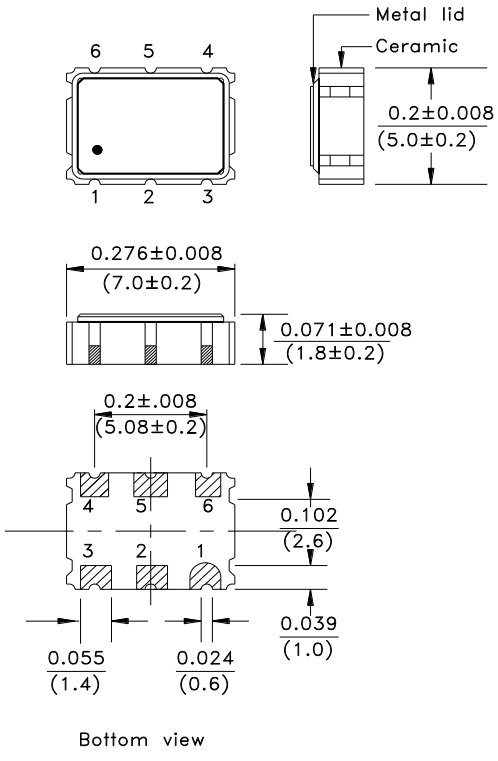
For CMOS Output

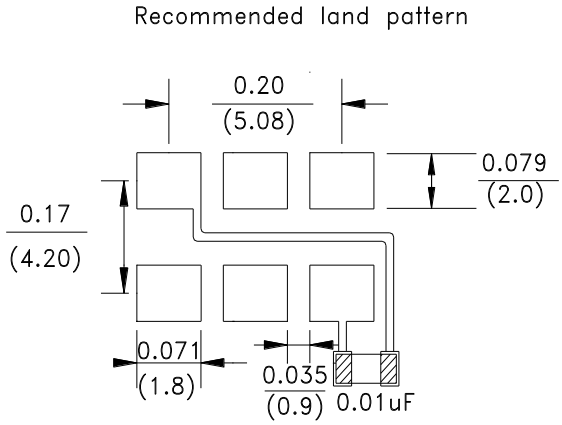




Pin	Function
1	Tri-State
2	GND/Case
3	Output
4	Vdd

For PECL and LVDS Output





Note: Recommend using an approximately 0.01uF bypass capacitor between PIN 3 and 6.

Pin #	Function
1	Tri-state
2	NC
3	GND
4	Q
5	$\overline{Q}$
6	Vdd

Dimensions: inches (mm)

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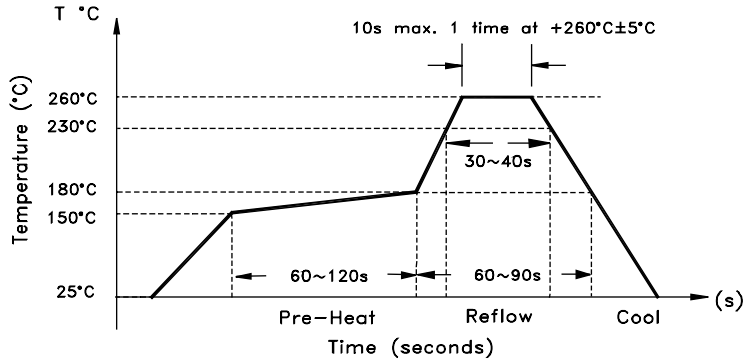
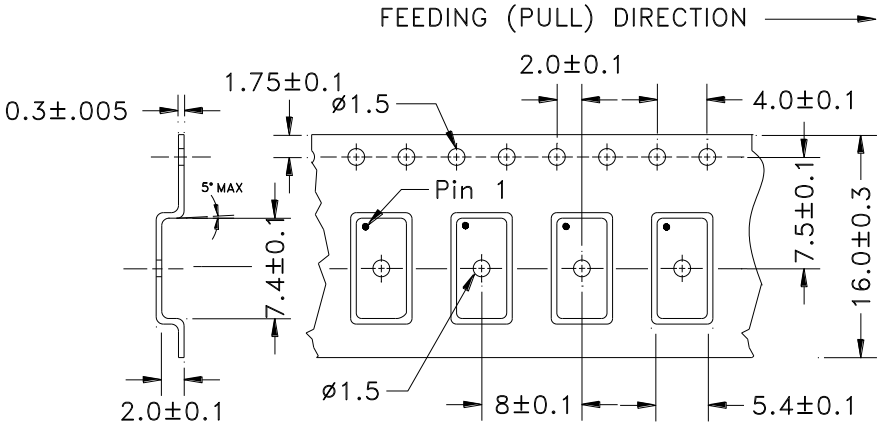
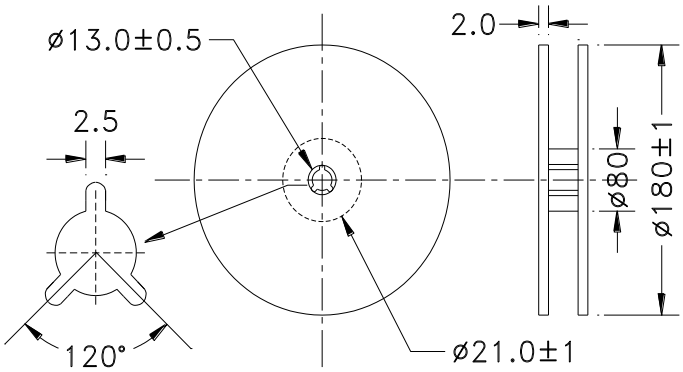
REFLOW PROFILE:



TAPE & REEL:

T= Tape and reel (1,000pcs/reel)





Dimensions: mm

Need a test socket for the ABNM Series? To view compatible PRECISION TEST & BURN-IN SOCKETS for these parts, **click here.**

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