REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. – gt	03-02-10	R. MONNIN
B	Modify drawing to current requirements. - rrp	10-04-27	C. SAFFLE
C	Add device type 02 and case outline X. Make changes to T_J, θ_{JC}, and θ_{JA} under paragraph 1.3. Add enable input, limiter output current, minimum VLOG output load resistance, differential input level, and single ended input level limits under paragraph 1.3. Add a new footnote to θ_{JC} under paragraph 1.3. Add paragraphs 1.4.1, 4.4.1c, 4.4.4.1, 6.7 and Table IIB. For device type 02, add I_{LIM10}, I_{LIM1}, VI_H, V_{IL}, I_{IH}, I_{IL}, P_{IN}, R_{IN}, V_{LIM}, F_{LIM}, P_{INLIM}, V_{LOGM}, t_{STL}, t_{RISE}, and t_{FALL} tests under Table I. - ro	12-04-25	C. SAFFLE
D	Add device type 03. Delete device class M references. - ro	13-04-26	C. SAFFLE

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
RAYMOND MONNIN

DRAWING APPROVAL DATE
99-04-26

REVISION LEVEL
D

MICROCIRCUIT, LINEAR, LOGARITHMIC AMPLIFIER, MONOLITHIC SILICON

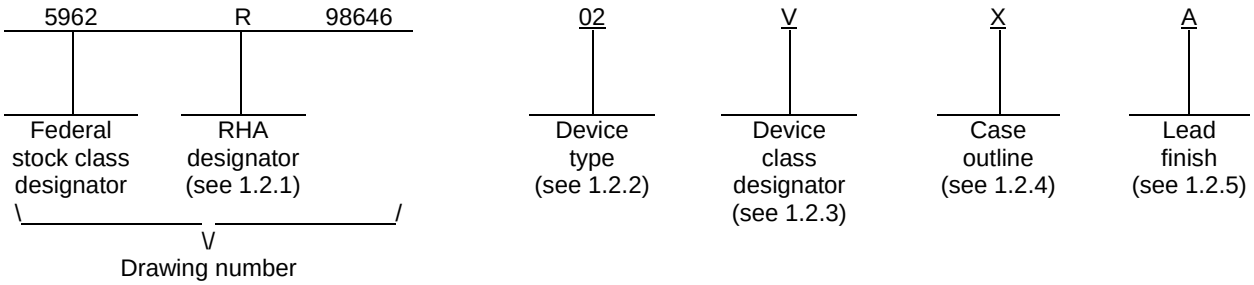
SIZE	CAGE CODE	
A	**67268**	**5962-98646**

SHEET 1 OF 24

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD8306	Logarithmic amplifier
02	AD8306	Logarithmic amplifier
03	AD8306	Logarithmic amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
X	CDFP4-F16	16	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{PS1}/V_{PS2})	7.5 V
Enable input (ENBL)	V_{PS1}/V_{PS2}
Limiter output current (LIMHI, LIMLO)	11 mA
Minimum VLOG output load resistance	40 Ω
Power dissipation (P_D)	800 mW
Input level, differential (reference 50 Ω)	+26 dBm
Input level, single ended (reference 50 Ω)	+20 dBm
Storage temperature range	-65°C to +150°C
Junction temperature (T_J): (both packages)	150°C
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC}) :	
Case outline E	30°C/W
Case outline X	67°C/W 2/
Thermal resistance, junction-to-ambient (θ_{JA}) :	
Case outline E	100°C/W
Case outline X	85°C/W 3/

1.4 Recommended operating conditions.

Operating voltage range (V_{PS1}/V_{PS2})	2.7 V to 6.5 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.4.1 Operating performance characteristics. (T_A = +25°C, V_{PS} = 5 V, unless otherwise specified).

Limiter amplifier section (LIMHI, LIMLO):	
Phase variation at 100 MHz (over input range -73 dBV to -3 dBV)	±2°
Rise / fall time (10% - 90%, R_L = 50 Ω, 40 Ω ≤ R_{LIM} ≤ 400 Ω)	0.6 ns
Logarithmic amplifier section (VLOG):	
± 3 dB error dynamic range (from noise floor to maximum input)	100 dB
Output voltage (input = -91 dBV at V_{PS} = 2.7 V, 5 V)	0.34 V
Output voltage (input = +9 dBV at V_{PS} = 5 V)	2.34 V
Output voltage (input = -3 dBV at V_{PS} = 3 V)	2.10 V
Output resistance	0.3 Ω
Maximum output sink current (to ground)	1 mA
Small signal bandwidth	3.5 MHz
Input stage section (INHI, INLO):	
Equivalent power in 50 Ω (52.3 Ω in parallel with R_{IN})	+22 dBm
Equivalent power in 50 Ω (400 MHz bandwidth)	-78 dBm
Noise floor terminated 50 Ω source	1.28 nV / $\sqrt{Hz}$
Input capacitance (from INHI to INLO)	2.5 pF
DC bias voltage (either INHI, INLO)	1.725 V

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Measurement taken under absolute worst case condition and represents data taken with a thermal camera for highest power density location. See MIL-STD-1835 for average package thermal numbers. Contact the manufacturer for improved thermal limits if LIMHI/LIMLO outputs are not used.

3/ Measurement taken under absolute worst case condition. Data taken with a thermal camera for highest power density location. Contact the manufacturer for improved thermal limits if LIMHI/LIMLO outputs are not used.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s):
For device type 02 ..... 100 krads(Si) 4/
Maximum total dose available (dose rate ≤ 0.10 rads(Si)/s):
For device type 03 ..... 50 krads(Si) 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

_____

4/ Device type 02 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 100 krads(Si).
5/ The device type 03 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition D to a maximum total dose of 50 krads (Si).

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ V_{PS1}/V_{PS2} = ENBL = +5 V, P_{IN} single ended input, unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Quiescent current	I_S	Zero-signal, LMDR open, ENBL > 3 V		1	01	13	20	mA
				2,3		10	24	
		PIN = 0 V, R_{LIM} = open, ENBL = VPS, V_{PS} = 2.7 V, 5 V, 6.5 V		1	02,03	13	20	
				2,3		10	24	
			M, D, P, L, R	1	02	13	20	
			M, D, P, L		03	13	20	
Disable current	I_{DIS}	Zero-signal, LMDR open, ENBL < 0.5 V		1,2,3	01	-25	25	µA
		PIN = 0 V, R_{LIM} = open, ENBL = 0 V, V_{PS} = 2.7 V, 5 V, 6.5 V			02,03	-25	25	
			M, D, P, L, R	1	02	-25	25	
			M,D,P,L		03	-25	25	
Additional I_S current 3/ from 10 mA limiter output drive current	I_{LIM10}	P_{IN} = 0V, ENBL = VPS, R_{LOAD}= 100 Ω, f = 5 MHz, R_{LIM} = 40 Ω (I_{OUT} = 10 mA), V_{PS} = 2.7 V, 5 V, 6.5 V		1,2,3	02,03	8	22.5	mA
			M, D, P, L, R	1	02	8	22.5	
			M,D,P,L		03	8	22.5	
Additional I_S current 3/ from 1 mA limiter output drive current	I_{LIM1}	P_{IN} = 0V, ENBL = VPS, R_{LOAD} = 100 Ω, f = 5 MHz, R_{LIM} = 400 Ω (I_{OUT} = 1 mA), V_{PS} = 2.7 V, 5 V, 6.5 V		1,2,3	02,03	1.5	2.25	mA
			M, D, P, L, R	1	02	1.5	2.25	
			M,D,P,L		03	1.5	2.25	
ENBL input high logic level voltage	V_{IH}	V_{PS} = 2.7 V, 5 V, 6.5 V		1,2,3	02,03	2.7	V_S	V
			M, D, P, L, R	1	02	2.7	V_S	
			M, D, P, L		03	2.7	V_S	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
ENBL input low logic level voltage	V_{IL}	V_{PS} = 2.7 V, 5 V, 6.5 V		1,2,3	02,03	0	0.5	V
			M, D, P, L, R	1	02	0	0.5	
			M, D, P, L		03	0	0.5	
ENBL input high input current	I_{IH}	ENBL = VPS,		1,2,3	02,03		60	µA
		VPS = 2.7 V	M, D, P, L, R	1	02		60	
			M, D, P, L		03		60	
		ENBL = VPS,		1,2,3	02,03		130	
		VPS = 5 V	M, D, P, L, R	1	02		130	
			M, D, P, L		03		130	
		ENBL = VPS,		1,2,3	02,03		160	
		VPS = 6.5 V	M, D, P, L, R	1	02		160	
			M, D, P, L		03		160	
ENBL input low input current	I_{IL}	ENBL = 0 V, VPS = 2.7 V, 5 V, 6.5 V		1,2,3	02,03		60	µA
			M, D, P, L, R	1	02		60	
			M, D, P, L		03		60	
Input INHI and INLO section.								
Usable input signal 4/ 5/ range	P_{IN}	Differential INHI to INLO input level, VPS = 5 V, 6.5 V		4,5,6	02,03	-91	+9	dBV
		Differential INHI to INLO input level, VPS = 2.7 V				-91	+3	
Input resistance 5/	R_{IN}	Differential INHI to INLO		4,5,6	02,03	800	1200	Ω
Limiting amplifier LMHI and LIMLO section.								
Output swing voltage 3/ at 10 mA output drive	V_{LIM10}	R_{LOAD} = 100 Ω, R_{LIM} = 40 Ω (I_{OUT} = 10 mA)		1,2,3	01	0.8	1.2	V
		P_{IN} = -3 dBV, f = 5 MHz, 6/ R_{LOAD} = 100 Ω, R_{LIM} = 40 Ω, V_{PS} = 5 V, 6.5 V		1,2,3	02,03	0.7	1.2	
			M, D, P, L, R	1	02	0.7	1.2	
			M, D, P, L		03	0.7	1.2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Limiting amplifier LMHI and LIMLO section - continued.							
Output swing voltage 3/ at 10 mA output drive	V_{LIM10}	P_{IN} = -3 dBV, f = 5 MHz, 6/ R_{LOAD} = 100 Ω, R_{LIM} = 40 Ω, V_{PS} = 2.7 V	1,2	02,03	0.7	1.2	V
		M, D, P, L, R	1	02	0.7	1.2	
		M, D, P, L		03	0.7	1.2	
		P_{IN} = -3 dBV, f = 5 MHz, 6/ R_{LOAD} = 100 Ω, R_{LIM} = 40 Ω, V_{PS} = 2.7 V	3	02,03	0.5	1.2	
		P_{IN} = -3 dBV, f = 400 MHz, 6/ R_{LOAD} = 100 Ω, R_{LIM} = 40 Ω, V_{PS} = 2.7 V, 5 V, 6.5 V	1,2,3	02,03	0.275	0.6	
Output swing voltage 3/ at 1 mA output drive	VLIM1	PIN = -3 dBV, f = 5 MHz, RLOAD = 100 Ω, RLIM = 400 Ω, V_{PS} = 5 V	1,2,3	02,03	0.07	0.12	V
		M, D, P, L, R	1	02	0.07	0.12	
		M, D, P, L		03	0.07	0.12	
		P_{IN} = -3 dBV, 6/ f = 400 MHz, R_{LOAD} = 100 Ω, R_{LIM} = 400 Ω, V_{PS} = 2.7 V, 5 V, 6.5 V	1,2,3	02,03	0.05	0.14	
Usable frequency range at limiter output	F_{LIM}	R_{LOAD} = 100 Ω, R_{LIM} = 400 Ω at V_{PS} = 5 V, R_{LIM} = 40 Ω at V_{PS} = 2.7 V, 5 V, 6.5 V	4,5,6	02,03	5	400 6/	MHz
		M, D, P, L, R	4	02	5	400 6/	
		M, D, P, L		03	5	400 6/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ V_{PS1}/V_{PS2} = ENBL = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Limiting amplifier LMHI and LIMLO section - continued.							
Usable input signal 4/ 5/ range for limiter	P_{IN} LIM	Differential INHI to INLO input level for limiter, V_{PS} = 5 V, 6.5 V	4,5,6	02,03	-78	+9	dBV
		Differential INHI to INLO input level for limiter, V_{PS} = 2.7 V			-78	+3	
Logarithmic amplifier section.							
Transfer slope	VY_{AC}	f = 10 MHz, -40 dBm < P_{IN} < 0 dBm	4	01	19.4	20.6	mV/dB
			5,6		19.25	20.75	
		f = 5 MHz, -63 dBV < P_{IN} < -23 dBV	4	02,03	19.7	20.9	
			5,6		19.55	21.05	
		M, D, P, L, R	4	02	19.7	20.9	
		M, D, P, L		03	19.7	20.9	
		f = 100 MHz, -63 dBm < P_{IN} < -23 dBm	4	02,03	19.4	20.6	
			5,6		19.25	20.75	
		M, D, P, L, R	4	02	19.4	20.6	
		M, D, P, L		03	19.4	20.6	
Transfer slope	VY_{AC}	f = 400 MHz, 6/ -63 dBm < P_{IN} < -23 dBm	4,5,6	02,03	18.5	19.2	mV/dB
Intercept	VXAC	f = 10 MHz	4	01	-110.4	-105.6	dBV
			5,6		-111.0	-105.0	
		f = 5 MHz	4	02,03	-110.4	-105.6	
			5,6		-111.0	-105.0	
		M, D, P, L, R	4	02	-110.4	-105.6	
		M, D, P, L		03	-110.4	-105.6	
		f = 100 MHz	4	02,03	-108.4	-103.6	
			5,6		-109.0	-103.0	
		M, D, P, L, R	4	02	-108.4	-103.6	
		M, D, P, L		03	-108.4	-103.6	
		f = 400 MHz 6/	4,5,6	02,03	-112	-107.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ V_{PS1}/V_{PS2} = ENBL = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logarithmic amplifier section – continued.							
Linearity error	LEAC	f = 10 MHz, -40 dBm < PIN < 0 dBm	4,5,6	01	-1.0	1.0	dB
		f = 5 MHz, 100 MHz, 6/ 400 MHz, -63 dBV < PIN < -23 dBV	4,5,6	02,03	-1.0	1.0	
		M, D, P, L, R	4	02	-1.0	1.0	
		M, D, P, L		03	-1.0	1.0	
VLOG maximum 7/ output voltage	V_{LOGM}	P_{IN} = +3 dBV at V_{PS} = 5 V, f = 5 MHz and 100 MHz	4,5,6	02,03	1.9	2.3	V
		P_{IN} = +3 dBV at V_{PS} = 6.5 V, f = 5 MHz			1.9	2.3	
		P_{IN} = -3 dBV at V_{PS} = 2.7 V, f = 5 MHz			1.9	2.3	
		M, D, P, L, R	4	02	1.9	2.3	
		M, D, P, L		03	1.9	2.3	
Output settling 5/ 7/ time to 10%	T_{STL}	P_{IN} = 0 V to 3.991 V step (+3 dBV), settle to 10%, f = 100 MHz, $R_{VLOGLOAD} \ge 50\ \Omega$, $C_{VLOGLOAD} \le 100$ pF	9,10,11	02,03		130	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_A \le +125°C$ V_{PS1}/V_{PS2} = ENBL = +5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logarithmic amplifier section – continued.							
Rise and fall time 5/ 7/ 10% to 90%	t_{RISE} t_{FALL}	P_{IN} = 0 V to 3.991 V step (+3 dBV), 10% to 90%, f = 100 MHz, $R_{VLOGLOAD} \ge 50\ \Omega$, $C_{VLOGLOAD} \le 100$ pF	9,10,11	02,03		100	ns

1/ Device type 02 supplied to this drawing has been characterized through all levels P, L, and R of irradiation. Device type 03 has been characterized through all levels P and L irradiation. However, device type 02 is tested only at the "R" level and device type 03 is only tested at the "L" level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ Device type 02 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A for device type 02 and condition D for device type 03. Device type 03 has been tested at low dose rate.

3/ Output swing is from V_{PS} to $V_{PS} - V_{LIM}$ swing voltage. When limiter output is used, output drive current is nominally 400mV/R_{LIM} which increases I_S as specified in I_{LIM}. R_{LIM} should be chosen for desired output swing and optimal application needs. When Limiter outputs are not used, it is recommended to disable the LIMHI and LIMLO outputs by connecting them to V_{PS2}. Refer to section 6.7 application notes.

4/ Due to the extremely high Gain bandwidth product, the output of either LIMHI or LIMLO will be unstable for P_{IN} input levels below –78 dBV (–65 dBm, reference 50 Ω). Power supply level, input circuitry, single ended versus differential input, and LIMHI/LIMLO circuitry alter the P_{IN} and P_{INLIM} specifications. Refer to section 6.7 application notes.

5/ Parameter is guaranteed by engineering characterization, not production tested. Characterization repeated after major design or process changes or with subsequent wafer lots. Parameter not tested post irradiation.

6/ Limits production tested at f = 5 MHz and 100 MHz, while f = 400 MHz limits are guaranteed by engineering characterization, not production tested. Characterization repeated after major design or process changes or with subsequent wafer lots. f = 400 MHz limits not tested post irradiation.

7/ Maximum V_{LOG} output sink current can increase V_{LOG} output settling and fall time. This may be reduced by adding a grounded load resistance though this must not be less than 40 Ω. Select bandwidth limiting filter as needed per application needs. Power supply level, input circuitry, and V_{LOG} application circuitry alter this specification. Refer to section 6.7 application notes.

Device types	01 02, and 03
Case outlines	E and X (See note)
Terminal number	Terminal symbol
1	COM2
2	VPS1
3	PADL
4	INHI
5	INLO
6	PADL
7	COM1
8	ENBL
9	LMDR
10	FLTR
11	PADL
12	LMLO
13	LMHI
14	PADL
15	VPS2
16	VLOG

Terminal symbol	Description
COM2	Special common pin for received signal strength indication (RSSI) output.
VPS1	Supply pin for first five amplifier stages and the main biasing system.
PADL	Four tie-downs to the paddle on which the device is mounted; grounded
INHI	Signal input, high or plus polarity.
INLO	Signal input, low or minus polarity.
COM1	Main common connection.
ENBL	Chip enable; active when high. Refer to ENBL enable interface section of the manufacturer's datasheet.
LMDR	Limiter drive programming pin.
FLTR	Received signal strength indication (RSSI) bandwidth reduction pin.
LMLO	Limiter output, low or minus polarity.
LMHI	Limiter output, high or plus polarity.
VPS2	Supply pin for sixth gain stage, limiter and received signal strength indication (RSSI) output stage load current.
VLOG	Logarithmic received signal strength indication (RRSI) output.

NOTE: Metal package lid can be grounded.

FIGURE 1. Terminal connections.

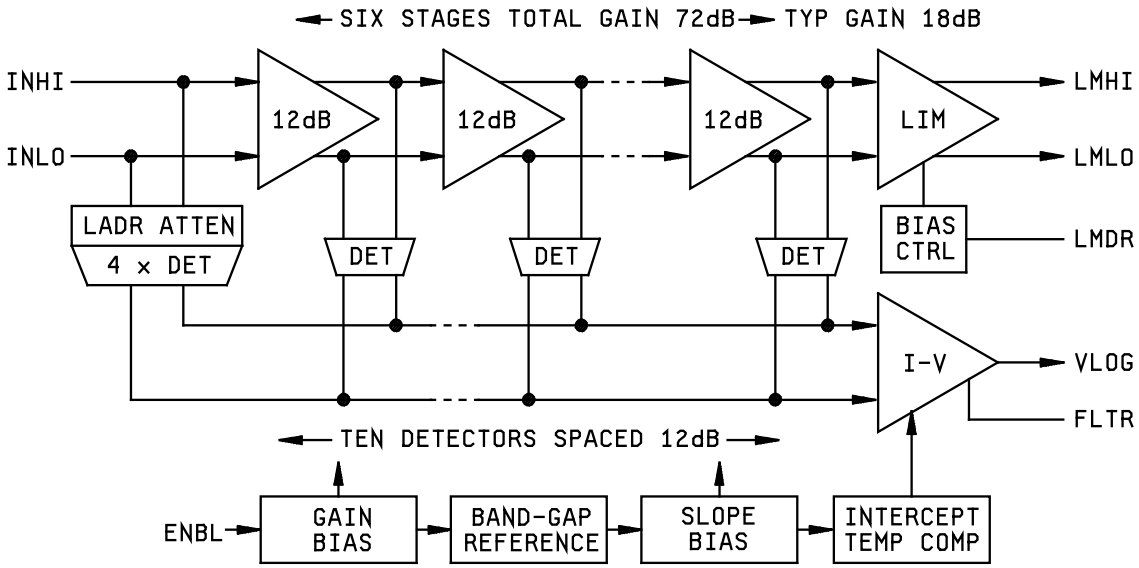


FIGURE 2. Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 4, 5, 6, 9, 10, and 11 are tested as part of device initial characterization and after design and process changes or with subsequent wafer lots as indicated in Table I.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/	1,2,3, 1/ 2/ 3/ 4,5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6, 2/ 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1,2,3, 2/ 3/ 4,5,6,9,10,11
Group D end-point electrical parameters (see 4.4)	1	1,2,3,4,5,6 2/
Group E end-point electrical parameters (see 4.4)	1,4	1,4 2/

1/ PDA applies to subgroup 1.
2/ See Table I for parameters tested or characterized for subgroups 4, 5, 6, 9, 10, and 11.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test delta parameters. T_A = +25°C. 1/ 2/

Parameters	Symbol	Condition	Delta limits	Units
Quiescent current	I_S	V_{PS} = 6.5 V	±0.8	mA
Output swing voltage	V_{LIM10}	V_{PS} = 6.5 V, f = 5 MHz	±0.05	V
High input current	I_{IH}	V_{PS} = 6.5 V	±12	µA
Low input current	I_{IL}	V_{PS} = 6.5 V	±12	µA
Additional I_S current from 10 mA limiter output drive current	I_{LIM10}	V_{PS} = 6.5 V	±0.5	mA
Disable current	I_{DIS}	V_{PS} = 6.5 V	±5	µA
Linearity	LEAC	V_{PS} = 5 V, f = 5 MHz	±0.4	dB

1/ Deltas are performed at room temperature.
2/ 240 hour burn-in and 1,000 hour operating group C life test.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A for device type 02 and condition D for device type 03 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Application notes.

The device (figure 2) comprises a chain of six main amplifier/limiter stages, each having a gain of 12.04 dB (X4) and small-signal –3 dB bandwidth of 850 MHz. The input interface at INHI and INLO pins is fully differential. Thus it may be driven from either single-sided or balanced inputs, the latter being required at the very top end of the dynamic range, where the total differential drive may be as large as 4 V in amplitude.

The first six stages, also used in developing the logarithmic RSSI output, are followed by a versatile programmable-output, and thus programmable-gain, final limiter section. Its open collector outputs are also fully differential, at LMHI and LMLO pins. This output stage provides a gain of 18 dB when using equal valued load and bias setting resistors and the pin-to-pin output is used. The overall voltage gain is thus 90 dB. When using $R_{LIM} = R_{LOAD} = 200\ \Omega$, the additional current consumption in the limiter is approximately 2.8 mA, of which 2 mA goes to the load. The ratio depends on R_{LIM} (for example, when 20 Ω, the efficiency is 90%), and the voltage at the pin LMDR is rather more than 400 mV, but the total load current is accurately (400 mV)/R_{LIM}. The rise and fall times of the hard-limited (essentially square wave) voltage at the outputs are normally 0.6 ns, when driven by a sine wave input having an amplitude of 316 mV or greater, and $R_{LOAD} = 50\ \Omega$. The change in time-delay ("phase skew") over the input range –73 dBV (316 mV in amplitude, or –60 dBm in 50 Ω) to –3 dBV (1 V or +10 dBm) is normally ±56 ps (±2° at 100 MHz).

The six main cells and their associated full-wave detectors, having a transconductance (gm) form, handle the lower part of the dynamic range. Biasing for these cells is provided by two references, one of which determines their gain, the other being a band-gap cell which determines the logarithmic slope, and stabilizes it against supply and temperature variations. A special dc-offset-sensing cell (not shown in figure 2) is placed at the end of this main section, and used to null any residual offset at the input, ensuring accurate response down to the noise floor. The first amplifier stage provides a short-circuited voltage noise spectral density of approximately 1.07 nV/$\sqrt{\text{Hz}}$. The last detector stage includes a modification to temperature stabilize the log intercept, which is accurately positioned so as to make optimal use of the full output voltage range. Four further "top end" detectors are placed at 12.04 dB taps along a passive attenuator, to handle the upper part of the range. The differential current mode outputs of all ten detectors stages are summed with equal weightings and converted to a single sided voltage by the output stage, generating the logarithmic (or RSSI) output at VLOG pin, nominally scaled 20 mV/dB (that is, 400 mV per decade). The junction between the lower and upper regions is seamless, and the logarithmic law conformance is normally well within ±0.4 dB over the 80 dB range from –80 dBV to 0 dBV (–67 dBm to +13 dBm).

The full scale rise time of the RSSI output stage, which operates as a two-pole low-pass filter with a corner frequency of 3.5MHz, is about 200 ns. A capacitor connected between FLTR pin and VLOG can be used to lower the corner frequency (see below). The output has a minimum level of about 0.34 V (corresponding to a noise power of –78 dBm, or 17 dB above the nominal intercept of –95 dBm). This rather high baseline level ensures that the pulse response remains unimpaired at very low inputs. The maximum RSSI output depends on the supply voltage and the load. An output of 2.34 V, that is, 20 mV/dB ´ (9 + 108) dB, is normal when using a supply voltage of 4.5 V or greater and a load resistance of 50 Ω or higher, for a differential input of +9 dBV (a 4 V sine amplitude, using balanced drives). When using a 3 V supply, the maximum differential input may still be as high as –3 dBV (1 V sine amplitude), and the corresponding RSSI output of 2.1 V, that is, 20 mV/dB (–3 + 108) dB is normal.

A fully programmable output interface is provided for the hard limited signal, permitting the user to establish the optimal output current from its differential current-mode output. Its magnitude is determined by the resistor R_{LIM} placed between LMDR pin and ground, across which a nominal bias voltage of ~400 mV appears. Using R_{LIM} = 200 Ω, this dc bias current, which is commutated alternately to the output pins, LMHI and LMLO, by the signal, is 2 mA. (The total supply current is somewhat higher). These currents may readily be converted to voltage form by the inclusion of load resistors, which will normally range from a few tens of ohms at 400 MHz to as high as 2 kΩ in lower frequency applications. Alternatively, a resonant load may be used to extract the fundamental signal and modulation sidebands, minimizing the out-of-band noise. A transformer or impedance matching network may also be used at this output. The peak voltage swing down from the supply voltage may be 1.2 V, before the output transistors go into saturation. The supply current for all sections except the limiter output stage, and with no load attached to the RSSI output, is nominally 16 mA at T_A = 27°C, substantially independent of supply voltage. It varies in direct proportion to the absolute temperature (PTAT). The RSSI load current is simply the voltage at VLOG divided by the load resistance (for example, 2.4 mA max in a 1 kΩ load). The limiter supply current is 1.1 times that flowing in RLIM. The device may be enabled/disabled by a CMOS compatible level at ENBL pin.

ENBL enable interface.
The chip-enable interface is shown in Figure 3. The current in R1 controls the turn-on and turn-off states of the band-gap reference and the bias generator. Left unconnected, or at any voltage below 1 V, the device will be disabled, when it consumes a sleep current of much less than 1 mA (leakage currents only); when tied to the supply, or any voltage above 2 V, it will be fully enabled. The internal bias circuitry requires approximately 300 ns for either OFF or ON, while a delay of some 6 ms is required for the supply current to fall below 10 mA.

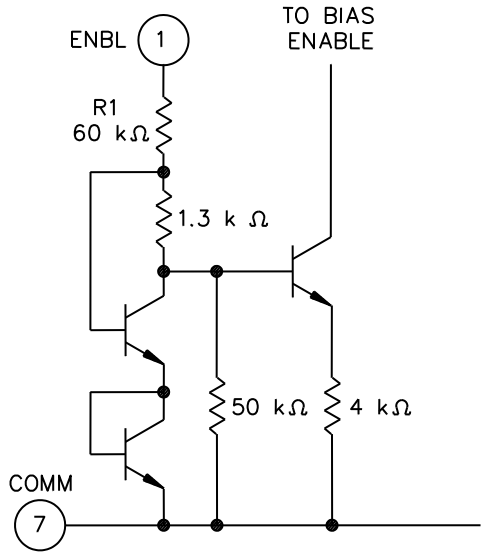


Figure 3. Enable interface.

INHI/INLO input interface.

Figure 4 shows the essentials of the signal input interface. The parasitic capacitances to ground are labeled C_P; the differential input capacitance, C_D, mainly due to the diffusion capacitance of Q1 and Q2. In most applications both input pins are AC coupled. The switch S closes when Enable is asserted. When disabled, the inputs float, bias current IE is shut off, and the coupling capacitors remain charged. If the log amp is disabled for long periods, small leakage currents will discharge these capacitors. If they are poorly matched, charging currents at power-up can generate a transient input voltage which may block the lower reaches of the dynamic range until it has become much less than the signal.

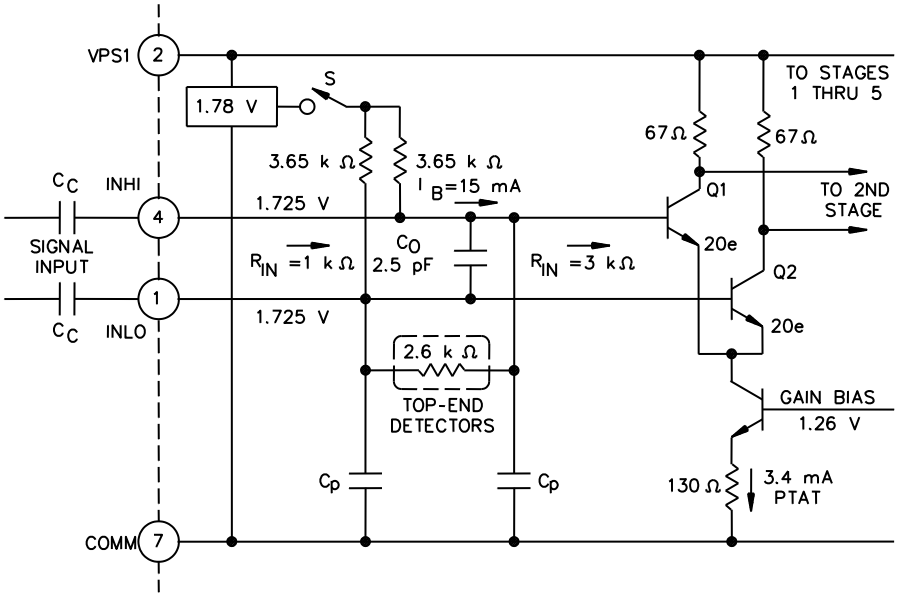


FIGURE 4. Signal input interface.

In most applications, the input signal will be single sided, and may be applied to either INHI or INLO pin, with the remaining pin AC coupled to ground. Under these conditions, the largest input signal that can be handled is –3 dBV (sine amplitude of 1 V) when operating from a 3 V supply; a +3 dBV input may be handled using a supply of 4.5 V or greater. When using a fully balanced drive, the +3 dBV level may be achieved for the supplies down to 2.7 V and +9 dBV using > 4.5 V. For frequencies in the range 10 MHz to 200 MHz these high drive levels are easily achieved using a matching network. Using such a network, having an inductor at the input, the input transient is eliminated.

LIMHI/LIMLO limiter output interface.
The simplified limiter output stage is shown in Figure 5. The bias for this stage is provided by a temperature-stable reference voltage of nominally 400 mV which is forced across the external resistor RLIM connected from LMDR pin by a special operational amplifier buffer stage. The biasing scheme also introduces a slight "lift" to this voltage to compensate for the finite current gain of the current source Q3 and the output transistors Q1 and Q2. A maximum current of 10 mA is permissible (R_{LIM} = 40 Ω). Note that while the bias currents are temperature stable, the ac gain of this stage will vary with temperature, by –6 dB over a 120°C range. A pair of supply and temperature stable complementary currents is generated at the differential output LMHI pin and LMLO pin, having a square wave form with rise and fall times of normally 0.6 ns, when load resistors of 50 Ω are used. The voltage at these output pins may swing to 1.2 V below the supply voltage applied to VPS2 pin. Because of the very high gain bandwidth product of this amplifier considerable care must be exercised in using the limiter outputs. The minimum necessary bias current and voltage swings should be used. These outputs are best utilized in a fully-differential mode. A flux-coupled transformer, a balun, or an output matching network can be selected to transform these voltages to a single-sided form. Equal load resistors are recommended, even when only one output pin is used, and these should always be returned to the same well decoupled node on the printed circuit (PC) board. When the device is used only to generate an RSSI output, the limiter should be completely disabled by omitting RLIM and strapping LMHI and LMLO to VPS2.

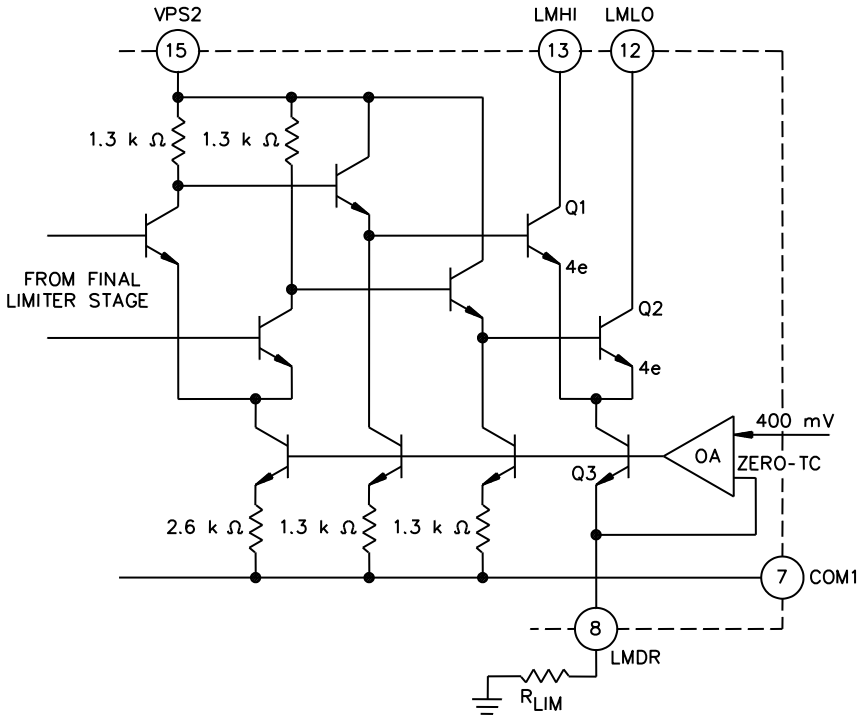


FIGURE 5. Limiter output interface.

VLOG (RSSI) output interface.
The outputs from the ten detectors are differential currents, having an average value that is dependent on the signal input level, plus a fluctuation at twice the input frequency. The currents are summed at the internal nodes LGP and LGN shown in figure 6. The temperature compensation current (I_T) is added to LGP, to position the intercept to –108 dBV, by raising the RSSI output voltage for zero input, and to provide temperature compensation, resulting in a stable intercept. For zero signal conditions, all the detector output currents are equal. For a finite input, of either polarity, their difference is converted by the output interface to a single sided voltage nominally scaled 20 mV/dB (400 mV per decade), at the output VLOG pin. This scaling is controlled by a separate feedback stage, having a tightly controlled transconductance. A small uncertainty in the log slope and intercept remains; the intercept may be adjusted.

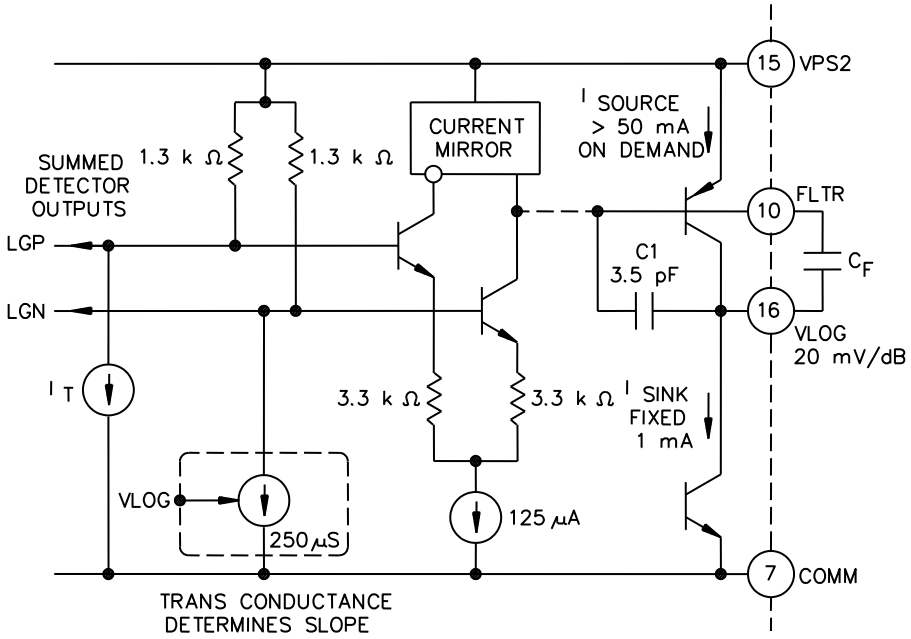


FIGURE 6. Simplified RSSI output interface.

The RSSI output bandwidth, f_{LP}, is nominally 3.5 MHz. This is controlled by the compensation capacitor C1, which may be increased by adding an external capacitor, C_F, between FLTR pin and VLOG pin. An external 33 pF will reduce f_{LP} to 350 kHz, while 360 pF will set it to 35 kHz, in each case with an essentially one-pole response. In general, the relationships (for f_{LP} in MHz) are:

$C_F = ((12.7 \times 10^{-10}) / f_{LP}) - 3.5$ pF; $f_{LP} = (12.7 \times 10^{-6}) / (C_F + 3.5$ pF).

Using a load resistance of 50 Ω or greater, and at any temperature, the peak output voltage may be at least 2.4 V when using a supply of 4.5 V, and at least 2.1 V for a 3 V supply, which is consistent with the maximum permissible input levels. The incremental output resistance is approximately 0.3 Ω at low frequencies, rising to 1 Ω at 150 kHz and 18 Ω at very high frequencies. The output is unconditionally stable with load capacitance, but it should be noted that while the peak sourcing current is over 100 mA, and able to rapidly charge even large capacitances, the internally provided sinking current is only 1 mA. Thus, the fall time from the 2 V level will be as long as 2 μs for a 1 nF load. This may be reduced by adding a grounded load resistance though this must not be less than 40 Ω.

Using the device.
The device exhibits very high gain from 1 MHz to over 1 GHz, at which frequency the gain of the main path is still over 65 dB. Consequently, it is susceptible to all signals, within this very broad frequency range, that find their way to the input terminals. It is important to remember that these are quite indistinguishable from the “wanted” signal, and will have the effect of raising the apparent noise floor (that is, lowering the useful dynamic range). Therefore, while the signal of interest may be 200 MHz, any of the following could easily be larger than this signal at the lower extremities of its dynamic range: a 60 Hz hum, picked up due to poor grounding techniques; spurious coupling from digital logic on the same PC board; a strong electromagnetic interference (EMI) source; etc. Very careful shielding is essential to guard against such unwanted signals, and also to minimize the likelihood of instability due to high frequency (HF) feedback from the limiter outputs to the input.

With this in mind, the minimum possible limiter gain should be used. Where only the logarithmic amplifier (RSSI) function is required, the limiter should be disabled by omitting RLIM and tying the outputs LMHI and LMLO directly to VPS2. A good ground plane should be used to provide a low impedance connection to the common pins, for the decoupling capacitor(s) used at VPS1 and VPS2, and at the output ground. Note that COM2 is a special ground pin serving just the RSSI output. The four pins labeled PADL tie down directly to the back of the chip. The process on which the device is fabricated uses a bonded wafer technique to provide a silicon-on-insulator isolation, and there is no junction or other dc path from the back side to the circuitry on the surface. These paddle pins must be connected directly to the ground plane using the shortest possible lead lengths to minimize inductance. The voltages at the two supply pins should not be allowed to differ greatly; up to 500 mV is permissible. It is desirable to allow VPS1 to be slightly more negative than VPS2. When the primary supply is greater than 2.7 V, the decoupling resistors R1 and R2 (figure 7) may be increased to improve the isolation and lower the dissipation in the device. However, since VPS2 supports the RSSI load current, which may be large, the value of R2 should take this into account.

Basic connections for VLOG (RSSI) output.
Figure 7 shows the connections required for most applications. The device is enabled by connecting ENBL to VPS1. Inputs are ac-coupled by C1 and C2, which normally should have the same value. The input is, in this case, terminated with a 52.3 Ω resistor that combines with the device’s input resistance of 1000 Ω to give a broadband input impedance of 50 Ω. Alternatively an input matching network can be used (see input matching section).

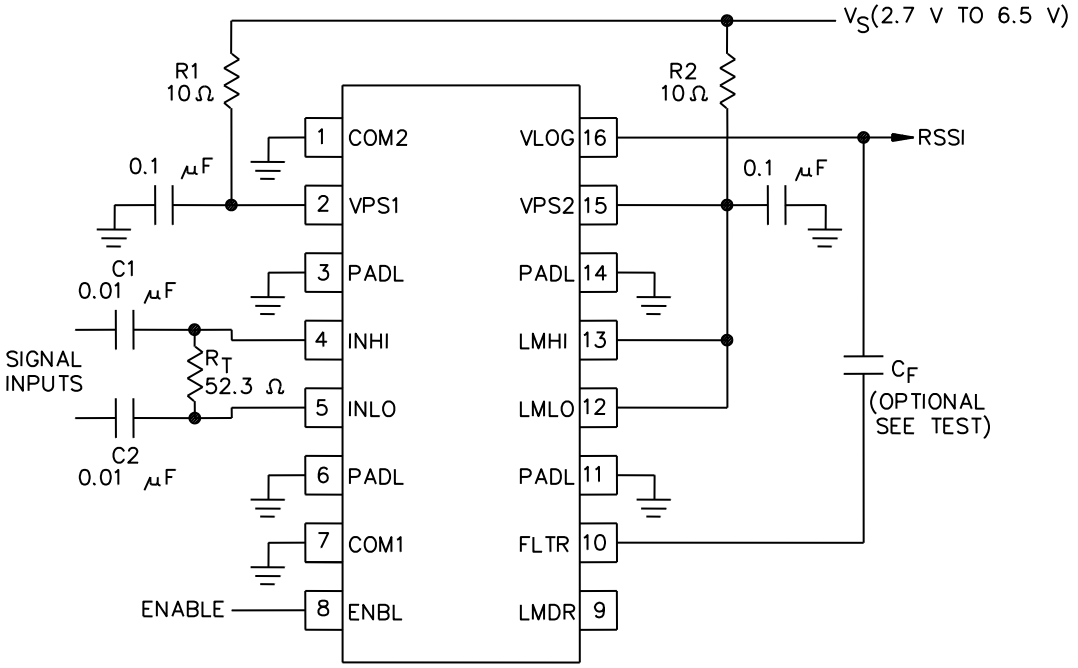


FIGURE 7. Bias connections for RSSI (log) output.

The 0.01 μF coupling capacitors and the resulting 50 Ω input impedance give a high-pass corner frequency of around 600 kHz. (1/(2 π RC)), where C = (C1)/2. In high frequency applications, this corner frequency should be placed as high as possible, to minimize the coupling of unwanted low frequency signals. In low frequency applications, a simple RC network forming a low pass filter should be added at the input for the same reason. If the limiter output is not required, LMDR pin should be left open and LMHI pin and LMLO pin should be tied to VPS2 as shown in figure 7.

Transfer function in terms of slope and intercept.
The transfer function of the device is characterized in terms of its slope and intercept. The logarithmic slope is defined as the change in the RSSI output voltage for a 1 dB change at the input. For the device the slope is calibrated to be 20 mV/dB. The intercept is the point at which the extrapolated linear response would intersect the horizontal axis. For the device the intercept is calibrated to be –108 dBV (–95 dBm). Using the slope and intercept, the output voltage can be calculated for any input level within the specified input range using the equation: V_{OUT} = VSLOPE X (PIN – PO) where V_{OUT} is the demodulated and filtered RSSI output, VSLOPE is the logarithmic slope, expressed in V/dB, PIN is the input signal, expressed in decibels relative to some reference level (either dBm or dBV in this case) and PO is the logarithmic intercept, expressed in decibels relative to the same reference level. For example, for an input level of –33 dBV (–20 dBm), the output voltage will be: V_{OUT} = 0.02 V/dB X (–33 dBV – (–108 dBV)) = 1.5 V.

The most widely used convention in RF systems is to specify power in dBm, that is, decibels above 1 mW in 50 Ω. Specification of log amp input level in terms of power is strictly a concession to popular convention; they do not respond to power (tacitly "power absorbed at the input"), but to the input voltage. The use of dBV, defined as decibels with respect to a 1 V rms sine wave, is more precise, although this is still not unambiguous because waveform is also involved in the response of a log amp, which, for a complex input (such as a CDMA signal) will not follow the rms value exactly. Since most users specify RF signals in terms of power more specifically, in dBm/50 Ω, we use both dBV and dBm in specifying the performance of the device, showing equivalent dBm levels for the special case of a 50 Ω environment. Values in dBV are converted to dBm with regard to 50 Ω by adding 13.

Output response time and CF.
The RSSI output has a low-pass corner frequency of 3.5 MHz, which results in a 10% to 90% rise time of 73 ns. For low frequency applications, the corner frequency can be reduced by adding an external capacitor, CF, between FLTR pin and VLOG pin as shown in figure 7. For example, an external 33 pF will reduce the corner frequency to 350 kHz, while 360 pF will set it to 35 kHz, in each case with an essentially one-pole response.

Using the LIMHI/LIMLO limiter output.
Figure 8 shows the basic connections for operating the limiter and the log output concurrently. The limiter output is a pair of differential currents of magnitude, IOUT, from high impedance (open-collector) sources. These are converted to equal-amplitude voltages by supply-referenced load resistors, R_{LOAD}. The limiter output current is set by RLIM, the resistor connected between LMDR pin and ground. The limiter output current is set according the equation: $I_{OUT} = -400mV/R_{LIM}$ and has an absolute accuracy of ±5%. The supply referenced voltage on each of the limiter pins will thus be given by: $V_{LIM} = V_S - 400mV \times R_{LOAD}/ R_{LIM}$.

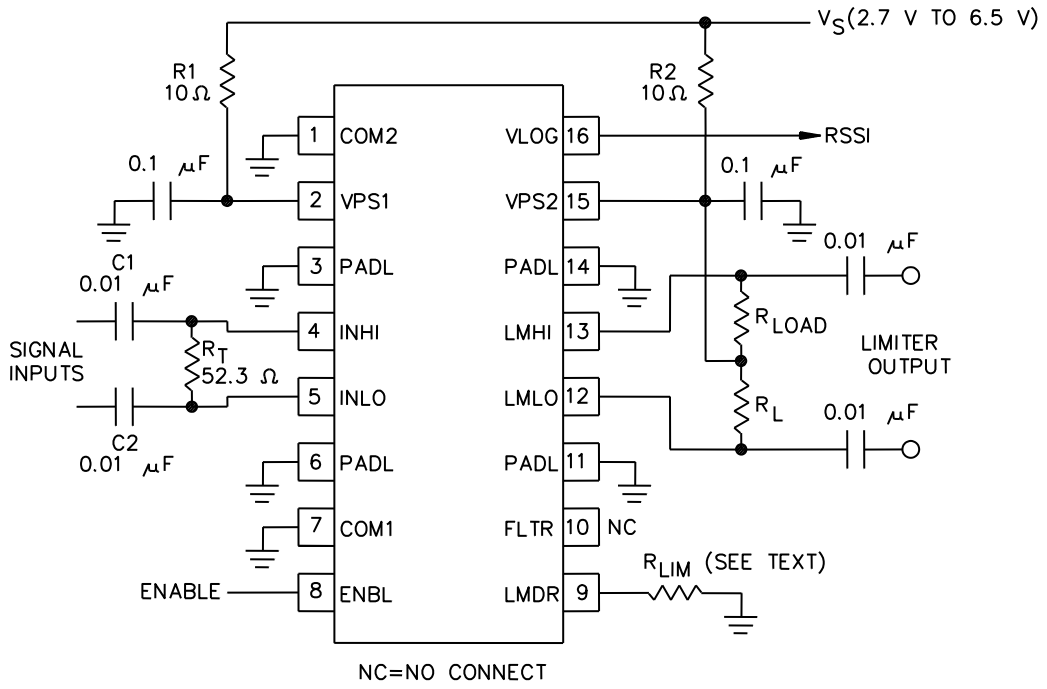


FIGURE 8. Basic connections for operating the limiter.

Depending on the application, the resulting voltage may be used in a fully balanced or unbalanced manner. It is good practice to retain both load resistors, even when only one output pin is used. These should always be returned to the same well decoupled node on the PC board. The unbalanced, or single-sided mode, is more inclined to result in instabilities caused by the very high gain of the signal path. The limiter current may be set as high as 10 mA (which requires R_{LIM} to be 40 Ω) and can be optionally increased somewhat beyond this level. It is generally inadvisable, however, to use a high bias current, since the gain of this wide bandwidth signal path is proportional to the bias current, and the risk of instability is elevated as R_{LIM} is reduced (recommended value is 400 Ω). However, as the size of R_{LOAD} is increased, the bandwidth of the limiter output decreases from 585 MHz for $R_{LOAD} = R_{LIM} = 50$ Ω to 50 MHz for $R_{LOAD} = R_{LIM} = 400$ Ω (bandwidth = 210 MHz for $R_{LOAD} = R_{LIM} = 100$ Ω and 100 MHz for $R_{LOAD} = R_{LIM} = 200$ Ω). As a result, the minimum necessary limiter output level should be chosen while maintaining the required limiter bandwidth. For $R_{LIM} = R_{LOAD} = 50$ Ω, the limiter output is specified for input levels between –78 dBV (–65 dBm) and +9 dBV (+22 dBm). The output of the limiter may be unstable for levels below –78 dBV (–65 dBm). However, keeping R_{LIM} above 100 Ω will make instabilities on the output less likely for input levels below –78 dBV. A transformer or a balun (for example, MACOM part number ETC1-1-13) can be used to convert the differential limiter output voltages to a single-ended signal.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-04-26

Approved sources of supply for SMD 5962-98646 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9864601QEA	24355 (2)	AD8306A/QMLQ
5962R9864602VXA	24355 (4)	AD8306AF/QMLR
5962L9864603VXA	24355 (4)	AD8306AF/QMLL

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices (2) Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462
24355	Analog Devices (4) Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605