REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22												
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
RICK OFFICER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dla.mil/landandmaritime

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DRAWING APPROVAL DATE
17-12-14

REVISION LEVEL

MICROCIRCUIT, LINEAR, 30 V, LOW NOISE, RAIL TO RAIL INPUT/OUTPUT, LOW POWER QUAD OPERATIONAL AMPLIFIER, MONOLITHIC SILICON

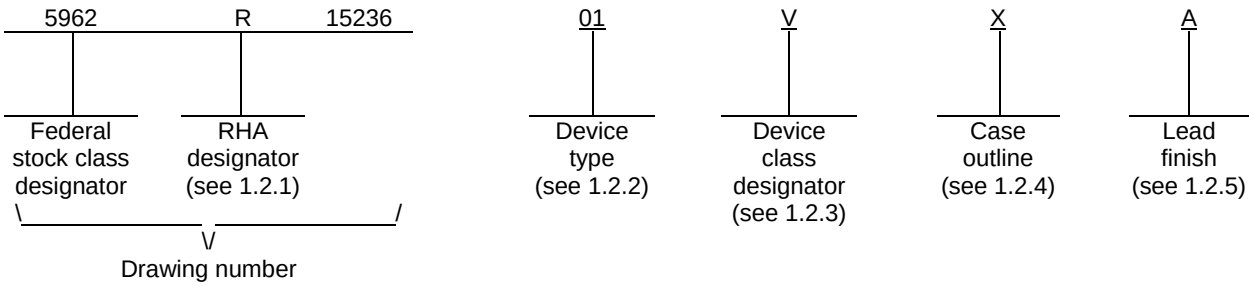
SIZE	CAGE CODE	
A	**67268**	**5962-15236**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADA4084-4	Radiation hardened, 30 V low noise, rail-to-rail input/output, low power quad operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F14	14	Bottom brazed flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (+V_S to -V_S)	36 V
Input voltage (V_{IN})	-V_S ≤ V_{IN} ≤ +V_S
Differential input voltage (V_{ID})	±0.6 V 2/
Output short circuit duration to GND	Indefinite
Power dissipation (P_D)	64 mW
Storage temperature range	-65°C to +150°C
Junction temperature (T_J) range	-65°C to +150°C
Lead temperature (soldering, 60 seconds)	+300°C
Electrostatic discharge (ESD) rating:	
Human body model (HDM)	4.5 kV
Machine model (MM)	200 V
Field induced charge device model (FICDM)	1.25 kV
Thermal resistance, junction-to-case (θ_{JC})	33°C/W 3/
Thermal resistance, junction-to-ambient (θ_{JA})	63°C/W 3/

1.4 Recommended operating conditions.

Dual supply voltage (±V_S)	±1.5 V to ±15.0 V
Single supply voltage (+V_S / 0 V)	+3.0 V to +30.0 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.4.1 Operating performance characteristics.

V_S = ±1.5 V.

Differential input resistance	100 kΩ
Differential input capacitance	1.1 pF
Common mode input resistance	80 MΩ
Common mode input capacitance	2.9 pF
Unity gain crossover, V_{IN} = 5 V_{PP}, R_L = 10 kΩ, A_V = 1	8.08 MHz
Phase margin	86 Degrees
Settling time, A_V = 10, V_{IN} = 2 V_{PP}, 0.1%	4 μs
Current noise density, f = 1 kHz	0.55 pA/$\sqrt{Hz}$

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ For input differential voltages greater than 0.6 V, limit the input current to less than 5 mA to prevent degradation or destruction of the input devices.

3/ Measurement taken under absolute worst case condition of still air and represent data taken with a thermal camera for highest power density location. See MIL-STD-1835 for average package θ_{JC} thermal numbers with smaller die size.

1.4.1 Operating performance characteristics - continued.

V_S = ±5.0 V.

Differential input resistance	100 kΩ
Differential input capacitance	1.1 pF
Common mode input resistance	200 MΩ
Common mode input capacitance	2.5 pF
Unity gain crossover, V_{IN} = 5 V_{PP}, R_L = 10 kΩ, A_V = 1	9.6 MHz
Phase margin	85 Degrees
Settling time, A_V = 10, V_{IN} = 8 V_{PP}, 0.1%	4 μs
Current noise density	0.55 pA/ $\sqrt{Hz}$

V_S = ±15.0 V.

Differential input resistance	100 kΩ
Differential input capacitance	1.1 pF
Common mode input resistance	200 MΩ
Common mode input capacitance	2.5 pF
Unity gain crossover, V_{IN} = 5 V_{PP}, R_L = 10 kΩ, A_V = 1	9.9 MHz
Phase margin	86 Degrees
Settling time, A_V = 10, V_{IN} = 10 V_{PP}, 0.1%	4 μs
Current noise density	0.55 pA/ $\sqrt{Hz}$

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rad(Si)/s)	100 krad (Si) 4/
Single event phenomenon (SEP):	
No Single event latchup (SEL) occurs at effective LET with V_S = ±15 V	≤ 50 MeV/(cm^2/mg) 5/ 6/

4/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

5/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics but are not production tested unless specified by the customer through the purchase order or contract.

6/ Manufacturer performed heavy ion SEL test at the RADEF, University of Jyvaskyla, Finland test lab with Krypton (Kr) ion beam at effective LET ≤ 50 MeV/(cm^2/mg) with supply voltage V_S = ±15 V at 125°C and observed no SEL. However, this device observed single event latch up (SEL) while using Xenon (Xe) ion beam at effective LET ≤ 60 MeV/(cm^2/mg) with supply voltage V_S = ± 15 V at 125°C. Manufacturer also tested SEL test using Xenon (Xe) ion beam with supply voltage V_S = ± 5 V and observed no SEL at effective LET ≤ 80 MeV/(cm^2/mg) at 125°C. See manufacturer's SEE test report for more information.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $V_S = \pm 1.5$ V, $V_{CM} = 0$ V, $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input characteristics.								
Offset voltage	V_{OS}			1	01	-100	100	µV
				2,3		-200	200	
			P,L,R	1		-100	100	
Offset voltage drift	$\Delta V_{OS}/\Delta T$			2,3	01	-1.75	1.75	µV/° C
Offset voltage matching		Worst case channel to channel		1,2,3	01	-150	150	µV
			P,L,R	1	150	-150	150	
Input bias current	I_{IB}			1	01	-300	300	nA
				2,3		-450	450	
			P,L,R	1		-300	300	
Input offset current	I_{OS}			1	01	-25	25	nA
				2,3		-50	50	
			P,L,R	1		-25	25	
Input voltage range	V_{IN}			1,2,3	01	-1.5	+1.5	V
			P,L,R	1		-1.5	+1.5	
Common mode rejection ratio	CMRR	$V_{CM} = \pm 1.5$ V		1	01	64		dB
				2,3		60		
			P,L,R	1		64		
Large signal voltage gain	A_{VO}	-1.3 V $\le V_{OUT} \le +1.3$ V, $R_L = 2$ kΩ		1	01	100		dB
				2		96		
				3		94		
			P,L,R	1		100		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $V_S = \pm 1.5$ V, $V_{CM} = 0$ V, $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output characteristics.								
Output voltage high	V_{OH}	R_L = 10 kΩ to V_{CM}		1,2,3	01	1.4		V
			P,L,R	1		1.4		
		R_L = 2 kΩ to V_{CM}		1,2,3		1.35		
			P,L,R	1		1.35		
Output voltage low	V_{OL}	R_L = 10 kΩ to V_{CM}		1,2,3	01		-1.45	V
			P,L,R	1			-1.45	
		R_L = 2 kΩ to V_{CM}		1			-1.4	
				2,3			-1.35	
			P,L,R	1			-1.4	
Short circuit current	I_{SC} source			1,2,3	01	-19		mA
			P,L,R	1		-19		
	I_{SC} sink			1,2,3			+20	
			P,L,R	1			+20	
Power supply								
Power supply rejection ratio	PSRR	$V_S = \pm 1.25$ V to ± 1.75 V		1	01	85		dB
				2		75		
				3		65		
			P,L,R	1		85		
Supply current all four amplifiers	I_S	I_{OUT} = 0 mA		1	01		±2700	μA
				2,3			±3800	
			P,L,R	1			±2700	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $V_S = \pm 1.5$ V, $V_{CM} = 0$ V $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance							
Slew rate 3/	SR	$R_L = 2$ kΩ	4	01	1.7		V/μs
			5		2		
			6		1.3		
Gain bandwidth product 3/	GBWP	$V_{IN} = 5$ mV_{PP}, $R_L = 10$ kΩ, $A_V = 100$	4,5,6	01	14.4		MHz
-3 dB closed loop bandwidth 3/	-3 dB	$A_V = 1$, $V_{IN} = 5$ mV_{PP}	4	01	9.5		MHz
			5		12		
			6		5.8		
Noise performance							
Voltage noise 3/	en_{PP}	0.1 Hz to 10 Hz	4	01		0.2	μV_{PP}
			5,6			0.22	
Voltage noise density 3/	e_n	f = 10 kHz	4	01		4.2	nV / $\sqrt{Hz}$
			5			5	
			6			4	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $V_S = \pm 5.0$ V, $V_{CM} = 0$ V $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input characteristics.								
Offset voltage	V_{OS}			1	01	-100	100	µV
				2,3		-200	200	
			P,L,R	1		-100	100	
Offset voltage drift	$\Delta V_{OS}/\Delta T$			2,3	01	-1.75	1.75	µV/° C
Offset voltage matching		Worst case channel to channel		1,2,3	01	-150	150	µV
			P,L,R	1		-150	150	
Input bias current	I_{IB}			1	01	-300	300	nA
				2,3		-450	450	
			P,L,R	1		-300	300	
Input offset current	I_{OS}			1	01	-25	25	nA
				2,3		-50	50	
			P,L,R	1		-25	25	
Input voltage range	V_{IN}			1,2,3	01	-5	5	V
			P,L,R	1		-5	5	
Common mode rejection ratio	CMRR	$V_{CM} = \pm 4$ V		1,2	01	98		dB
				3		88		
			P,L,R	1		98		
		$V_{CM} = \pm 5$ V		1,2,3		76		
			P,L,R	1		76		
Large signal voltage gain	A_{VO}	$-4 V \le V_{OUT} \le 4$ V,		1	01	108		dB
		$R_L = 2$ kΩ		2		103		
				3		96		
			P,L,R	1		108		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $V_S = \pm 5.0$ V, $V_{CM} = 0$ V, $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output characteristics.								
Output voltage high	V_{OH}	$R_L = 10\ k\Omega$ to V_{CM}		1	01	4.9		V
				2,3		4.8		
			P,L,R	1		4.9		
		$R_L = 2\ k\Omega$ to V_{CM}		1		4.8		
				2,3		4.7		
			P,L,R	1		4.8		
Output voltage low	V_{OL}	$R_L = 10\ k\Omega$ to V_{CM}		1	01		-4.9	V
				2,3			-4.8	
			P,L,R	1			-4.9	
		$R_L = 2\ k\Omega$ to V_{CM}		1			-4.8	
				2,3			-4.7	
			P,L,R	1			-4.8	
Short circuit current	I_{SC} source			1,2,3	01	-36		mA
			P,L,R	1		-36		
	I_{SC} sink			1,2,3			+35	
			P,L,R	1			+35	
Power supply								
Power supply rejection ratio	PSRR	$V_S = \pm 2$ V to ± 18 V		1	01	110		dB
				2,3		105		
			P,L,R	1		110		
Supply current all four amplifiers	I_S	$I_{OUT} = 0$ mA		1	01		± 2800	µA
				2,3			± 4000	
			P,L,R	1			± 2800	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $V_S = \pm 5.0$ V, $V_{CM} = 0$ V $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance							
Slew rate 3/	SR	R_L = 2 kΩ to V_{CM}	4	01	1.8		V/µs
			5		2.4		
			6		1.4		
Gain bandwidth product 3/	GBWP	V_{IN} = 5 mV_{PP}, R_L = 10 kΩ, A_V = 100	4,5,6	01	14.9		MHz
-3 dB closed loop bandwidth 3/	-3 dB	A_V = 1, V_{IN} = 5 mV_{PP}	4	01	11		MHz
			5		12.9		
			6		5.2		
Noise performance							
Voltage noise 3/	en_{PP}	0.1 Hz to 10 Hz	4	01		0.2	μV_{PP}
			5,6			0.22	
Voltage noise density 3/	e_n	f = 10 kHz	4	01		4.5	nV / $\sqrt{Hz}$
			5			5.1	
			6			4.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $V_S = \pm 15.0$ V, $V_{CM} = 0$ V, $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input characteristics.								
Offset voltage	V_{OS}			1	01	-100	100	µV
				2,3		-200	200	
			P,L,R	1		-100	100	
Offset voltage drift	$\Delta V_{OS}/\Delta T$			2,3	01	-1.75	1.75	µV/° C
Offset voltage matching		Worst case channel to channel		1	01	-150	150	µV
			P,L,R	1		-150	150	
Input bias current	I_{IB}			1	01	-300	300	nA
				2,3		-450	450	
			P,L,R	1		-300	300	
Input offset current	I_{OS}			1	01	-25	25	nA
				2,3		-50	50	
			P,L,R	1		-25	25	
Input voltage range	V_{IN}			1,2,3	01	-15	15	V
			P,L,R	1		-15	15	
Common mode rejection ratio	CMRR	$V_{CM} = \pm 14$ V		1,2,3	01	106		dB
			P,L,R	1		106		
		$V_{CM} = \pm 15$ V		1,2,3		85		
			P,L,R	1		85		
Large signal voltage gain	A_{VO}	$-13.5\text{ V} \le V_{OUT} \le +13.5$ V, $R_L = 2\text{ k}\Omega$		1	01	110		dB
				2		105		
				3		100		
			P,L,R	1		110		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $V_S = \pm 15.0$ V, $V_{CM} = 0$ V, $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output characteristics.								
Output voltage high	V_{OH}	$R_L = 10\ k\Omega$ to V_{CM}		1,2,3	01	14.8		V
			P,L,R	1		14.8		
		$R_L = 2\ k\Omega$ to V_{CM}		1,2		14.5		
				3		13.0		
			P,L,R	1		14.5		
Output voltage low	V_{OL}	$R_L = 10\ k\Omega$ to V_{CM}		1	01		-14.9	V
				2,3			-14.8	
			P,L,R	1			-14.9	
		$R_L = 2\ k\Omega$ to V_{CM}		1			-14.8	
				2,3			-14.7	
			P,L,R	1			-14.8	
Short circuit current	I_{SC} source			1,2,3	01	-71		mA
			P,L,R	1		-71		
	I_{SC} sink			1,2,3			+35	
			P,L,R	1			+35	
Power supply								
Power supply rejection ratio	PSRR	$V_S = \pm 2$ V to ± 18 V		1	01	110		dB
				2,3		105		
			P,L,R	1		110		
Supply current all four amplifiers	I_S	$I_{OUT} = 0$ mA		1	01		± 3000	µA
				2,3			± 4200	
			P,L,R	1			± 3000	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $V_S = \pm 15.0$ V, $V_{CM} = 0$ V $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic performance							
Slew rate	SR	$R_L = 2$ kΩ	4	01	1.9		V/μs
			5		2.4		
			6		1.5		
Gain bandwidth product 3/	GBWP	$V_{IN} = 5$ mV$_{PP}$, $R_L = 10$ kΩ, $A_V = 100$	4,5,6	01	14.9		MHz
-3 dB closed loop bandwidth 3/	-3 dB	$A_V = 1$, $V_{IN} = 5$ mV$_{PP}$	4	01	11		MHz
			5		12.9		
			6		6		
Noise performance							
Voltage noise 3/ 4/ 5/	en$_{PP}$	0.1 Hz to 10 Hz	4	01		0.2	μV$_{PP}$
			5,6			0.22	
Voltage noise density 3/	en	f = 1 kHz	4	01		4.5	nV / $\sqrt{Hz}$
			5			5.1	
			6			4.1	

1/ Device type 01 supplied to this drawing has been characterized through all levels P, L, R of irradiation. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

2/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

3/ Parameter is part of device initial characterization which is only repeated after major design and process changes or with subsequent wafer lots. Not tested post irradiation.

4/ Not tested post irradiation.

5/ The test parameter en$_{PP}$ is 100% production tested at $V_S = \pm 15$ V, T_A = ambient temperature.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	SEP 4/	Temperature (T_C)	Bias V_S	Effective linear energy transfer (LET)
01	No Single event latchup (SEL) occurs	125°C	$V_S = \pm 15$ V	≤ 50 MeV/(cm^2/mg)

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.

3/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

4/ Manufacturer performed heavy ion SEL test at the RADEF, University of Jyvaskyla, Finland test lab with Krypton (Kr) ion beam at effective LET ≤ 50 MeV/(cm^2/mg) with supply voltage $V_S = \pm 15$ V at 125°C and observed no SEL. However, this device observed single event latch up (SEL) while using Xenon (Xe) ion beam at effective LET ≤ 60 MeV/(cm^2/mg) with supply voltage $V_S = \pm 15$ V at 125°C. Manufacturer also tested SEL test using Xenon (Xe) ion beam with supply voltage $V_S = \pm 5$ V and observed no SEL at effective LET ≤ 80 MeV/(cm^2/mg) at 125°C. See manufacturer's SEE test report for more information.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	OUTPUT A	Operational amplifier output, amplifier A.
2	-INPUT A	Operational amplifier negative input, amplifier A.
3	+INPUT A	Operational amplifier positive input, amplifier A.
4	$+V_S$	Positive power supply.
5	+INPUT B	Operational amplifier positive input, amplifier B.
6	-INPUT B	Operational amplifier negative input, amplifier B.
7	OUTPUT B	Operational amplifier output, amplifier B.
8	OUTPUT C	Operational amplifier output, amplifier C.
9	-INPUT C	Operational amplifier negative input, amplifier C.
10	+INPUT C	Operational amplifier positive input, amplifier C.
11	$-V_S$	Negative power supply.
12	+INPUT D	Operational amplifier positive input, amplifier D.
13	-INPUT D	Operational amplifier negative input, amplifier D.
14	OUTPUT D	Operational amplifier output, amplifier D.

FIGURE 1. Terminal connections.

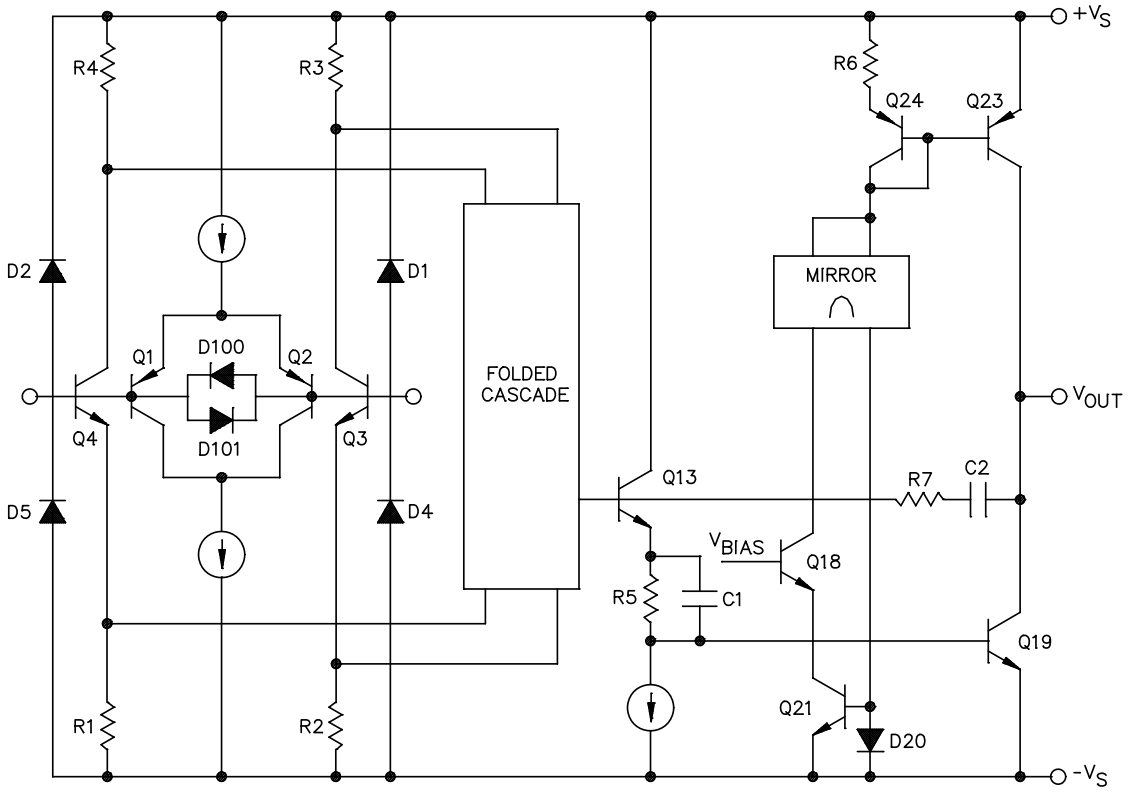


FIGURE 2 Block diagram.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 4, 5, and 6 are tested as part of device initial characterization and after design and process changes or with subsequent wafer lots as indicated in Table IA.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4, 5, 6 1/	1, 2, 3, 4, 5, 6 1/ 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6 2/ 3/
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	1

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters (see Table I).
3/ See table IA for parameters characterized for subgroups 4, 5, and 6.

.

TABLE IIB. Burn-in and operating life test delta parameters. 1/

Parameters	Symbol	Conditions	Device type	Limit	Units
Supply current	I_S	V_S = ±1.5 V	01	±30	µA
		V_S = ±5 V		±30	µA
		V_S = ±15 V		±35	µA
Offset voltage	V_{OS}	V_S = ±1.5 V	01	±15	µV
		V_S = ±5 V		±15	µV
		V_S = ±15 V		±15	µV
Input bias current	I_B	V_S = ±1.5 V	01	±6	nA
		V_S = ±5 V		±6	nA
		V_S = ±15 V		±10	nA

1/ 240 hour burn in and group C end point electrical parameters.
Deltas are performed at T_A = +25°C.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +125°C ±10°C for SEL.

f. Bias conditions shall be V_S = ±15 V or ±5 V for latchup measurements.

g. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Application notes.

6.7.1 Functional description. The device is a precision single supply, rail-to-rail operational amplifier. Intended for portable instrumentation, the device combines the attributes of precision, wide bandwidth, and low noise to make it an ideal choice in single supply applications that require both ac and precision dc performance. Other low supply voltage applications for which the device is well suited are active filters, audio microphone preamplifiers, power supply control, and telecommunications. See manufacturer's datasheet for more application information regarding these specifications.

6.8 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test conditions of SEP.

b. Single event latchup (SEL) occurrence.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-12-14

Approved sources of supply for SMD 5962-15236 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1523601VXA	24355	ADA4084-4AFQMLR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Greensboro, NC 27409-9605