14-Bit, 1300 MSPS, JESD204B, Analog-to-Digital Converter

Preliminary Technical Data

AD9697

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Lane rates up to 16 Gbps
- 1.01 W total power at 1300 MSPS
- SNR = 65.6 dBFS at 172 MHz (1.59 V p-p input range)
- SFDR = 78 dBFS at 172.3 MHz (1.59 V p-p input range)
- Noise density
  - –153.9 dBFS/Hz (1.59 V p-p input range)
  - –155.6 dBFS/Hz (2.04 V p-p input range)
- 0.95 V, 1.8 V, and 2.5 V supply operation
- No missing codes
- Internal ADC voltage reference
- Flexible input range
  - 1.36 V p-p to 2.04 V p-p (1.59 V p-p typical)
- 2 GHz usable analog input full power bandwidth
- Amplitude detect bits for efficient AGC implementation
- 2 integrated digital downconverters per ADC channel
  - 48-bit NCO
  - Programmable decimation rates
- Differential clock input
- SPI control
  - Integer clock divide by 2 and divide by 4
  - Flexible JESD204B lane configurations
- On-chip dithering to improve small signal linearity

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, TD-SCDMA, WCDMA, GSM, LTE
- General-purpose software radios
- Ultrawideband satellite receiver
- Instrumentation
  - Oscilloscopes
  - Spectrum analyzers
  - Network analyzers
  - Integrated RF test solutions
- Radars
- Electronic support measures, electronic counter measures, and electronic counter-counter measures
- High speed data acquisition systems
- DOCSIS 3.0 CMTS upstream receive paths
- Hybrid fiber coaxial digital reverse path receivers
- Wideband digital predistortion

FUNCTIONAL BLOCK DIAGRAM

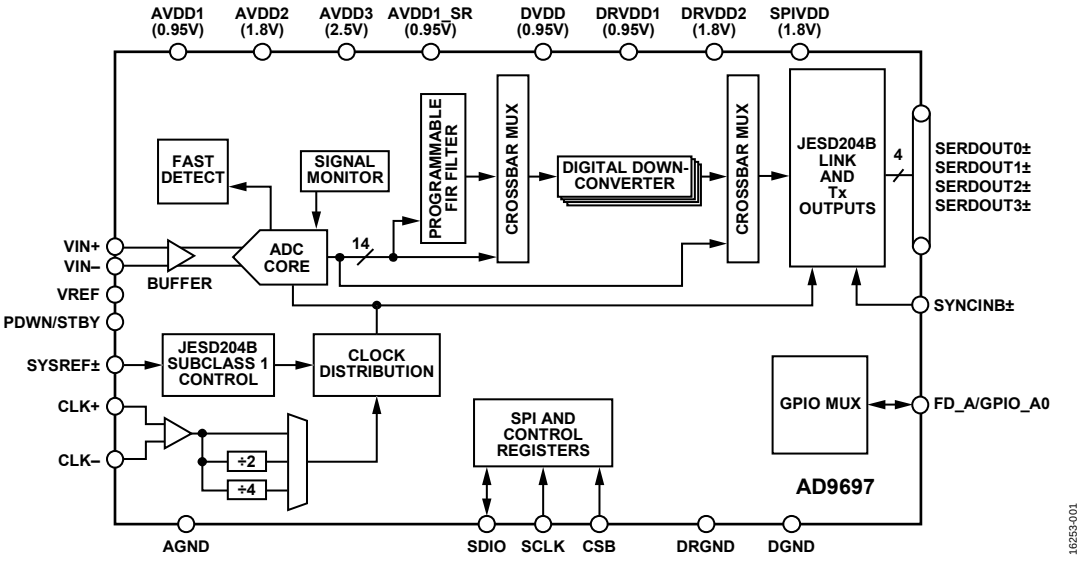

Figure 1.

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REVISION HISTORY

10/2017—Revision PrA: Preliminary Version

GENERAL DESCRIPTION

The AD9697 is a single, 14-bit, 1300 MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of direct sampling wide bandwidth analog signals of up to 2 GHz. The −3 dB bandwidth of the ADC input is 2 GHz. The AD9697 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. The ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four digital downconverters (DDCs) through a crossbar mux. Each DDC consists of multiple signal processing stages: a 48-bit frequency translator (numerically controlled oscillator (NCO)), and decimation filters. The NCO has the option to select up to 16 preset bands over the general-purpose input/output (GPIO) pins, or use a coherent fast frequency hopping mechanism for band selection. Operation of the AD9697 between the DDC modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD9697 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x0245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9697 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

The user can configure the Subclasss 1 JESD204B-based high speed serialized output using either one lane, two lanes, or four lanes, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9697 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 3-wire serial port interface (SPI) and or PDWN/STBY pin.

The AD9697 is available in a Pb-free, 64-lead LFCSP and is specified over the −40°C to +105°C junction temperature range. This product may be protected by one or more U.S. or international patents.

Note that, throughout this data sheet, multifunction pins, such as FD_A/GPIO_A0, are referred to either by the entire pin name or by a single function of the pin, for example, FD_A, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Low power consumption.
2. JESD204B lane rate support up to 16 Gbps.
3. Wide, full power bandwidth supports intermediate frequency (IF) sampling of signals up to 2 GHz.
4. Buffered inputs ease filter design and implementation.
5. Four integrated wideband decimation filters and NCO blocks supporting multiband receivers.
6. Programmable fast overrange detection.
7. On-chip temperature diode for system thermal management.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, 1.7 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, and sample rate = 1300 MSPS unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = TBD°C (T_A = 25°C).

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
ACCURACY				
No Missing Codes		Guaranteed		
Offset Error[1]		5		Codes
Offset Matching	−0.48	0	+0.48	% FSR
Gain Error	−2.9	±1	+2.9	% FSR
Gain Matching	−2.64	±0.18	+2.64	% FSR
Differential Nonlinearity (DNL)	−0.7		0.8	LSB
Integral Nonlinearity (INL)	−7	±1	5	LSB
TEMPERATURE DRIFT				
Offset Error		±9		ppm/°C
Gain Error		69		ppm/°C
INTERNAL VOLTAGE REFERENCE				
Voltage		0.5		V
INPUT-REFERRED NOISE		3.8		LSB rms
ANALOG INPUTS				
Differential Input Voltage Range	1.36	1.59	2.04	V p-p
Common-Mode Voltage (V_{CM})		1.41		V
Differential Input Resistance		200		Ω
Differential Input Capacitance		1.75		pF
Analog Full-Power Bandwidth		2		GHz
POWER SUPPLY				
AVDD1	0.93	0.95	0.98	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
AVDD1_SR	0.93	0.95	0.98	V
DVDD	0.93	0.95	0.98	V
DRVDD1	0.93	0.95	0.98	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD[2]	1.71	1.8	1.89	V
I_{AVDD1}		177	250	mA
I_{AVDD2}		267	306	mA
I_{AVDD3}		29	33	mA
I_{AVDD1_SR}		15	27	mA
I_{DVDD}		121	302	mA
I_{DRVDD1}[3]		124	204	mA
I_{DRVDD2}		21	25	mA
I_{SPIVDD}		2	5	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)[4]		1.01	1.39	W
Power-Down Dissipation		TBD		mW
Standby[5]		TBD		mW

[1] DC offset calibration on (Register 0x0701, Bit 7 = 1 and Register 0x073B, Bit 7 = 0).
[2] The voltage level on the SPIVDD rail and on the DRVDD2 rail must be the same.
[3] All lanes running. Power dissipation on DRVDD changes with lane rate and number of lanes used.
[4] Default mode. No DDCs used.
[5] Can be controlled by SPI.

AC SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, 1.7 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, and sample rate = 1300 MSPS unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = TBD°C (T_A = 25°C).

Table 2.

	Analog Input Full Scale = 1.36 V p-p			Analog Input Full Scale = 1.59 V p-p			Analog Input Full Scale = 2.04 V p-p			
Parameter[1]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE		1.36			1.59			2.04		V p-p
NOISE DENSITY[2]		−152.6			−153.9			−155.6		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)										
f_{IN} = 10.3 MHz		64.4			65.7			67.5		dBFS
f_{IN} = 172.3 MHz		64.4		64.5	65.6			67.5		dBFS
f_{IN} = 340 MHz		64.3			65.6			67.3		dBFS
f_{IN} = 750 MHz		64.0			65.2			66.6		dBFS
f_{IN} = 1000 MHz		63.8			64.9			66.1		dBFS
f_{IN} = 1400 MHz		63.2			64.2			65.2		dBFS
f_{IN} = 1700 MHz		62.7			63.6			64.5		dBFS
f_{IN} = 1980 MHz		62.3			63.0			63.9		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)										
f_{IN} = 10.3 MHz		64.3			65.4			66.1		dBFS
f_{IN} = 172.3 MHz		64.3		64.3	65.4			66.2		dBFS
f_{IN} = 340 MHz		64.2			65.3			65.7		dBFS
f_{IN} = 750 MHz		63.9			65.0			65.5		dBFS
f_{IN} = 1000 MHz		63.6			64.7			65.7		dBFS
f_{IN} = 1400 MHz		63.1			63.8			62.9		dBFS
f_{IN} = 1700 MHz		62.6			63.4			64.2		dBFS
f_{IN} = 1980 MHz		62.1			62.8			61.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)										
f_{IN} = 10.3 MHz		10.3			10.5			10.6		Bits
f_{IN} = 172.3 MHz		10.3		10.3	10.5			10.7		Bits
f_{IN} = 340 MHz		10.3			10.5			10.6		Bits
f_{IN} = 750 MHz		10.3			10.5			10.5		Bits
f_{IN} = 1000 MHz		10.2			10.4			10.6		dBFS
f_{IN} = 1400 MHz		10.1			10.3			10.1		dBFS
f_{IN} = 1700 MHz		10.1			10.2			10.3		dBFS
f_{IN} = 1980 MHz		10.0			10.1			9.9		dBFS
SPURIOUS FREE DYNAMIC RANGE (SFDR)										
f_{IN} = 10.3 MHz		81			79			73		dBFS
f_{IN} = 172.3MHz		81		74	78			72		dBFS
f_{IN} = 340 MHz		80			77			71		dBFS
f_{IN} = 750 MHz		83			80			72		dBFS
f_{IN} = 1000 MHz		82			81			79		dBFS
f_{IN} = 1400 MHz		80			76			67		dBFS
f_{IN} = 1700 MHz		80			80			78		dBFS
f_{IN} = 1980 MHz		81			79			68		dBFS

Parameter[1]	Analog Input Full Scale = 1.36 V p-p			Analog Input Full Scale = 1.59 V p-p			Analog Input Full Scale = 2.04 V p-p			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
WORST OTHER, EXCLUDING 2ND OR 3RD HARMONIC										
f_{IN} = 10.3 MHz		−96			−94			−101		dBFS
f_{IN} = 172.3 MHz		−95			−96	−85		−95		dBFS
f_{IN} = 340 MHz		−98			−99			−98		dBFS
f_{IN} = 750 MHz		−95			−95			−92		dBFS
f_{IN} = 1000 MHz		−96			−93			−91		dBFS
f_{IN} = 1400 MHz		−90			−89			−86		dBFS
f_{IN} = 1700 MHz		−91			−90			−84		dBFS
f_{IN} = 1980 MHz		−90			−90			−77		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), AIN1 AND AIN2 = −7.0 dBFS										
f_{IN1} = 170.8 MHz, f_{IN2} = 173.8 MHz		−84			−84			−83		dBFS
f_{IN1} = 343.5 MHz, f_{IN2} = 346.5 MHz		−83			−82			−81		dBFS
CROSSTALK[3]		>95			>95			>95		dB
Overrange Condition[4]		>95			>95			>95		dB
ANALOG INPUT BANDWIDTH, FULL POWER[5]		2			2			2		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (10 MHz).
[3] Crosstalk is measured at 10 MHz with a −1.0 dBFS analog input on one channel, and no input on the adjacent channel.
[4] The overrange condition is specified with 3 dB of the full-scale input range.
[5] Full power bandwidth is the bandwidth of operation to achieve proper ADC performance.

DIGITAL SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, 1.7 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, and sample rate = 1300 MSPS, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = TBD°C (T_A = 25°C).

Table 3.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1600	mV p-p
Input Common-Mode Voltage		0.65		V
Input Resistance (Differential)		32		kΩ
Input Capacitance (Differential)			0.9	pF
SYSREF INPUTS (SYSREF+, SYSREF−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.65	2	V
Input Resistance (Differential)		18		kΩ
Input Capacitance (Differential)		1		pF
LOGIC INPUTS (SDIO, SCLK, CSB, PDWN/STBY, FD_A/GPIO_A0, FD_B/GPIO_B0)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		30		kΩ

Parameter	Min	Typ	Max	Unit
LOGIC OUTPUT (SDIO, FD_A, FD_B)				
Logic Compliance		CMOS		
Logic 1 Voltage (I_{OH} = 4 mA)	0.65 × SPIVDD			V
Logic 0 Voltage (I_{OL} = 4 mA)	0		0.35 × SPIVDD	V
SYNCIN INPUTS (SYNCINB−, SYNCINB+)				
Logic Compliance		LVDS/LVPECL/CMOS		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.65	2	V
Input Resistance (Differential)		18		kΩ
Input Capacitance (Single-Ended per Pin)		1		pF
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3)				
Logic Compliance		SST		
Differential Output Voltage	360	520	770	mV p-p
Differential Termination Impedance	80	100	1200	Ω

SWITCHING SPECIFICATIONS

AVDD1 = 0.95 V, AVDD1_SR = 0.95 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.95 V, DRVDD1 = 0.95 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, clock divider = 2, 1.7 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, and sample rate = 1300 MSPS, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = TBD°C (T_A = 25°C).

Table 4.

Parameter	Min	Typ	Max	Unit
CLOCK				
Clock Rate (at CLK+/CLK− Pins)	0.24		1.28	GHz
Maximum Sample Rate[1]	TBD			MSPS
Minimum Sample Rate	240[2]			MSPS
Clock Pulse Width[3]				
High	156.25			ps
Low	156.25			ps
OUTPUT PARAMETERS				
Unit Interval (UI)[4]	62.5	76.9		ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		28		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		28		ps
Phase-Locked Loop (PLL) Lock Time		5		ms
Data Rate per Channel (NRZ)[5]	1.6875	13	16	Gbps
LATENCY[6]				
Pipeline Latency		56		Clock cycles
Fast Detect Latency		26		Clock cycles
Wake-Up Time[7]				
Standby		400		µs
Power-Down		15		ms
APERTURE				
Aperture Delay (t_A)		TBD		ps
Aperture Uncertainty (Jitter, t_J)		TBD		fs rms
Out of Range Recovery Time		1		Clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 240 MSPS. See SPI Register 0x011A to reduce the threshold of the clock detect circuit.
[3] Clock duty stabilizer (DCS) on. See SPI Register 0x011C and Register 0x011E to enable DCS.
[4] Baud rate = 1/UI. A subset of this range can be supported.
[5] Default L = 4. This number can change based on the sample rate and decimation ratio.
[6] No DDCs used. L = 4, M = 2, and F = 1.
[7] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 3				
t_{SU_SR}	Device clock to SYSREF+ setup time		−70		ps
t_{H_SR}	Device clock to SYSREF+ hold time		120		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

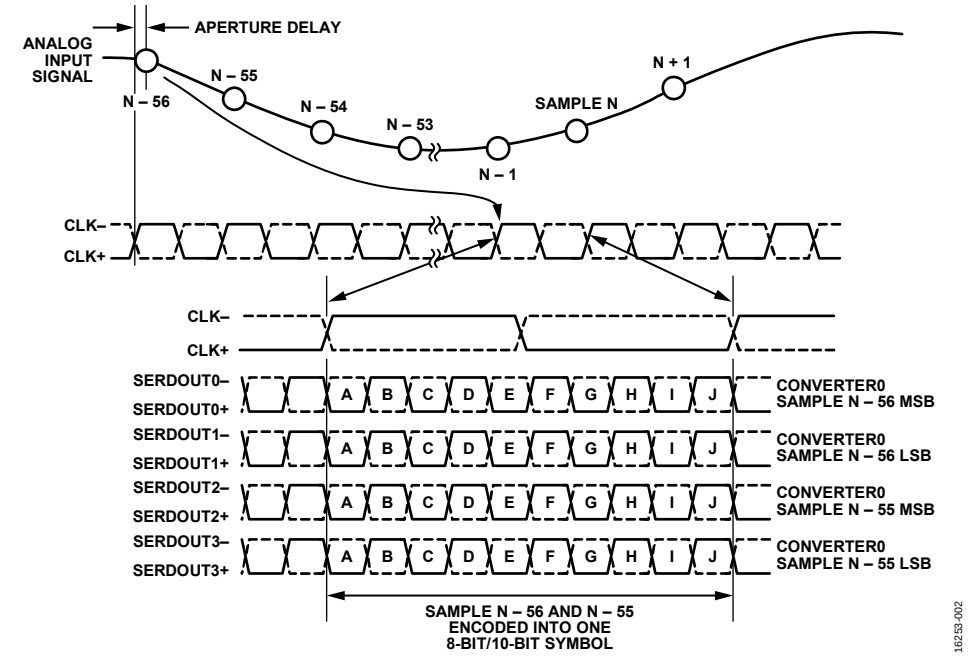


Figure 2. Data Output Timing Diagram

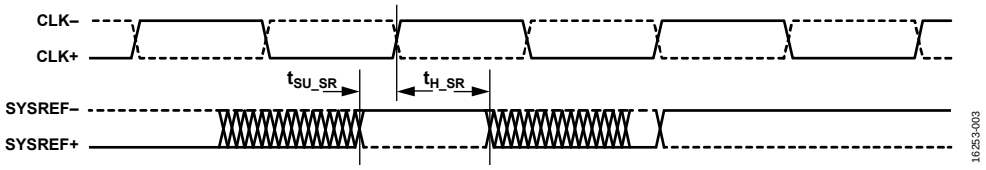


Figure 3. SYSREF± Setup and Hold Timing Diagram

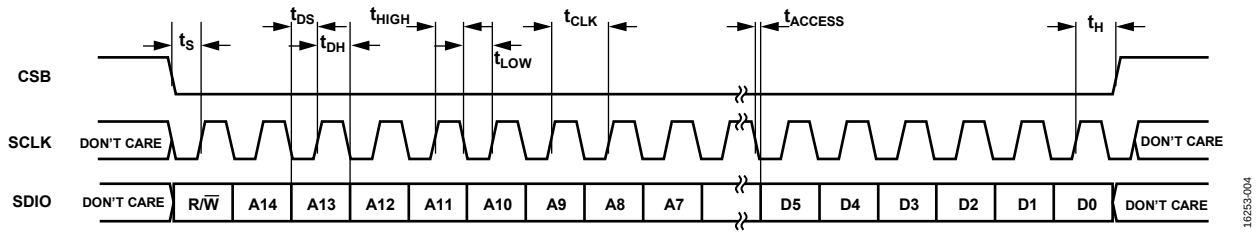


Figure 4. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.00 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.00 V
SPIVDD to DGND	2.00 V
AGND to DRGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
DGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	AGND − 0.3 V to AVDD3 + 0.3 V
CLK± to AGND	AGND − 0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND	2.5 V
SYNCINB± to DRGND	2.5 V
Junction Temperature Range (T_J)	−40°C to +125°C
Storage Temperature Range, Ambient (T_A)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified vs. the number of printed circuit board (PCB) layers in different airflow velocities (in m/sec). Airflow increases heat dissipation effectively reducing θ_{JA} and θ_{JB}. In addition, metal in direct contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes, reduces θ_{JA}. Thermal performance for actual applications requires careful inspection of the conditions in an application. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 6.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC_BOT}[1,3]	θ_{JC_TOP}[1,3]	θ_{JB}[1,4]	θ_{JT}[1,2]	Unit
CP-64-17	0	22.5	1.7	7.6	4.3	0.2	°C/W
	1.0	17.9					°C/W
	2.5	16.8					°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

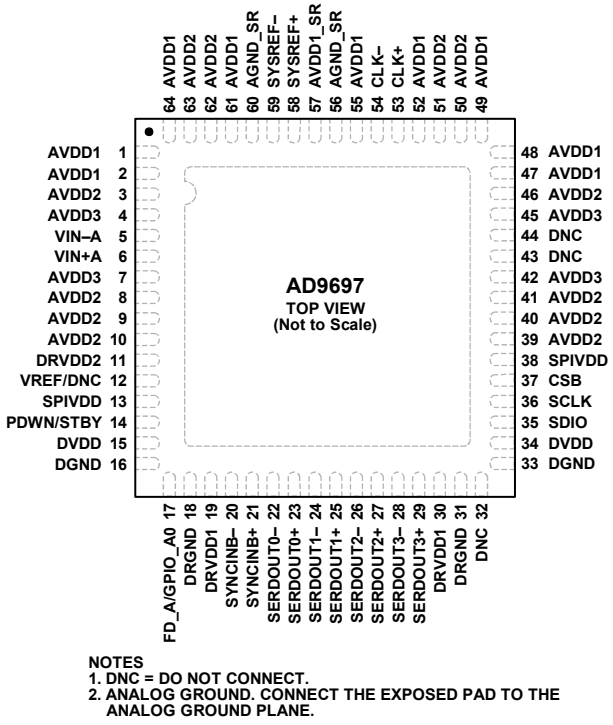


Figure 5. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 2, 47 to 49, 52, 55, 61, 64	AVDD1	Power supply	Analog Power Supply (0.95 V Nominal).
3, 8, 9, 10, 39 to 41, 46, 50, 51, 62, 63	AVDD2	Power supply	Analog Power Supply (1.8 V Nominal).
4, 7, 42, 45	AVDD3	Power supply	Analog Power Supply (2.5 V Nominal).
5, 6	VIN–A, VIN+A	Analog input	ADC A Analog Input Complement/True.
11	DRVDD2	Power supply	Digital Driver Power Supply (1.8 V Nominal).
12	VREF	Input/do not connect	Reference Voltage Input (0.50 V)/Do Not Connect. This pin is configurable through the SPI as a no connect or as an input. Do not connect this pin if using the internal reference. This pin requires a 0.50 V reference voltage input if using an external voltage reference source.
13, 38	SPIVDD	Power supply	Digital Power Supply for SPI (1.8 V Nominal).
14	PDWN/STBY	Digital control input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
15, 34	DVDD	Power supply	Digital Power Supply (0.95 V Nominal).
16, 33	DGND	Ground power supply	Digital Control Ground Supply. These pins connect to the digital ground plane.
17	FD_A/GPIO_A0	CMOS output	Fast Detect Outputs for Channel A. General-purpose Input/Output (GPIO) Pin A0.
18, 31	DRGND	Ground power supply	Digital Driver Ground Supply. This pin connects to the digital driver ground plane.
19, 30	DRVDD1	Power supply	Digital Driver Power Supply (0.95 V Nominal).
20, 21	SYNCINB–, SYNCINB+	Digital input	Active Low JESD204B LVDS Sync Input True/Complement.
22, 23	SERDOUT0–, SERDOUT0+	Data output	Lane 0 Output Data Complement/True.
24, 25	SERDOUT1–, SERDOUT1+	Data output	Lane1 Output Data Complement/True.

Pin No.	Mnemonic	Type	Description
26, 27	SERDOUT2− SERDOUT2+	Data output	Lane 2 Output Data Complement/True.
28, 29	SERDOUT3−, SERDOUT3+	Data output	Lane 3 Output Data Complement/True.
32	DNC	Do not connect	Do Not Connect.
35	SDIO	Digital control input/output	SPI Serial Data Input/Output.
36	SCLK	Digital control input	SPI Serial Clock.
37	CSB	Digital control input	SPI Chip Select (Active Low).
43, 44	DNC	Do not connect	Do Not Connect.
53, 54	CLK+, CLK−	Analog input	Clock Input True/Complement.
56, 60	AGND_SR	Ground power supply	Ground Reference for SYSREF±.
57	AVDD1_SR	Power supply	Analog Power Supply for SYSREF± (0.9 V Nominal).
58, 59	SYSREF+, SYSREF−	Digital input	Active High JESD204B LVDS System Reference Input Complement/True.
0	EPAD	Ground power supply	Analog Ground. Connect the exposed pad to the analog ground plane.

EQUIVALENT CIRCUITS

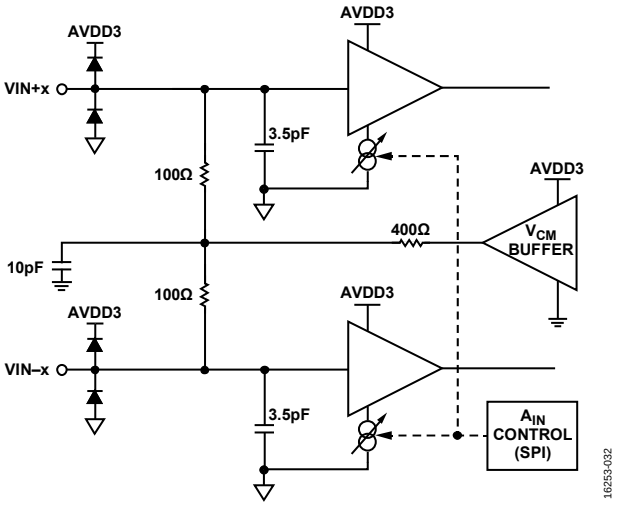


Figure 6. Analog Inputs

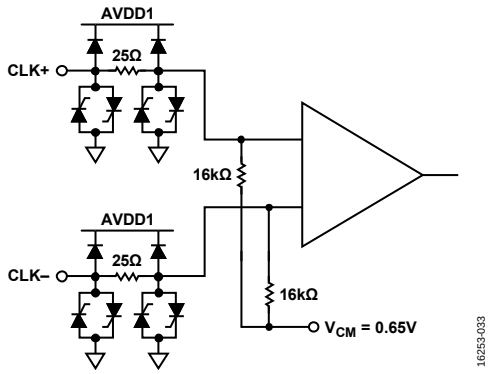


Figure 7. Clock Inputs

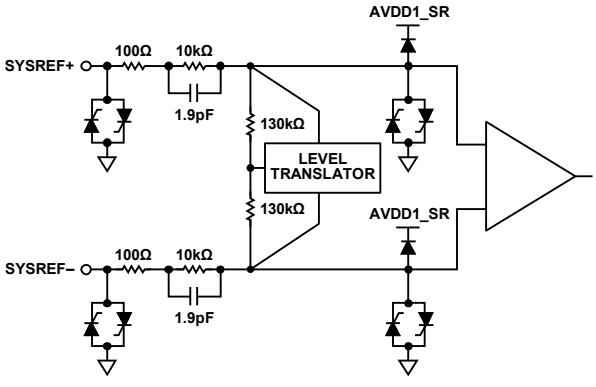


Figure 8. SYSREF± Inputs

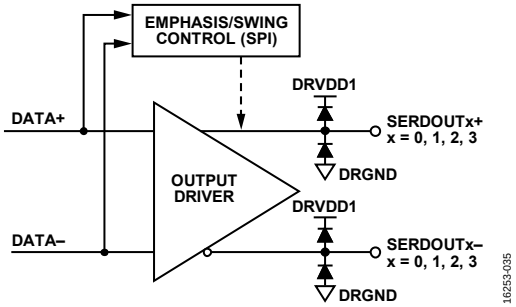


Figure 9. Digital Outputs

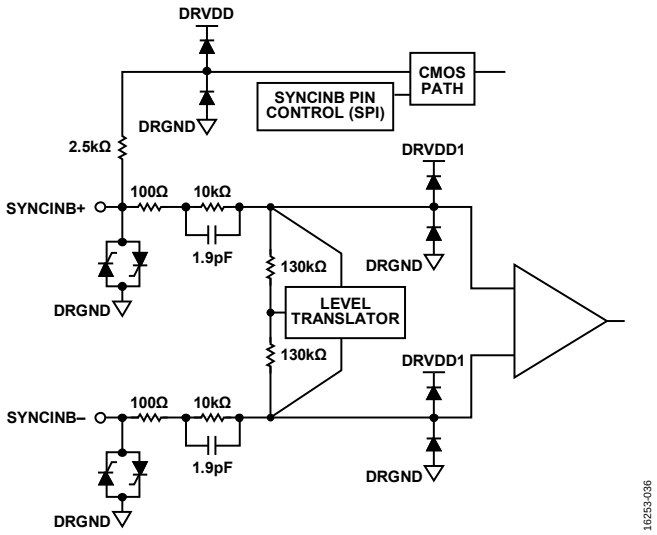


Figure 10. SYNCINB± Inputs

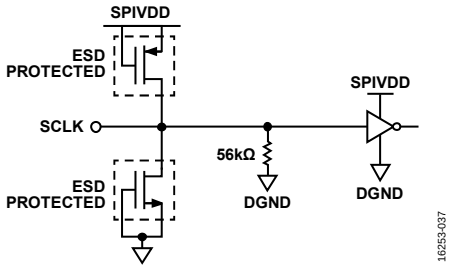


Figure 11. SCLK Input

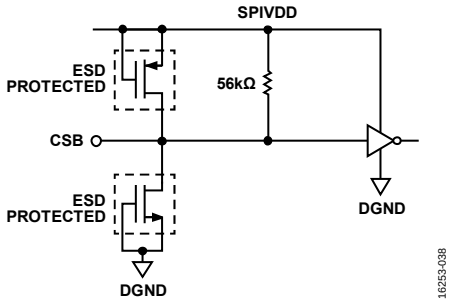


Figure 12. CSB Input

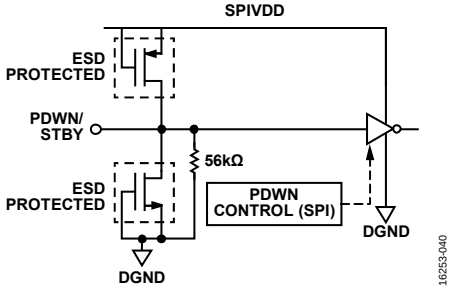


Figure 14. PDWN/STBY Input

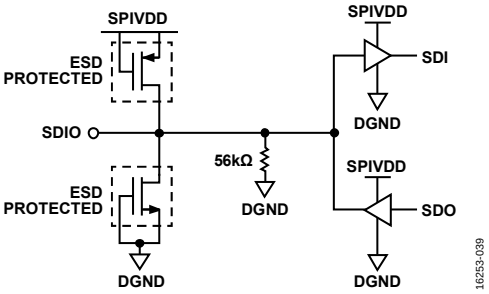


Figure 13. SDIO Input

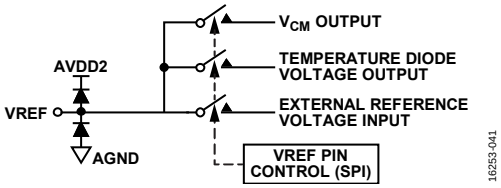


Figure 15. VREF Input/Output

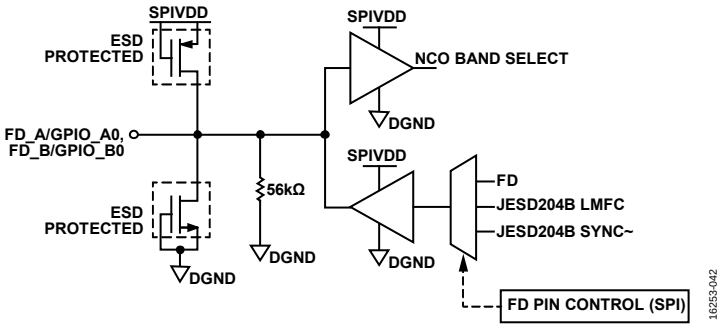
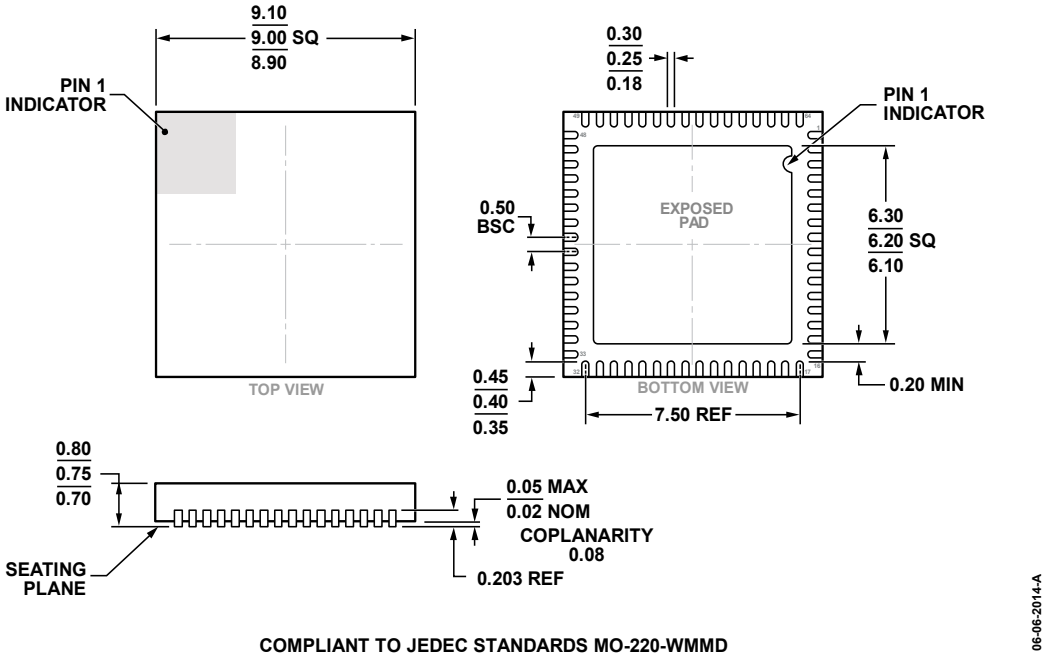


Figure 16. FD_A/GPIO_A0 and FD_B/GPIO_B0

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WMMD

Figure 17. 64-Lead Lead Frame Chip Scale Package [LFCSP]
9 mm × 9 mm Body and 0.75 mm Package Height
(CP-64-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9697BCPZ-1300	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-17
AD9697BCPZRL7-1300	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP]	CP-64-17
AD9695-1300EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

PR16253-0-10/17(PrA)