

FEATURES

Single-ended-to-differential converter

Excellent linearity

Distortion -110 dBc at 100 kHz for V_O , $dm = 2$ V p-p

Low noise: 10.2 nV/ $\sqrt{\text{Hz}}$, output-referred, $G = 2$

Extremely low power: 2.2 mA (3 V supply)

High input impedance: 24 M Ω

User-adjustable gain

High speed: 31 MHz, -3 dB bandwidth ($G = +2$)

Fast settling time: 300 ns to 0.005% for a 2 V step

Low offset: 0.8 mV maximum, output-referred, $G = 2$

Rail-to-rail output

Disable feature

Wide supply voltage range: 2.7 V to 12 V

Available in space-saving, 3 mm $\times$ 3 mm LFCSP

APPLICATIONS

Single-supply data acquisition systems

Instrumentation

Process control

Battery-power systems

Medical instrumentation

GENERAL DESCRIPTION

The [ADA4941-1](#) is a low power, low noise differential driver for analog-to-digital converters (ADCs) up to 18 bits in systems that are sensitive to power. The [ADA4941-1](#) is configured in an easy-to-use, single-ended-to-differential configuration and requires no external components for a gain of 2 configuration. A resistive feedback network can be added to achieve gains greater than 2. The [ADA4941-1](#) provides essential benefits, such as low distortion and high SNR that are required for driving high resolution ADCs.

With a wide input voltage range (0 V to 3.9 V on a single 5 V supply), rail-to-rail output, high input impedance, and a user-adjustable gain, the [ADA4941-1](#) is designed to drive single-supply ADCs with differential inputs found in a variety of low power applications, including battery-operated devices and single-supply data acquisition systems.

The [ADA4941-1](#) is ideal for driving the 16-bit and 18-bit PulSAR[®] ADCs, such as the [AD7687](#), [AD7690](#), and [AD7691](#).

The [ADA4941-1](#) is manufactured on Analog Devices, Inc., proprietary, second-generation, eXtra fast complementary

FUNCTIONAL BLOCK DIAGRAM

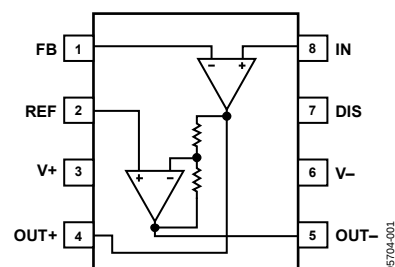


Figure 1.

bipolar (XFCB) process, which enables the amplifier to achieve 18-bit performance on low supply currents.

The [ADA4941-1](#) is available in a small 8-lead LFCSP as well as a standard 8-lead SOIC and is rated to work over the extended industrial temperature range, -40°C to $+125^{\circ}\text{C}$.

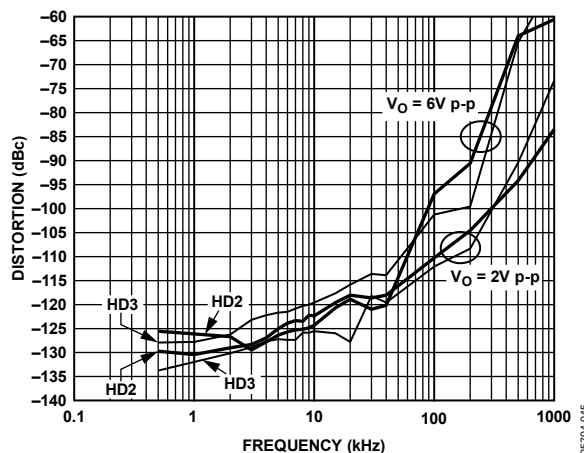


Figure 2. Distortion vs. Frequency at Various Output Amplitudes

Rev. D

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Comparable Parts

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Evaluation Kits

- Universal Evaluation Board for Single Differential Amplifiers

Documentation

Data Sheet

- ADA4941-1: Single-Supply, Differential, 18-Bit ADC Driver Data Sheet

User Guides

- UG-474: Evaluation Board for Differential Amplifiers Offered in 8-Lead SOIC Packages

Tools and Simulations

- ADA4941 SPICE Macro Model

Reference Designs

- CN0032
- CN0033

Reference Materials

Product Selection Guide

- Amplifiers for Video Distribution
- High Speed Amplifiers Selection Table
- SAR ADC & Driver Quick-Match Guide

Technical Articles

- Exploring Different SAR ADC Analog Input Architectures

Tutorials

- MT-218: Multiple Feedback Band-Pass Design Example

Design Resources

- ADA4941-1 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

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REVISION HISTORY

5/16—Rev. C to Rev. D

Change CP-8-2 to CP-8-13.....	Throughout
Changes to Figure 4.....	7
Added Figure 5; Renumbered Sequentially.....	7
Updated Outline Dimensions.....	23
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8/11—Rev. B to Rev. C

Change to Gain Error Drift Unit, Table 1.....	3
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8/10—Rev. A to Rev. B

Added Caption to Figure 1.....	1
Added Exposed Pad Notation to Figure 4 and Table 6.....	7
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3/09—Rev. 0 to Rev. A

Change to Gain Error Drift Parameter, Table 1.....	3
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Updated Outline Dimensions.....	23

4/06—Revision 0: Initial Version

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_S = 3\text{ V}$, OUT+ connected to FB ($G = 2$), $R_{L, dm} = 1\text{ k}\Omega$, REF = 1.5 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$V_O = 0.1\text{ V p-p}$	21	30		MHz
	$V_O = 2.0\text{ V p-p}$	4.6	6.5		MHz
Overdrive Recovery Time	+Recover/–recovery		320/650		ns
Slew Rate	$V_O = 2\text{ V step}$		22		V/ μs
Settling Time 0.005%	$V_O = 2\text{ V p-p step}$		300		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	$f_c = 40\text{ kHz}, V_O = 2\text{ V p-p}, \text{HD2/HD3}$		–116/–112		dBc
	$f_c = 100\text{ kHz}, V_O = 2\text{ V p-p}, \text{HD2/HD3}$		–101/–98		dBc
	$f_c = 1\text{ MHz}, V_O = 2\text{ V p-p}, \text{HD2/HD3}$		–75/–71		dBc
RTO Voltage Noise	$f = 100\text{ kHz}$		10.2		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		1.6		pA/ $\sqrt{\text{Hz}}$
DC PERFORMANCE					
Differential Output Offset Voltage	Amp A1 or Amp A2		0.2	0.8	mV
Differential Input Offset Voltage Drift			1.0		$\mu\text{V}/^\circ\text{C}$
Single-Ended Input Offset Voltage			0.1	0.4	mV
Single-Ended Input Offset Voltage Drift			0.3		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	IN and REF		3	4.5	μA
Input Offset Current	IN and REF		0.1		μA
Gain	$(+OUT - -OUT)/(IN - REF)$	1.98	2.00	2.01	V/V
Gain Error		–1		+1	%
Gain Error Drift			1	5	ppm/ $^\circ\text{C}$
INPUT CHARACTERISTICS					
Input Resistance	IN and REF		24		M Ω
Input Capacitance	IN and REF		1.4		pF
Input Common-Mode Voltage Range		0.2		1.9	V
Common-Mode Rejection Ratio (CMRR)	$\text{CMRR} = V_{OS, dm}/V_{CM}, V_{REF} = V_{IN}, V_{CM} = 0.2\text{ V to }1.9\text{ V}, G = 4$	81	105		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, $G = 4$	± 2.90	± 2.95		V
Output Current			25		mA
Capacitive Load Drive	20% overshoot, $V_{O, dm} = 200\text{ mV p-p}$		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			2.2	2.4	mA
Quiescent Current—Disable			10	16	μA
Power Supply Rejection Ratio (PSRR)					
+PSRR	$\text{PSRR} = V_{OS, dm}/\Delta V_S, G = 4$	86	100		dB
–PSRR		86	110		dB
DISABLE					
DIS Input Voltage	Disabled, DIS = high		≥ 1.5		V
	Enabled, DIS = low		≤ 1.0		V
DIS Input Current	Disabled, DIS = high		5.5	8	μA
	Enabled, DIS = low		4	6	μA
Turn-On Time			0.7		μs
Turn-Off Time			30		μs

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, OUT+ connected to FB ($G = 2$), $R_{L, dm} = 1\text{ k}\Omega$, REF = 2.5 V, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$V_O = 0.1\text{ V p-p}$	22	31		MHz
	$V_O = 2.0\text{ V p-p}$	4.9	7		MHz
Overdrive Recovery Time	+Recover/–recovery		200/600		ns
Slew Rate	$V_O = 2\text{ V step}$		24.5		V/ μs
Settling Time 0.005%	$V_O = 6\text{ V p-p step}$		610		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	$f_c = 40\text{ kHz}, V_O = 2\text{ V p-p}, \text{HD2/HD3}$		–118/–119		dBc
	$f_c = 100\text{ kHz}, V_O = 2\text{ V p-p}, \text{HD2/HD3}$		–110/–112		dBc
	$f_c = 1\text{ MHz}, V_O = 2\text{ V p-p}, \text{HD2/HD3}$		–83/–73		dBc
RTO Voltage Noise	$f = 100\text{ kHz}$		10.2		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		1.6		pA/ $\sqrt{\text{Hz}}$
DC PERFORMANCE					
Differential Output Offset Voltage	Amp A1 or Amp A2		0.2	0.8	mV
Differential Input Offset Voltage Drift			1.0		$\mu\text{V}/^\circ\text{C}$
Single-Ended Input Offset Voltage			0.1	0.4	mV
Single-Ended Input Offset Voltage Drift			0.3		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	IN and REF		3	4.5	μA
Input Offset Current	IN and REF		0.1		μA
Gain	(+OUT – –OUT)/(IN – REF)	1.98	2	2.01	V/V
Gain Error		–1		+1	%
Gain Error Drift			1	5	ppm/ $^\circ\text{C}$
INPUT CHARACTERISTICS					
Input Resistance	IN and REF		24		M Ω
Input Capacitance	IN and REF		1.4		pF
Input Common-Mode Voltage Range		0.2		3.9	V
Common-Mode Rejection Ratio (CMRR)	$\text{CMRR} = V_{OS, dm}/V_{CM, r}$, VREF = VIN, $V_{CM} = 0.2\text{ V to }3.9\text{ V}$, $G = 4$	84	106		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, $G = 4$	± 4.85	± 4.93		V
Output Current			25		mA
Capacitive Load Drive	20% overshoot, $V_{O, dm} = 200\text{ mV p-p}$		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			2.3	2.6	mA
Quiescent Current—Disable			12	20	μA
Power Supply Rejection Ratio (PSRR)					
+PSRR	$\text{PSRR} = V_{OS, dm}/\Delta V_{S, r}$, $G = 4$	87	100		dB
–PSRR		87	110		dB
DISABLE					
DIS Input Voltage	Disabled, DIS = high		≥ 1.5		V
	Enabled, DIS = low		≤ 1.0		V
DIS Input Current	Disabled, DIS = high		5.5	8	μA
	Enabled, DIS = low		4	6	μA
Turn-On Time			0.7		μs
Turn-Off Time			30		μs

$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{ V}$, OUT+ connected to FB ($G = 2$), $R_{L, dm} = 1\text{ k}\Omega$, REF = 0 V, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$V_O = 0.1\text{ V p-p}$	23	32		MHz
	$V_O = 2.0\text{ V p-p}$	5.2	7.5		MHz
Overdrive Recovery Time	+Recover/–recovery		200/650		ns
Slew Rate	$V_O = 2\text{ V step}$		26		V/ μs
Settling Time 0.005%	$V_O = 12\text{ V p-p step}$		980		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	$f_C = 40\text{ kHz}$, $V_O = 2\text{ V p-p}$, HD2/HD3		–118/–119		dBc
	$f_C = 100\text{ kHz}$, $V_O = 2\text{ V p-p}$, HD2/HD3		–109/–112		dBc
	$f_C = 1\text{ MHz}$, $V_O = 2\text{ V p-p}$, HD2/HD3		–84/–75		dBc
RTO Voltage Noise	$f = 100\text{ kHz}$		10.2		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		1.6		pA/ $\sqrt{\text{Hz}}$
DC PERFORMANCE					
Differential Output Offset Voltage	Amp A1 or Amp A2		0.2	0.8	mV
Differential Input Offset Voltage Drift			1.0		$\mu\text{V}/^\circ\text{C}$
Single-Ended Input Offset Voltage			0.1	0.4	mV
Single-Ended Input Offset Voltage Drift			0.3		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	IN and REF		3	4.5	μA
Input Offset Current	IN and REF		0.1		μA
Gain	(+OUT – –OUT)/(IN – REF)	1.98	2	2.01	V/V
Gain Error		–1		+1	%
Gain Error Drift			1	5	ppm/ $^\circ\text{C}$
INPUT CHARACTERISTICS					
Input Resistance	IN and REF		24		M Ω
Input Capacitance	IN and REF		1.4		pF
Input Common-Mode Voltage Range		–4.8		+3.9	V
Common-Mode Rejection Ratio (CMRR)	$\text{CMRR} = V_{OS, dm}/V_{CM}$, $V_{REF} = V_{IN}$, $V_{CM} = -4.8\text{ V to }+3.9\text{ V}$, $G = 4$	85	105		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, $G = 4$	$V_S - 0.25$	$V_S \pm 0.14$		V
Output Current			25		mA
Capacitive Load Drive	20% overshoot, $V_{O, dm} = 200\text{ mV p-p}$		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			2.5	2.7	mA
Quiescent Current—Disable			15	26	μA
Power Supply Rejection Ratio (PSRR)	$\text{PSRR} = V_{OS, dm}/\Delta V_S$, $G = 4$				
+PSRR		87	100		dB
–PSRR		87	110		dB
DISABLE					
DIS Input Voltage	Disabled, DIS = high		≥ -3		V
	Enabled, DIS = low		≤ -4		V
DIS Input Current	Disabled, DIS = high		7	10	μA
	Enabled, DIS = low		4	6	μA
Turn-On Time			0.7		μs
Turn-Off Time			30		μs

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12 V
Power Dissipation	See Figure 3
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad (if applicable) on the PCB surface that is thermally connected to a copper plane, with zero airflow.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC on 4-Layer Board	126	28	°C/W
8-Lead LFCSP with EP on 4-Layer Board	83	19	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the [ADA4941-1](#) package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the [ADA4941-1](#). Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the

quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. The power dissipated due to all of the loads is equal to the sum of the power dissipation due to each individual load. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA} . In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA} . The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a copper plane to achieve the specified θ_{JA} .

Figure 3 shows the maximum safe power dissipation in the packages vs. the ambient temperature for the 8-lead SOIC (126°C/W) and for the 8-lead LFCSP (83°C/W) on a JEDEC standard 4-layer board. The LFCSP must have its underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

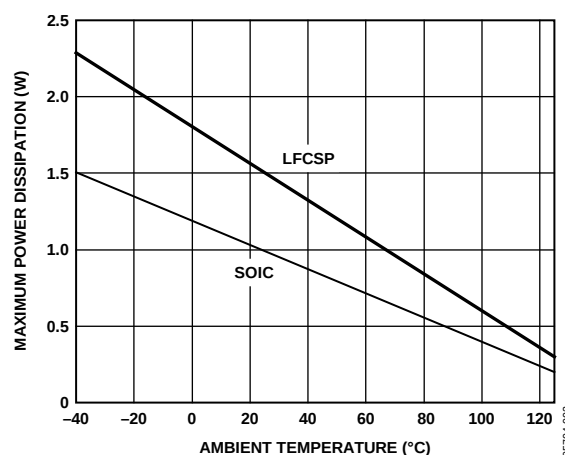


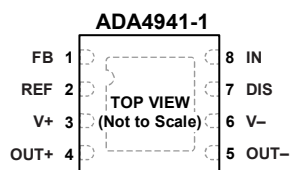
Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

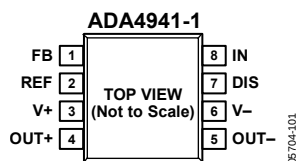


NOTES

1. THE EXPOSED PAD IS NOT ELECTRICALLY CONNECTED TO THE DEVICE. IT IS TYPICALLY SOLDERED TO GROUND OR A POWER PLANE ON THE PCB THAT IS THERMALLY CONDUCTIVE.

05704-1.02

Figure 4. 8-Lead LFCSP Pin Configuration



05704-1.01

Figure 5. 8-Lead SOIC Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB	Feedback Input.
2	REF	Reference Input.
3	V+	Positive Power Supply.
4	OUT+	Noninverting Output.
5	OUT-	Inverting Output.
6	V-	Negative Power Supply.
7	DIS	Disable.
8	IN	Input.
	EPAD (LFCSP Only)	Exposed Paddle. The exposed pad is not electrically connected to the device. It is typically soldered to ground or a power plane on the PCB that is thermally conductive.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, $V_S = 5\text{ V}$, $R_{L, dm} = 1\text{ k}\Omega$, $REF = 2.5\text{ V}$, $DIS = \text{low}$, $OUT+$ directly connected to FB ($G = 2$), $T_A = 25^\circ\text{C}$.

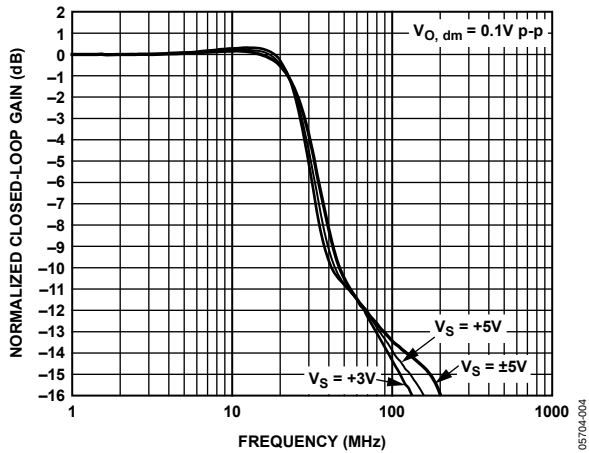


Figure 6. Small Signal Frequency Response for Various Power Supplies

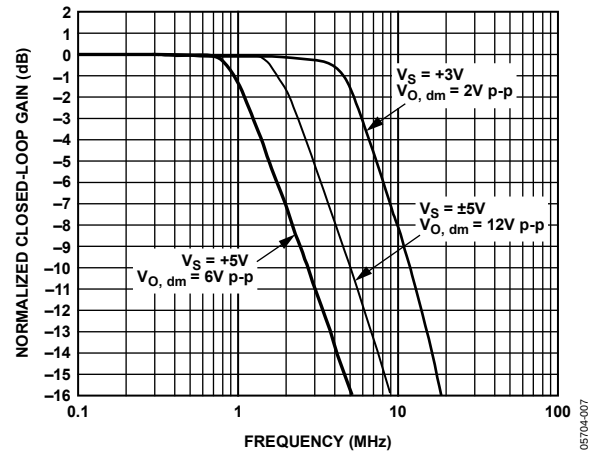


Figure 9. Large Signal Frequency Response for Various Power Supplies

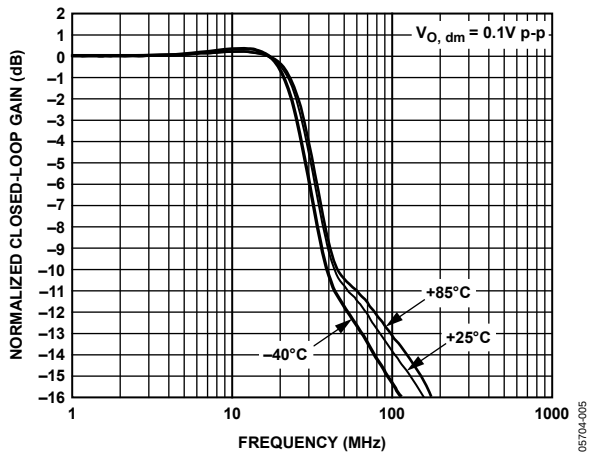


Figure 7. Small Signal Frequency Response at Various Temperatures

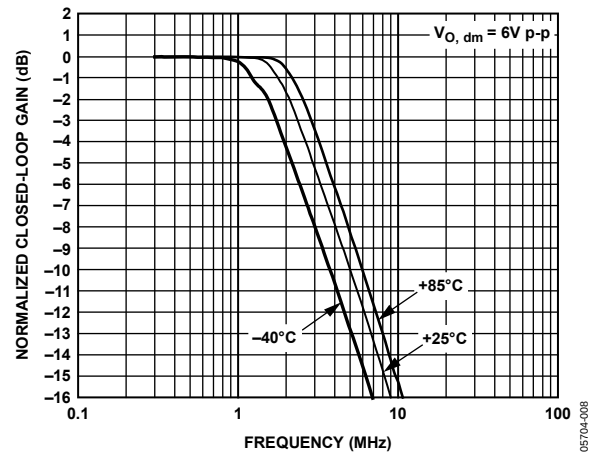


Figure 10. Large Signal Frequency Response at Various Temperatures

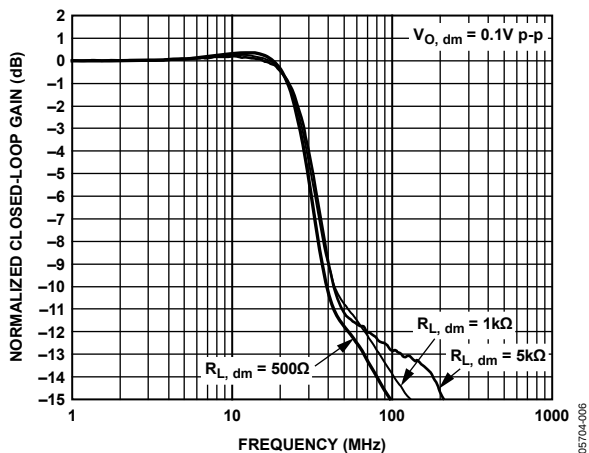


Figure 8. Small Signal Frequency Response for Various Resistive Loads

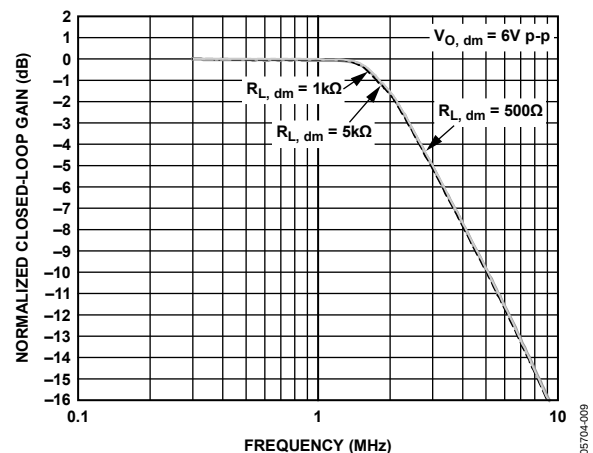


Figure 11. Large Signal Frequency Response for Various Resistive Loads

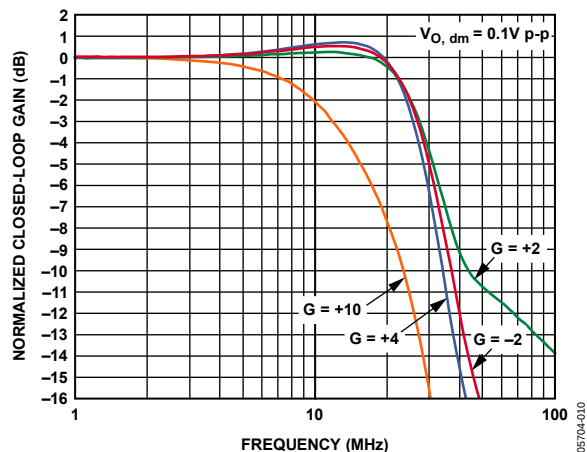


Figure 12. Small Signal Frequency Response for Various Gains

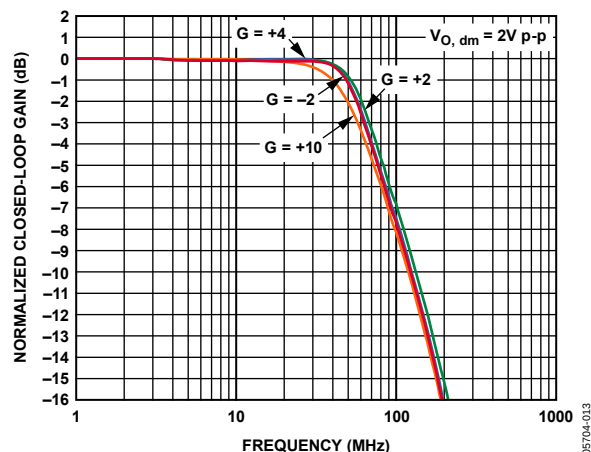


Figure 15. Large Signal Frequency Response for Various Gains

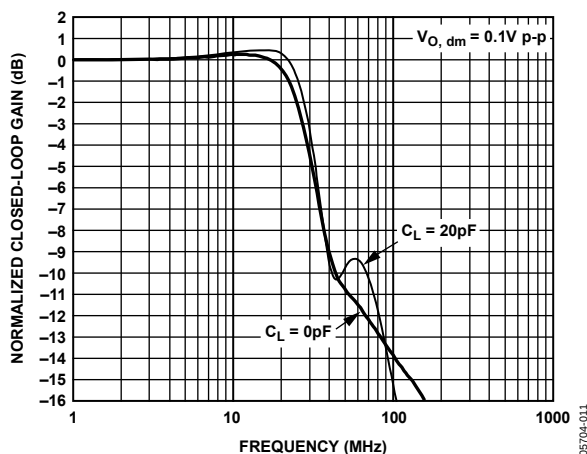


Figure 13. Small Signal Frequency Response for Various Capacitive Loads

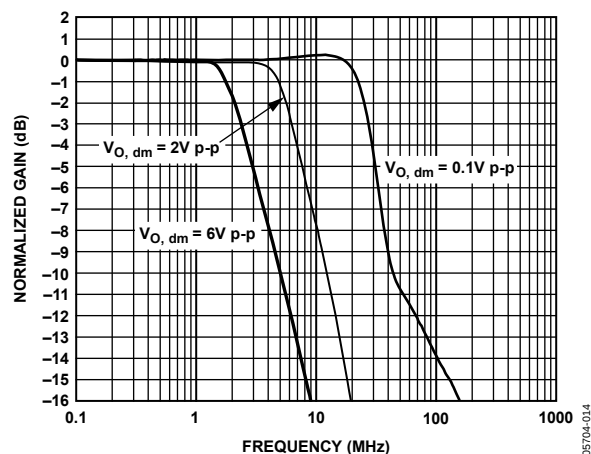


Figure 16. Frequency Response for Various Output Amplitudes

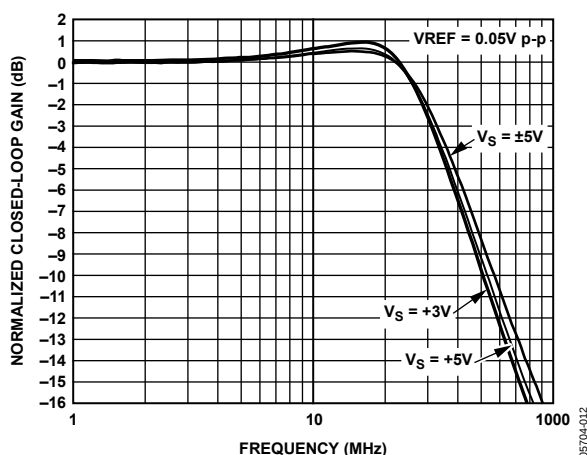


Figure 14. REF Input Small Signal Frequency Response for Various Supplies

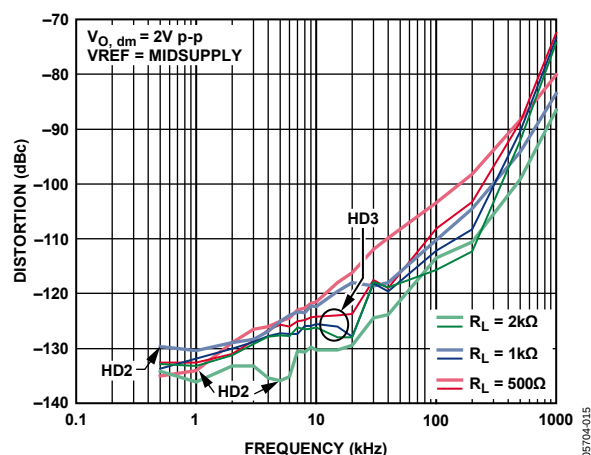


Figure 17. Distortion vs. Frequency for Various Loads

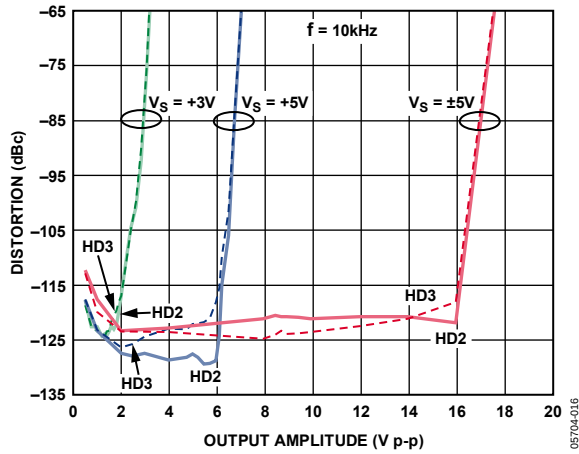


Figure 18. Distortion vs. Output Amplitude for Various Supplies ($G = +2$)

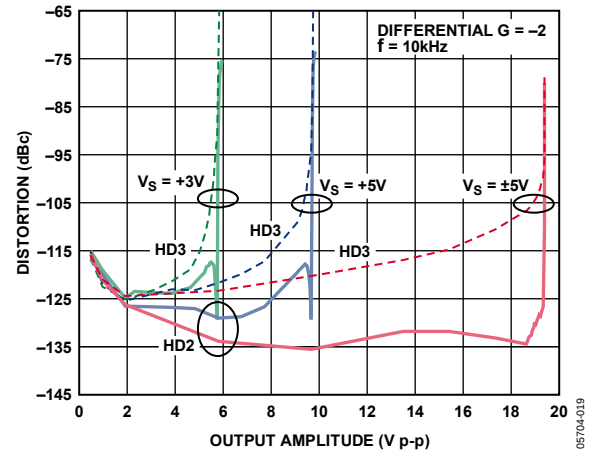


Figure 21. Distortion vs. Output Amplitude for Various Supplies ($G = -2$)

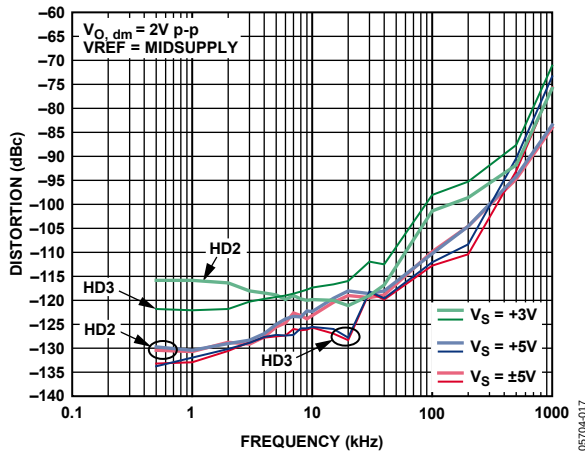


Figure 19. Distortion vs. Frequency for Various Supplies

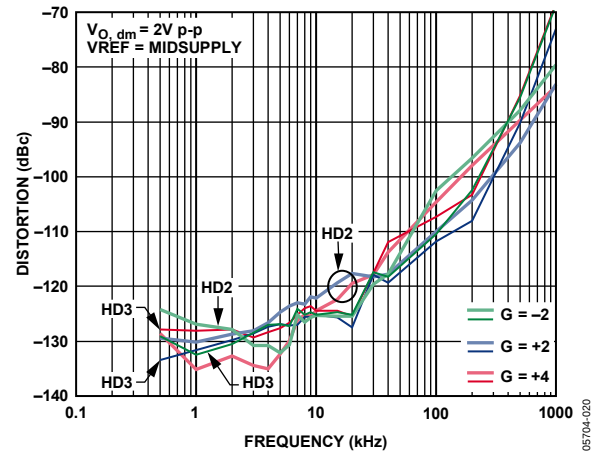


Figure 22. Distortion vs. Frequency for Various Gains

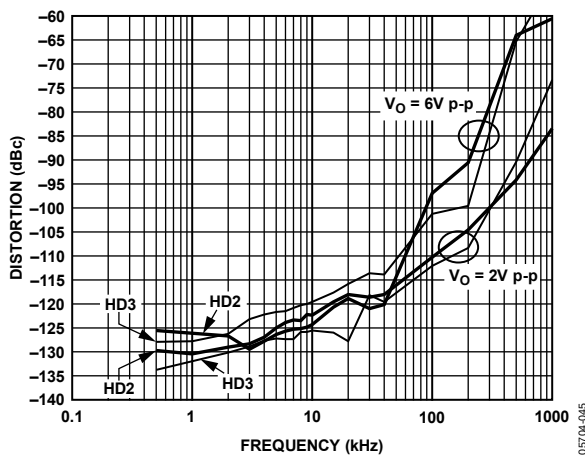


Figure 20. Distortion vs. Frequency at Various Output Amplitudes

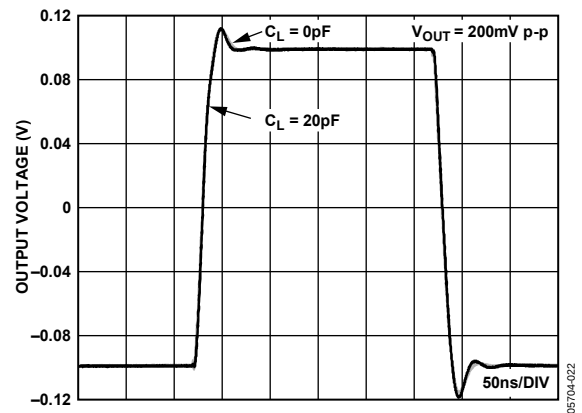


Figure 23. Small Signal Transient Response for Various Capacitive Loads

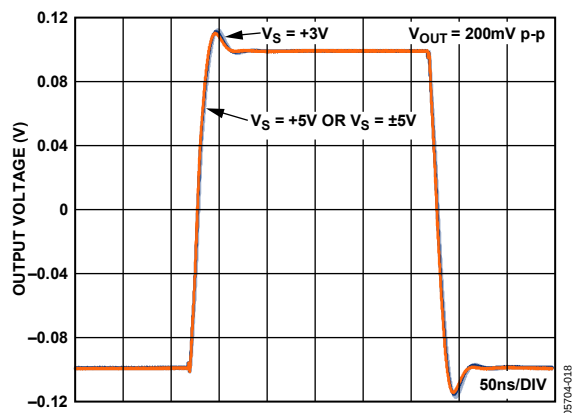


Figure 24. Small Signal Transient Response for Various Supplies

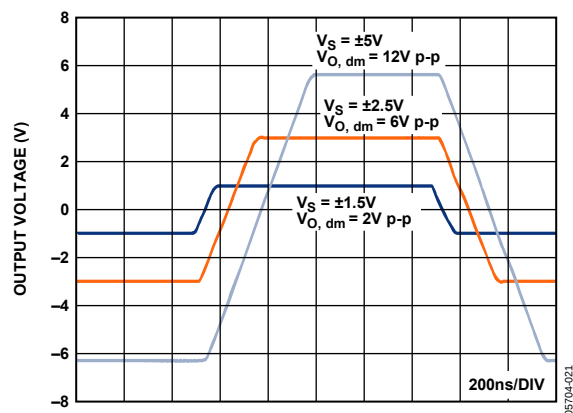
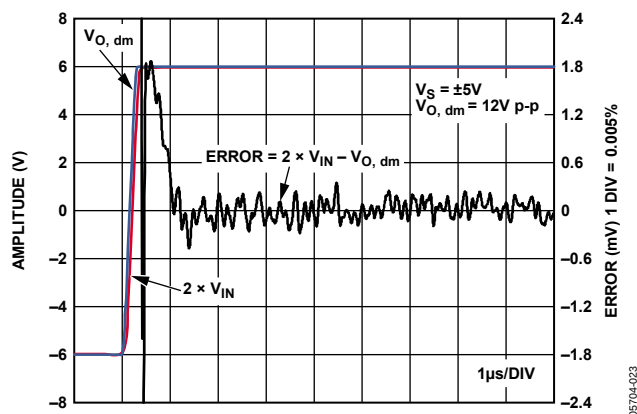
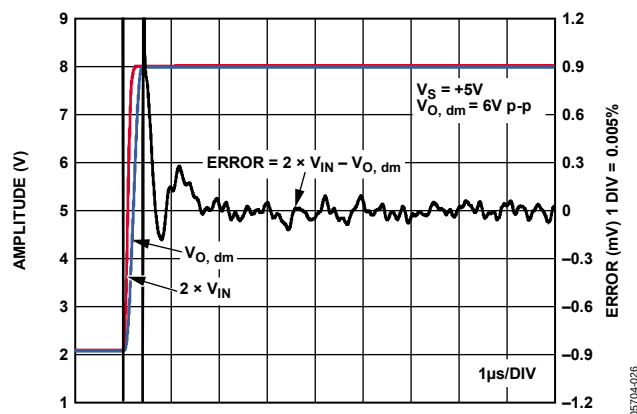
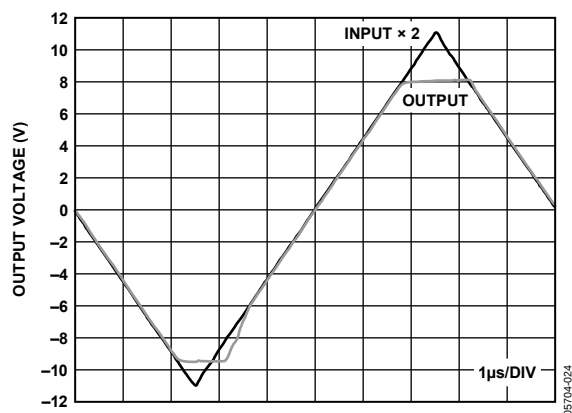
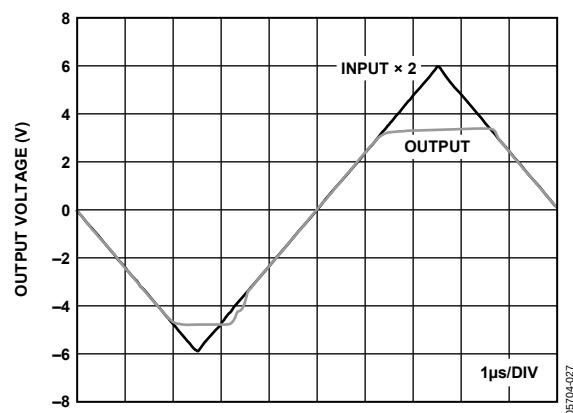


Figure 27. Large Signal Transient Response for Various Supplies

Figure 25. Settling Time (0.005%), $V_S = \pm 5 V$ Figure 28. Settling Time (0.005%), $V_S = +5 V$ Figure 26. Input Overdrive Recovery, $V_S = \pm 5 V$ Figure 29. Input Overdrive Recovery, $V_S = +5 V$

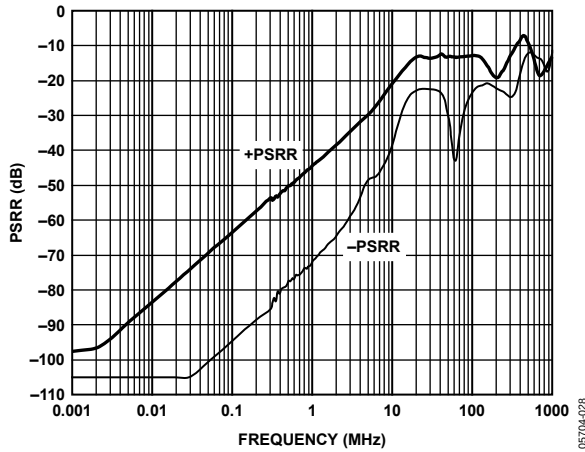


Figure 30. Power Supply Rejection Ratio vs. Frequency

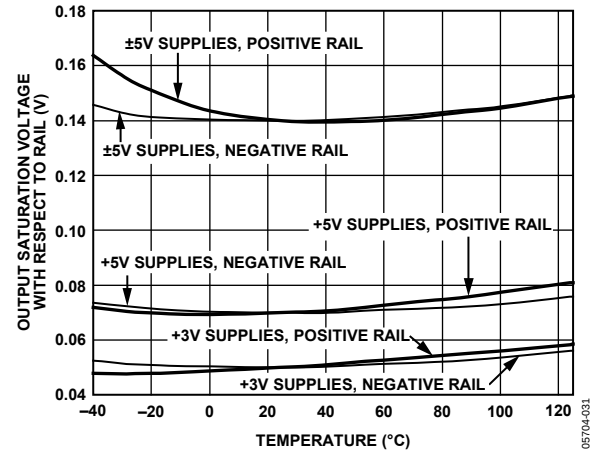


Figure 33. Output Saturation Voltage vs. Temperature

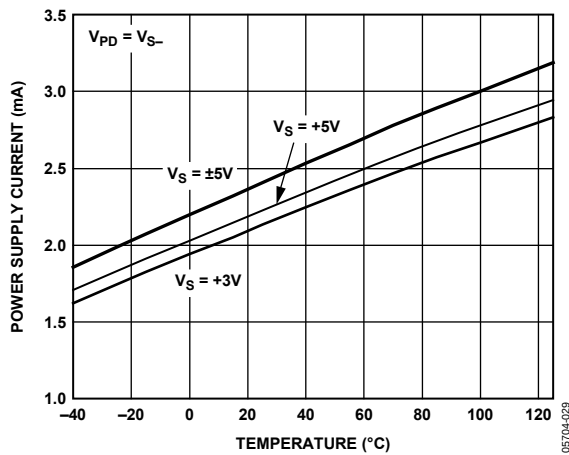


Figure 31. Power Supply Current vs. Temperature

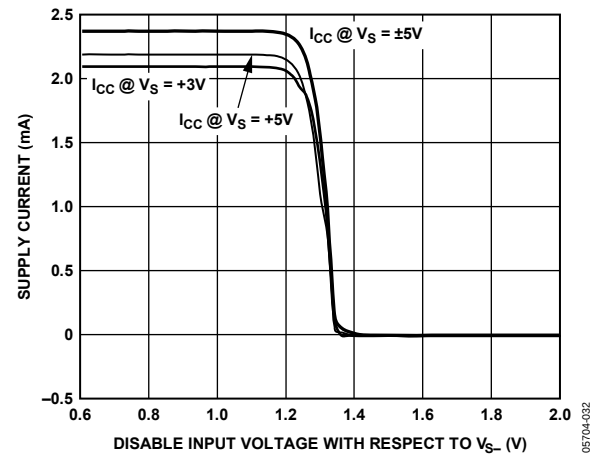


Figure 34. Power Supply Current vs. Disable Voltage

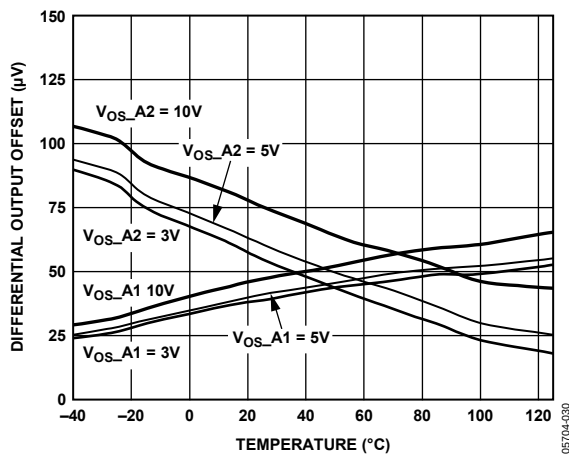


Figure 32. Differential Output Offset Voltage vs. Temperature

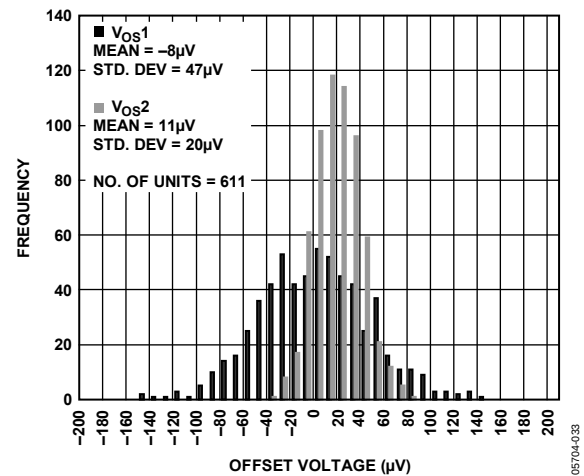


Figure 35. Differential Output Offset Distribution

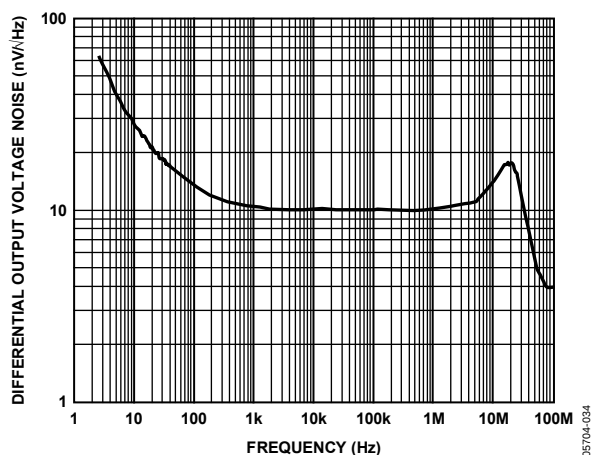


Figure 36. Differential Output Voltage Noise vs. Frequency

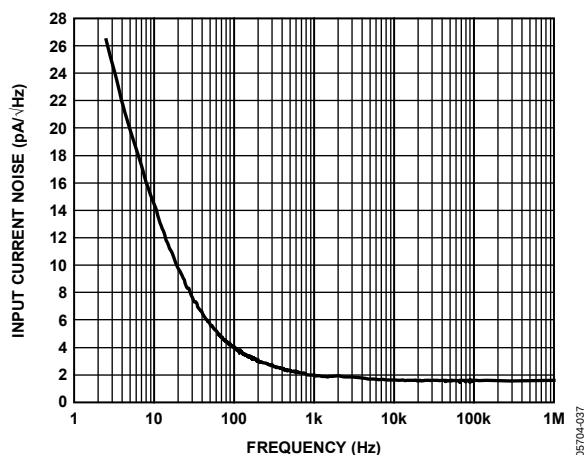


Figure 39. Input Current Noise vs. Frequency

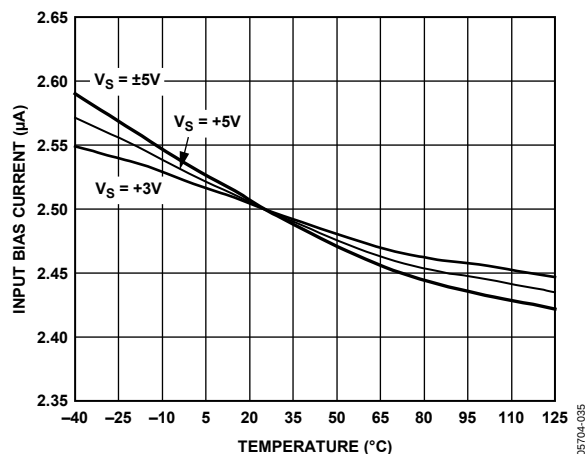


Figure 37. Input Bias Current vs. Temperature for Various Supplies

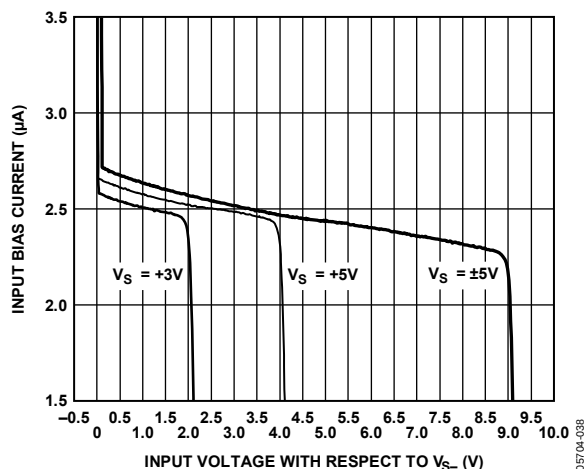


Figure 40. Input Bias Current vs. Input Voltage

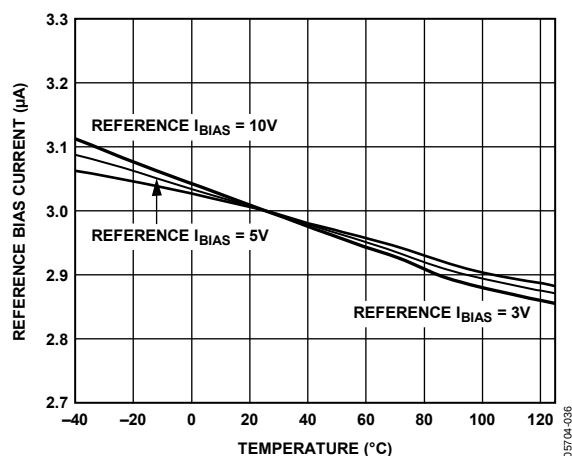


Figure 38. REF Input Bias Current vs. Temperature

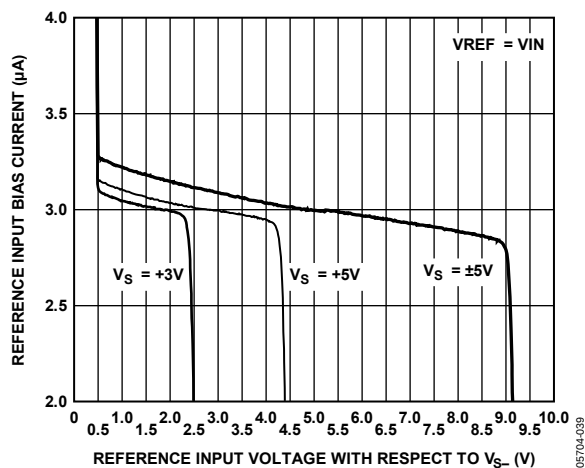


Figure 41. REF Input Bias Current vs. REF Input Voltage

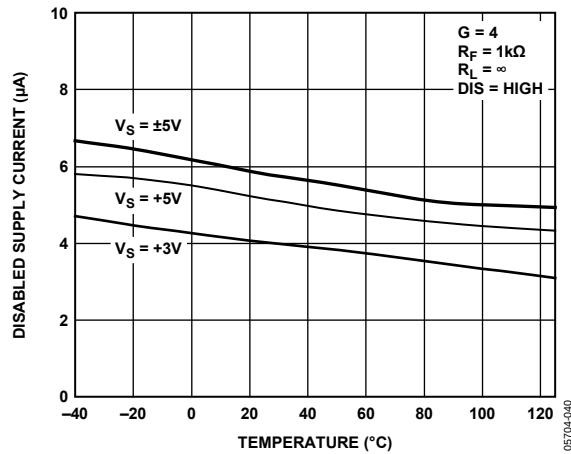


Figure 42. Disable Supply Current vs. Temperature for Various Supplies

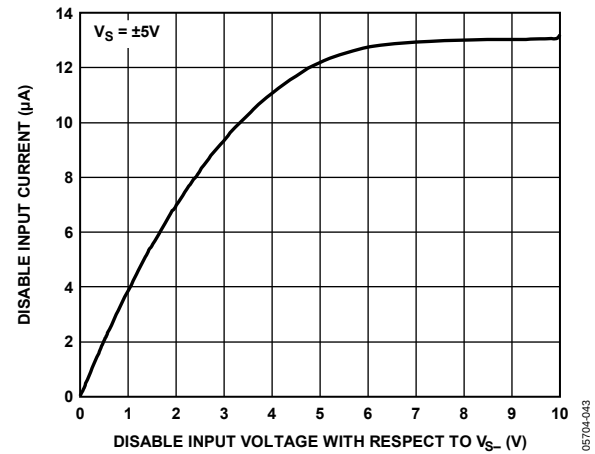


Figure 45. Disable Input Current vs. Disable Input Voltage

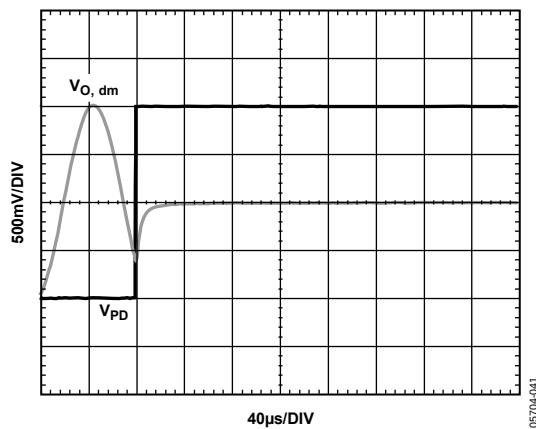


Figure 43. Disable Assert Time

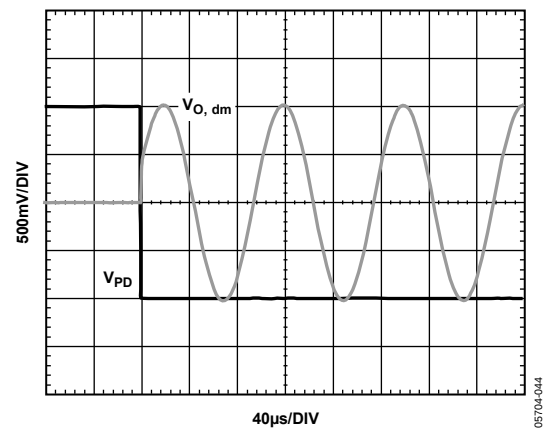


Figure 46. Disable Deassert Time

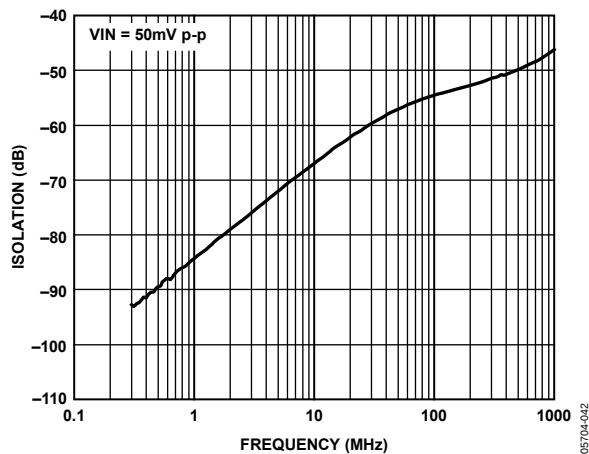


Figure 44. Disabled Input-to-Output Isolation vs. Frequency

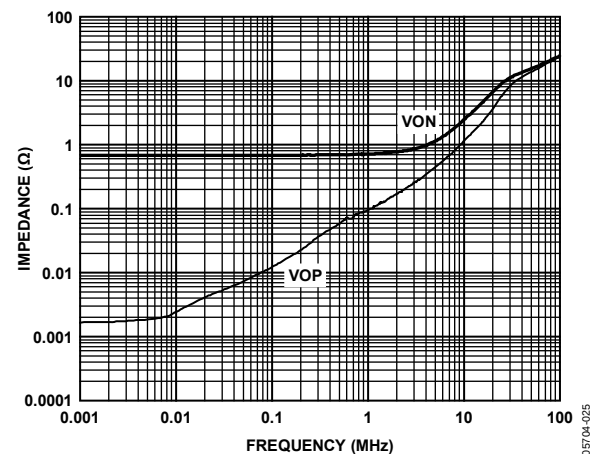


Figure 47. Single-Ended Output Impedance vs. Frequency

THEORY OF OPERATION

The ADA4941-1 is a low power, single-ended input, differential output amplifier optimized for driving high resolution ADCs. Figure 48 illustrates how the ADA4941-1 is typically connected. The amplifier is composed of an uncommitted amplifier, A1, driving a precision inverter, A2. The negative input of A1 is brought out to Pin 1 (FB), allowing for user-programmable gain. The inverting op amp, A2, provides accurate inversion of the output of A1, VOP, producing the output signal VON.

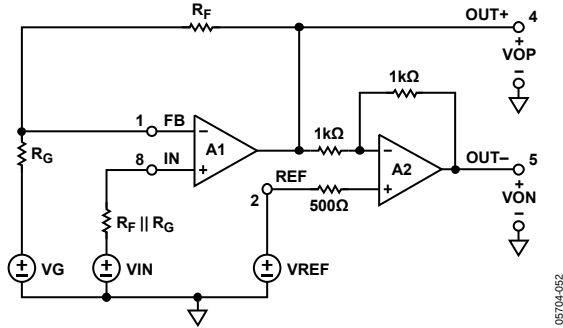


Figure 48. Basic Connections (Power Supplies Not Shown)

The voltage applied to the REF pin appears as the output common-mode voltage. Note that the voltage applied to the REF pin does not affect the voltage at the OUT+ pin. Because of this, a differential offset can exist between the outputs, while the desired output common-mode voltage is present. For example, when VOP = 3.5 V and VON = 1.5 V, the output common-mode voltage is equal to 2.5 V, just as it is when both outputs are at 2.5 V. In the first case, the differential voltage (or offset) is 2.0 V, and in the latter case, the differential voltage is 0 V. When calculating output voltages, both differential and common-mode voltages must be considered at the same time to avoid undesired differential offsets.

BASIC OPERATION

In Figure 48, R_G and R_F form the external gain-setting network. V_G and V_{REF} are externally applied voltages. V_{O, cm} is defined as the output common-mode voltage and V_{O, dm} is defined as the differential-mode output voltage. The following equations can be derived from Figure 48:

$$VOP = VIN \left(1 + \frac{R_F}{R_G} \right) - VG \left(\frac{R_F}{R_G} \right) \quad (1)$$

$$VON = -VIN \left(1 + \frac{R_F}{R_G} \right) + VG \left(\frac{R_F}{R_G} \right) + 2(VREF) \quad (2)$$

$$V_{O, dm} =$$

$$VOP - VON = 2(VIN) \left(1 + \frac{R_F}{R_G} \right) - 2VG \left(\frac{R_F}{R_G} \right) - 2(VREF) \quad (3)$$

$$V_{O, cm} = \left(\frac{VOP + VON}{2} \right) = VREF \quad (4)$$

When R_F = 0 and R_G is removed, Equation 3 simplifies to the following:

$$V_{O, dm} = 2(VIN) - 2(VREF) \quad (5)$$

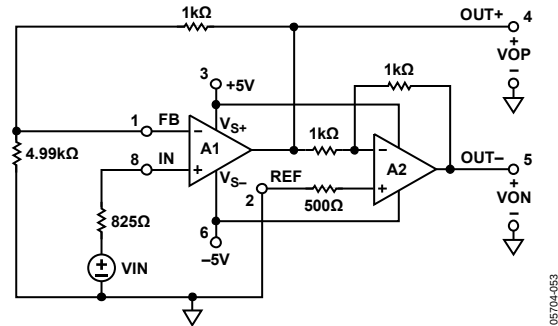


Figure 49. Dual Supply, G = 2.4, Single-Ended-to-Differential Amplifier

Figure 49 shows an example of a dual-supply connection. In this example, V_G and V_{REF} are set to 0 V, and the external R_F and R_G network provides a noninverting gain of 1.2 in A1. This example takes full advantage of the rail-to-rail output stage. The gain equation is

$$VOP - VON = 2.4(VIN) \quad (6)$$

The in-series, 825 Ω resistor combined with Pin 8 compensates for the voltage error generated by the input offset current of A1. The linear output range of both A1 and A2 extends to within 200 mV of each supply rail, which allows a peak-to-peak differential output voltage of 19.2 V on ±5 V supplies.

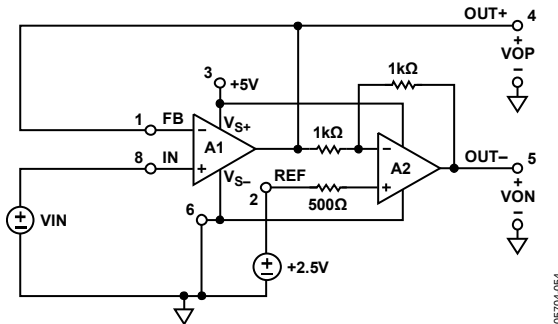


Figure 50. Single +5V Supply, G=2 Single-Ended-to-Differential Amplifier

Figure 50 shows a single 5 V supply connection with A1 used as a unity gain follower. The 2.5 V at the REF pin sets the output common-mode voltage to 2.5 V. The transfer function is then

$$VOP - VON = 2(VIN) - 5V \quad (7)$$

In this case, the linear output voltage is limited by A1. On the low end, the output of A1 starts to saturate and show degraded linearity when VOP approaches 200 mV. On the high end, the input of A1 becomes saturated and exhibits degraded linearity when VIN moves beyond 4 V (within 1 V of VCC). This limits the linear differential output voltage in the circuit shown in Figure 50 to about 7.6 V p-p.

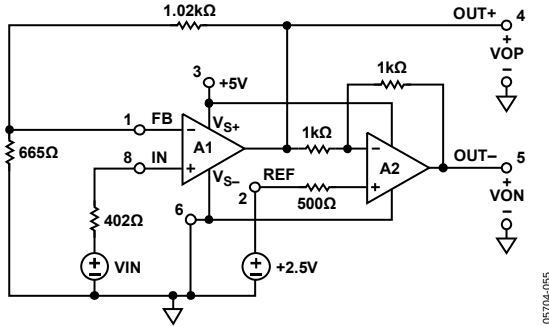


Figure 51. 5 V Supply, G = 5, Single-Ended-to-Differential Amplifier

Figure 51 shows a single 5 V supply connection for G = 5. The R_F and R_G network sets the gain of A1 to 2.5, and the 2.5 V at the REF input provides a centered 2.5 V output common-mode voltage. The transfer function is then

$$VOP - VON = 5(VIN) - 5V \quad (8)$$

The output range limits of A1 and A2 limit the differential output voltage of the circuit shown in Figure 51 to approximately 8.4 V p-p.

DC ERROR CALCULATIONS

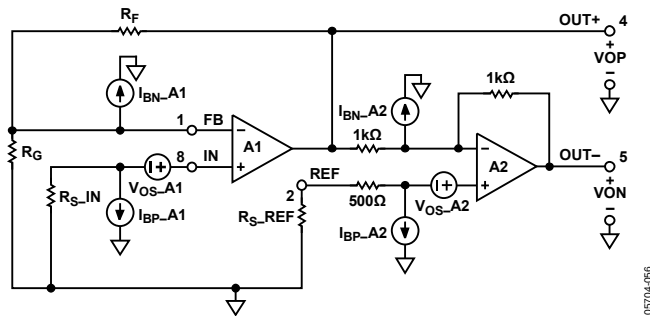


Figure 52. DC Error Sources

Figure 52 shows the major contributions to the dc output voltage error. For each output, the total error voltage can be calculated using familiar op amp concepts. Equation 9 expresses the dc voltage error present at the VOP output.

$$VOP_error = \left(1 + \frac{R_F}{R_G}\right) \left[V_{OS_A1} - (I_{BP_A1})(R_{S_IN}) \right] + (I_{BP_A1})R_F \quad (9)$$

When using data from the Specifications tables, it is often more expedient to use input offset current in place of the individual input bias currents when calculating errors. Input offset current is defined as the magnitude of the difference between the two input bias currents. Using this definition, each input bias current can be expressed in terms of the average of the two input bias currents, I_B , and the input offset current, I_{OS} , as $I_{BP_N} = I_B \pm I_{OS}/2$. DC errors are minimized when $R_S = R_F \parallel R_G$. In this case, Equation 9 is reduced to

$$VOP_error = \left(1 + \frac{R_F}{R_G}\right) \left[V_{OS_A1} \right] + (I_{OS})R_F \quad (R_S = R_F \parallel R_G)$$

Equation 10 expresses the dc voltage error present at the VON output.

$$VON_error = -(VOP_error) + 2[V_{OS_A2} - (I_{BP_A2})(R_{S_REF} + 500)] + 1000(I_{BN_A2}) \quad (10)$$

The internal 500 Ω resistor is provided on-chip to minimize dc errors due to the input offset current in A2. The minimum error is achieved when $R_{S_REF} = 0 \Omega$. In this case, Equation 10 is reduced to

$$VON_error = -(VOP_error) + 2[V_{OS_A2}] + (I_{OS})1000 \quad (R_{S_REF} = 0 \Omega)$$

The differential output voltage error $V_{O_error, dm}$, is the difference between VOP_error and VON_error :

$$V_{O_error, dm} = VOP_error - VON_error \quad (11)$$

The output offset voltage of each amplifier in the ADA4941-1 also includes the effects of finite common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and dc open-loop gain (A_{VOL}).

$$V_{OS} = V_{OS_nom} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_S}{PSRR} + \frac{\Delta VOUT}{A_{VOL}} \quad (12)$$

where:

V_{OS_nom} is the nominal output offset voltage without including the effects of CMRR, PSRR, and A_{VOL} .

Δ indicates the change in conditions from nominal.

V_{CM} is the input common-mode voltage (for A1, the voltage at IN, and for A2, the voltage at REF).

V_S is the power supply voltage.

$VOUT$ is either op amp output.

Table 7, Table 8, and Table 9 show typical error budgets for the circuits shown in Figure 49, Figure 50, and Figure 51.

$R_F = 1.0 \text{ k}\Omega$, $R_G = 4.99 \text{ k}\Omega$, $R_{S_IN} = 825 \text{ }\Omega$, $R_{S_REF} = 0 \text{ }\Omega$

Table 7. Output Voltage Error Budget for G = 2.4 Amplifier Shown in Figure 49

Error Source	Typical Value	VOP_error	VON_error	V _{o_dm_error}
V _{OS_A1}	0.1 mV	+0.12 mV	−0.12 mV	+0.24 mV
I _{BP_A1}	3 μ A	+2.48 mV	−2.48 mV	−4.96 mV
I _{BN_A1}	3 μ A	−2.48 mV	+2.48 mV	+4.96 mV
V _{OS_A2}	0.1 mV	0 mV	+0.2 mV	+0.2 mV

Total V_{O_error, dm} = 0.44 mV

$R_F = 0 \text{ }\Omega$, $R_G = \infty$, $R_{S_IN} = 0 \text{ }\Omega$, $R_{S_REF} = 0 \text{ }\Omega$

Table 8. Output Voltage Error Budget for Amplifier Shown in Figure 50

Error Source	Typical Value	VOP_error	VON_error	V _{o_dm_error}
V _{OS_A1}	0.1 mV	+0.1 mV	−0.1 mV	+0.2 mV
I _{BP_A1}	3 μ A	+2.48 mV	−2.48 mV	−4.96 mV
I _{BN_A1}	3 μ A	−2.48 mV	+2.48 mV	+4.96 mV
V _{OS_A2}	0.1 mV	0 mV	+0.2 mV	+0.2 mV

Total V_{O_error, dm} = 0.4 mV

$R_F = 1.02 \text{ k}\Omega$, $R_G = 665 \text{ }\Omega$, $R_{S_IN} = 402 \text{ }\Omega$, $R_{S_REF} = 0 \text{ }\Omega$

Table 9. Output Voltage Error Budget for G = 5 Amplifier Shown in Figure 51

Error Source	Typical Value	VOP_error	VON_error	V _{o_dm_error}
V _{OS_A1}	0.1 mV	+0.25 mV	−0.25 mV	+0.5 mV
I _{BP_A1}	3 μ A	+1.21 mV	−1.21 mV	−2.4 mV
I _{BN_A1}	3 μ A	−1.21 mV	+1.21 mV	+2.4 mV
V _{OS_A2}	0.1 mV	0 mV	+0.2 mV	+0.2 mV

Total V_{O_error, dm} = 0.7 mV

OUTPUT VOLTAGE NOISE

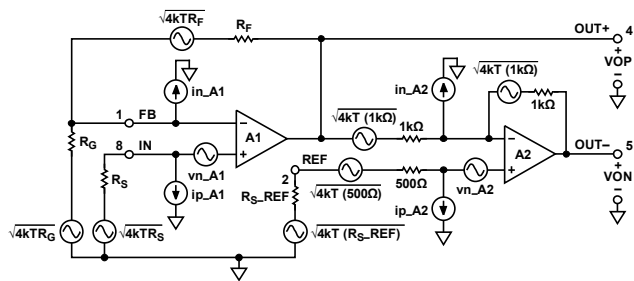


Figure 53. Noise Sources

Figure 53 shows the major contributors to the ADA4941-1 differential output voltage noise. The differential output noise mean-square voltage equals the sum of twice the noise mean-square voltage contributions from the noninverting channel (A1), plus the noise mean-square voltage terms associated with the inverting channel (A2).

$$\begin{aligned} \overline{V_{O, dm_n}^2} = & 2 \left[\left(1 + \frac{R_F}{R_G} \right) \times (\overline{vn_A1}) \right]^2 + 2 \times \\ & \left[\left(1 + \frac{R_F}{R_G} \right) \times (\overline{ip_A1} \times R_S) \right]^2 + 2 [\overline{in_A1} \times R_F]^2 + \\ & 2 \left[\sqrt{4kTR_F} \right]^2 + 2 \left[\sqrt{4kTR_G} \times \frac{R_F}{R_G} \right]^2 + 2 \times \\ & \left[\left(1 + \frac{R_F}{R_G} \right) \times \sqrt{4kTR_S} \right]^2 + \overline{VON_n^2} \end{aligned} \quad (13)$$

where $\overline{VON_n^2}$ is calculated as

$$\begin{aligned} \overline{VON_n^2} = & 4 (\overline{vn_A2})^2 + \\ & 4 [\overline{ip_A2} (500 + R_{S_REF})]^2 + [1000 (\overline{in_A2})]^2 + \\ & 8 kT(1000) + 16 kT(500) + 16 kT(R_{S_REF}) \end{aligned} \quad (14)$$

where:

$\overline{vn_A1}$ and $\overline{vn_A2}$ are the input voltage noises of A1 and A2, each equal to 2.1 nV/ $\sqrt{\text{Hz}}$.

$\overline{in_A1}$, $\overline{in_A2}$, $\overline{ip_A1}$, and $\overline{ip_A2}$ are amplifier input current noise terms, each equal to 1 pA/ $\sqrt{\text{Hz}}$.

R_S , R_F , and R_G are the external source, feedback, and gain resistors, respectively.

kT is Boltzmann's constant times absolute temperature, equal to $4.2 \times 10^{-21} \text{ W}\cdot\text{s}$ at room temperature.

R_{S_REF} is any source resistance at the REF pin.

When A1 is used as a unity gain follower, the output voltage noise spectral density is at its minimum, 10 nV/ $\sqrt{\text{Hz}}$. Higher voltage gains have higher output voltage noise.

Table 10, Table 11, and Table 12 show the noise contributions and output voltage noise for the circuits in Figure 49, Figure 50, and Figure 51.

Table 10. Output Voltage Noise, G = 2.4 Differential Amplifier Shown in Figure 49

Noise Source	Typical Value	VOP Contribution (nV/√Hz)	VON Contribution (nV/√Hz)	V _o , dm Contribution (nV/√Hz)
$\overline{vn_{A1}}$	2.1 nV/√Hz	2.5	2.5	5
$\overline{ip_{A1}}$	1 pA/√Hz	1	1	2
$\overline{in_{A1}}$	1 pA/√Hz	1	1	2
$\sqrt{4 kTR_F}$	4 nV/√Hz	4	4	8
$\sqrt{4 kTR_G}$	9 nV/√Hz	1.8	1.8	3.6
$\sqrt{4 kTR_S}$	3.6 nV/√Hz	4.4	4.4	8.8
$\overline{vn_{inverter}}$	9.2 nV/√Hz	0	9.2	9.2
$\sqrt{R_{S_REF}}$	0	0	0	0
$\overline{ip_{A2} \times R_{S_REF}}$	0	0	0	0
Totals		6.8	11.4	16.5

$R_F = 1.0 \text{ k}\Omega$, $R_G = 4.99 \text{ k}\Omega$, $R_S = 825 \text{ }\Omega$, $R_{S_REF} = 0 \text{ }\Omega$.

$\overline{vn_{inverter}}$ = noise contributions from A2 and its associated internal 1 k Ω feedback resistors and 500 Ω offset current balancing resistor.

Table 11. Output Voltage Noise, G = 2 Differential Amplifier Shown in Figure 50

Noise Source	Typical Value	VOP Contribution (nV/√Hz)	VON Contribution (nV/√Hz)	V _o , dm Contribution (nV/√Hz)
$\overline{vn_{A1}}$	2.1 nV/√Hz	2.1	2.1	4.2
$\overline{ip_{A1}}$	0	0	0	0
$\overline{in_{A1}}$	0	0	0	0
$\sqrt{4 kTR_F}$	0	0	0	0
$\sqrt{4 kTR_G}$	0	0	0	0
$\sqrt{4 kTR_S}$	0	0	0	0
$\overline{vn_{inverter}}$	9.2 nV/√Hz	0	9.2	9.2
$\sqrt{R_{S_REF}}$	0	0	0	0
$\overline{ip_{A2} \times R_{S_REF}}$	0	0	0	0
Totals		2.1	9.4	10

$R_F = 0 \text{ }\Omega$, $R_G = \infty$, $R_S = 0 \text{ }\Omega$, $R_{S_REF} = 0 \text{ }\Omega$.

Table 12. Output Voltage Noise, G = 5 Differential Amplifier Shown in Figure 51

Noise Source	Typical Value	VOP Contribution (nV/√Hz)	VON Contribution (nV/√Hz)	V _o , dm Contribution (nV/√Hz)
$\overline{vn_{A1}}$	2.1 nV/√Hz	5.25	5.25	10.5
$\overline{ip_{A1}}$	1 pA/√Hz	1	1	2
$\overline{in_{A1}}$	1 pA/√Hz	1	1	2
$\sqrt{4 kTR_F}$	4 nV/√Hz	4	4	8
$\sqrt{4 kTR_G}$	3.26 nV/√Hz	4.9	4.9	9.8
$\sqrt{4 kTR_S}$	2.54 nV/√Hz	6.54	6.54	13.1
$\overline{vn_{inverter}}$	9.2 nV/√Hz	0	9.2	9.2
$\sqrt{R_{S_REF}}$	0	0	0	0
$\overline{ip_{A2} \times R_{S_REF}}$	0	0	0	0
Totals		10.7	14.1	23.1

$R_F = 1.02 \text{ k}\Omega$, $R_G = 665 \text{ }\Omega$, $R_S = 402 \text{ }\Omega$, $R_{S_REF} = 0 \text{ }\Omega$.

FREQUENCY RESPONSE VS. CLOSED-LOOP GAIN

The operational amplifiers used in the ADA4941-1 are voltage feedback with an open-loop frequency response that can be approximated with the integrator response, as shown in Figure 54.

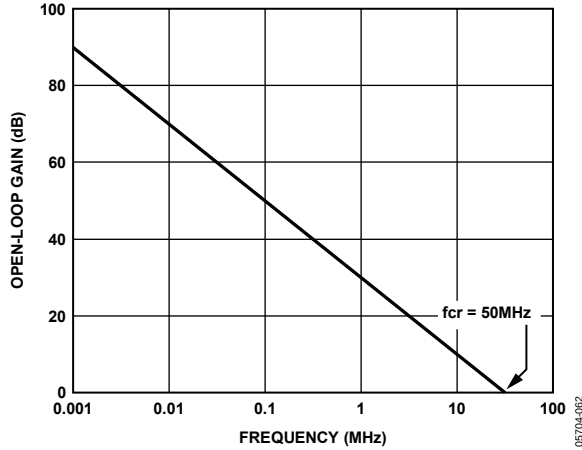


Figure 54. ADA4941-1 Op Amp Open-Loop Gain vs. Frequency

For each amplifier, the frequency response can be approximated by the following equations:

$$V_{O_A1} = VIN \times \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + \left[\frac{R_F + R_G}{R_G} \right] \times \frac{f}{f_{cr}}} \right) \quad (15)$$

(Noninverting Response)

$$V_{O_A2} = VIN \times \left(\frac{-R_F}{R_G} \right) \times \left(\frac{1}{1 + \left[\frac{R_F + R_G}{R_G} \right] \times \frac{f}{f_{cr}}} \right) \quad (16)$$

(Inverting Response)

f_{CR} is the gain-bandwidth frequency of the amplifier (where the open-loop gain shown in Figure 54 equals 1). f_{CR} for both amplifiers is about 50 MHz.

The inverting amplifier A2 has a fixed feedback network. The transfer function is approximately

$$V_{O_A2} = -VIN \times \left(\frac{1}{1 + \frac{2 \times f}{50 \text{ MHz}}} \right) = -VOP \times \left(\frac{1}{1 + \frac{f}{25 \text{ MHz}}} \right) \quad (17)$$

The frequency response of A1 depends on the external feedback network as indicated by Equation 15. The overall differential output voltage is therefore

$$V_{O, dm} = VOP - VON = VOP + VOP \times \left(\frac{1}{1 + \frac{f}{25 \text{ MHz}}} \right) \quad (18)$$

$$V_{O, dm} = VIN \times \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + \left[\frac{R_F + R_G}{R_G} \right] \times \frac{f}{50 \text{ MHz}}} \right) \times \left(\frac{1 + \frac{1}{1 + \frac{f}{25 \text{ MHz}}}}{1 + \frac{f}{25 \text{ MHz}}} \right) \quad (19)$$

Multiplying the terms and neglecting negligible terms leads to the following approximation:

$$V_{O, dm} = VIN \times \left(1 + \frac{R_F}{R_G}\right) \times \left[\frac{2}{\left(1 + \left[\frac{R_F + R_G}{R_G} \right] \times \frac{f}{50 \text{ MHz}}\right) \times \left(1 + \frac{f}{25 \text{ MHz}}\right)} \right] \quad (20)$$

There are two poles in this transfer function, and the lower frequency pole limits the bandwidth of the differential amplifier. If VOP is shorted to IN- (A1 is a unity gain follower), the 25 MHz closed-loop bandwidth of the inverting channel limits the overall bandwidth. When A1 is operating with higher noise gains, the bandwidth is limited by the closed-loop bandwidth of A1, which is inversely proportional to the noise gain $(1 + R_F/R_G)$. For instance, if the external feedback network provides a noise gain of 10, the bandwidth drops to 5 MHz.

APPLICATIONS INFORMATION

OVERVIEW

The [ADA4941-1](#) is an adjustable-gain, single-ended-to-differential voltage amplifier, optimized for driving high resolution ADCs. Single-ended-to-differential gain is controlled by one feedback network, comprised of two external resistors: R_F and R_G .

USING THE REF PIN

The REF pin sets the output baseline in the inverting path and is used as a reference for the input signal. In most applications, the REF pin is set to the input signal midswing level, which in many cases is also midsupply. For bipolar signals and dual power supplies, REF is generally set to ground. In single-supply applications, setting REF to the input signal midswing level provides optimal output dynamic range performance with minimum differential offset. Note that the REF input only affects the inverting signal path or VON.

Most applications require a differential output signal with the same dc common-mode level on each output. It is possible for the signal measured across VOP and VON to have a common-mode voltage that is of the desired level but not common to both outputs. This type of signal is generally avoided because it does not allow for optimal use of the output dynamic range of the amplifier.

Defining V_{IN} as the voltage applied to the input pin, the equations that govern the two signal paths are given in Equation 21 and Equation 22.

$$VOP = VIN \quad (21)$$

$$VON = -VIN + 2(REF) \quad (22)$$

When the REF voltage is set to the midswing level of the input signal, the two output signals fall directly on top of each other with minimal offset. Setting the REF voltage elsewhere results in an offset between the two outputs.

The best use of the REF pin can be further illustrated by considering a single-supply case with a 10 V power supply and an input signal that varies between 2 V and 7 V. This is a case where the midswing level of the input signal is not at midsupply but is at 4.5 V. Setting the REF input at 4.5 V and neglecting offsets, Equation 21 and Equation 22 are used to calculate the results. When the input signal is at its midpoint of 4.5 V, $OUT+$ is at 4.5 V, as is VON. This can be considered as a baseline state where the differential output voltage is 0. When the input increases to 7 V, VOP tracks the input to 7 V, and VON decreases to 2 V. This can be viewed as a positive peak signal where the differential output voltage equals 5 V. When the input signal decreases to 2 V, VOP again tracks to 2 V, and VON increases to 7 V. This can be viewed as a negative peak signal where the differential output voltage equals -5 V. The resulting differential output voltage is 10 V p-p.

The previous discussion reveals how the single-ended-to-differential gain of 2 is achieved.

INTERNAL FEEDBACK NETWORK POWER DISSIPATION

While traditional op amps do not have on-chip feedback elements, the [ADA4941-1](#) contains two on-chip, 1 k Ω resistors that comprise an internal feedback loop. The power dissipated in these resistors must be included in the overall power dissipation calculations for the device. Under certain circumstances, the power dissipated in these resistors could be comparable to the quiescent dissipation of the device. For example, on ± 5 V supplies with the REF pin tied to ground and $OUT-$ at +4 VDC, each 1 k Ω resistor carries 4 mA and dissipates 16 mW for a total of 32 mW. This is comparable to the quiescent power and must therefore be included in the overall device power dissipation calculations. For ac signals, rms analysis is required.

DISABLE FEATURE

The [ADA4941-1](#) includes a disable feature that can be asserted to minimize power consumption in a device that is not needed at a particular time. When asserted, the disable feature does not place the device output in a high impedance or tristate condition. The disable feature is active high. See the Specifications tables for the high and low level voltage specifications.

ADDING A 3-POLE, Sallen-Key FILTER

The noninverting amplifier in the ADA4941-1 can be used as the buffer amplifier of a Sallen-Key filter. A 3-pole, low-pass filter can be designed to limit the signal bandwidth in front of an ADC. The input signal first passes through the noninverting stage where it is filtered. The filtered signal is then passed through the inverting stage to obtain the complementary output.

Figure 55 illustrates a 3-pole, Sallen-Key, low-pass filter with a -3 dB cutoff frequency of 100 kHz. The 1.69 k Ω resistor is included to minimize dc errors due to the input offset current in A1. The passive RC filters on the outputs are generally required by the ADC converter that is being driven. The frequency response of the filter is shown in Figure 56.

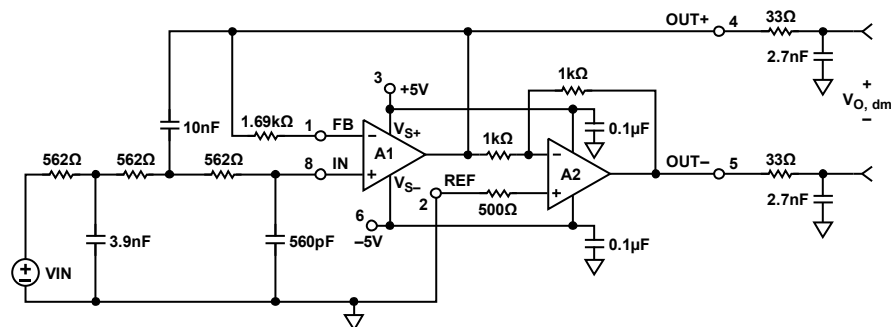


Figure 55. Sallen-Key, Low-Pass Filter with 100 kHz Cutoff Frequency

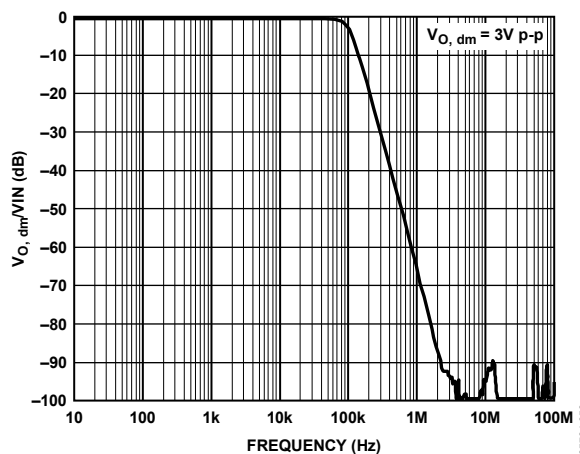


Figure 56. Frequency Response of the Circuit Shown in Figure 55

DRIVING THE AD7687 ADC

The ADA4941-1 is an excellent driver for high resolution ADCs, such as the AD7687, as shown in Figure 57. The Sallen-Key, low-pass filter shown in Figure 55 is included in this example but is not required. The circuit shown in Figure 57 accepts single-ended input signals that swing between 0 V and 3 V.

The ADR443 provides a stable, low noise, 3 V reference that is buffered by one of the AD8032 amplifiers and applied to the AD7687 REF input, providing a differential input full-scale level of 6 V. The reference voltage is also divided by two and buffered to supply the midsupply REF level of 1.5 V for the ADA4941-1.

GAIN OF -2 CONFIGURATION

The ADA4941-1 can be operated in a configuration referred to as gain of -2. Clearly, a gain of -2 can be achieved by simply swapping the outputs of a gain of +2 circuit, but the configuration described here is different. The configuration is referred to as having negative gain to emphasize that the input amplifier, A1, is operated as an inverting amplifier instead of in its usual noninverting mode. As implied in its name, the voltage gain from V_{IN} to $V_{O, dm}$ is -2 V/V. See Figure 58 for the gain of -2 configuration on ± 5 V supplies.

The gain of -2 configuration is most useful in applications that have wide input swings because the input common-mode voltages are held at constant levels. The signal size is therefore constrained by the output swing limits. The gain of -2 has a low input resistance that is equal to R_G .

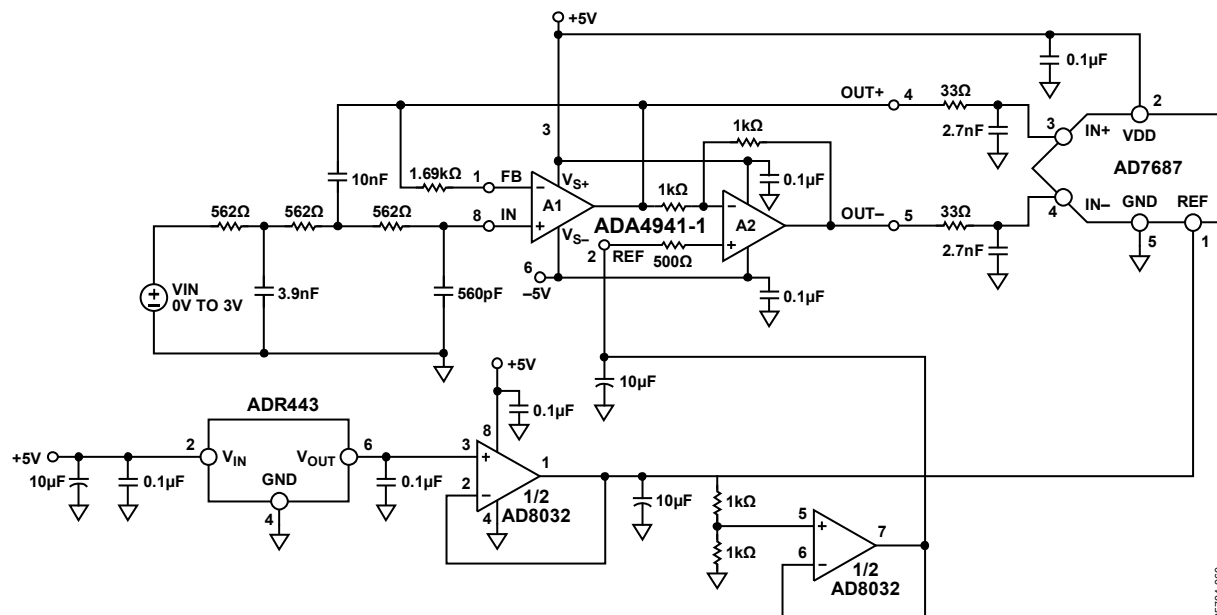


Figure 57. ADA4941-1 Driving the AD7687 ADC

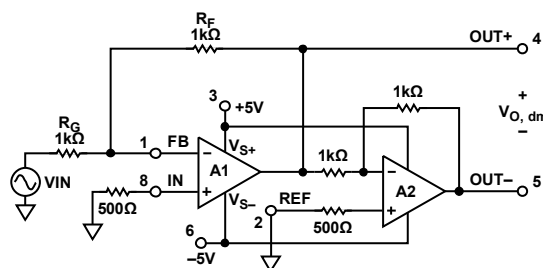
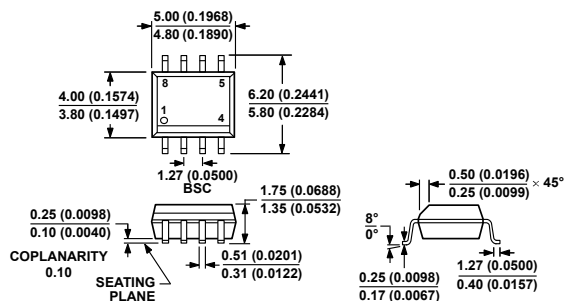


Figure 58. Gain of -2 Configuration

OUTLINE DIMENSIONS

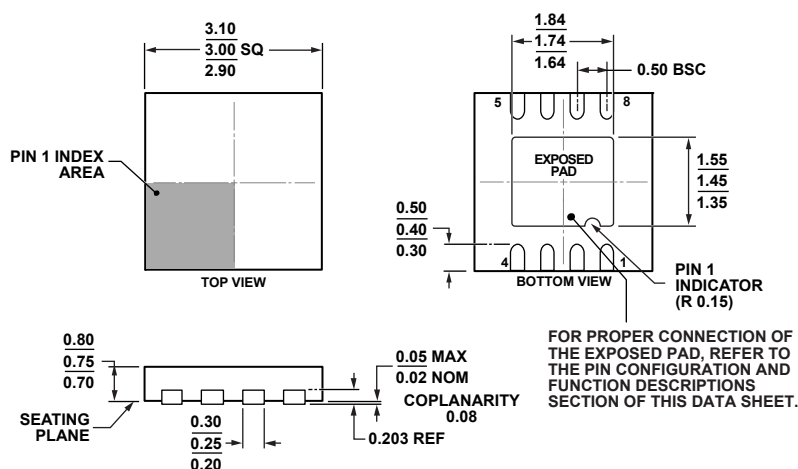


COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 59. 8-Lead Standard Small Outline Package [SOIC_N]

Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-229-WEED

Figure 60. 8-Lead Lead Frame Chip Scale Package [LFCSPP]

3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4941-1YRZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	98	
ADA4941-1YRZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	2,500	
ADA4941-1YRZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	1,000	
ADA4941-1YCPZ-R2	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSPP]	CP-8-13	250	H0C
ADA4941-1YCPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSPP]	CP-8-13	5,000	H0C
ADA4941-1YCPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSPP]	CP-8-13	1,500	H0C
ADA4941-1YCP-EBZ		Evaluation Board			

¹ Z = RoHS Compliant Part.