AD8315 Evaluation Boards

EVAL-AD8315EB

BOARD DESCRIPTION

Figure 1 shows the schematic of the AD8315 MSOP evaluation board. The layout and silkscreen of the component side are shown in Figures 2 and 3. An evaluation board is also available for the LFCSP package (for exact part numbers, see Ordering Guide). Apart from the slightly smaller device footprint, the LFCSP evaluation board is identical to the MSOP board. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by a single 0.1 µF capacitor. Table I details the various configuration options of the evaluation board.

For operation in controller mode, both jumpers, LK1 and LK2, should be removed. The setpoint voltage is applied to VSET, RFIN is connected to the RF source (PA output or directional coupler), and VAPC is connected to the gain control pin of the PA. When used in controller mode, a capacitor must be installed in C4 for loop stability. For GSM/DCS handset power amplifiers, this capacitor should typically range from 150 pF to 300 pF.

A quasi-measurement mode (where the AD8315 delivers an output voltage proportional to the log of the input signal) can be implemented to establish the relationship between VSET and RFIN by installing the two jumpers, LK1 and LK2. This mimics an AGC loop. To establish the transfer function of the log amp, the RF input should be swept while the voltage on VSET is measured; that is, the SMA connector labeled VSET now acts as an output. This is the simplest method to validate operation of the evaluation board. When operated in this mode, a large capacitor (0.01 µF or greater) must be installed in C4 (filter capacitor) to ensure loop stability.

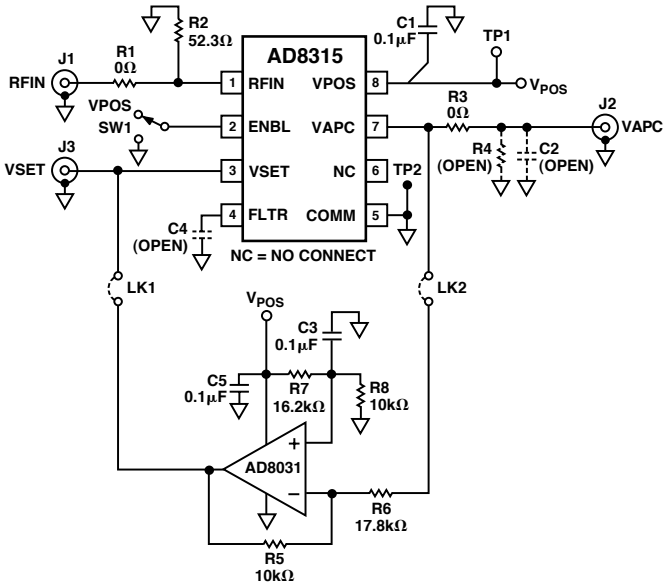

Figure 1. Evaluation Board Schematic (MSOP)

ORDERING GUIDE

Model	Package Description
AD8315-EVAL	MSOP Evaluation Board
AD8315ACP-EVAL	LFCSP Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the EVAL-AD8315EB features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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Table I. Evaluation Board Configuration Options

Component	Function	Default Condition
TP1, TP2	Supply and Ground Vector Pins.	Not Applicable
SW1	Device Enable. When in Position A, the ENBL pin is connected to VPOS and the AD8315 is in operating mode. In Position B, the ENBL pin is grounded, putting the device in power-down mode.	SW1 = A
R1, R2	Input Interface. The 52.3 Ω resistor in Position R2 combines with the AD8315's internal input impedance to give a broadband input impedance of around 50 Ω. A reactive match can be implemented by replacing R2 with an inductor and R1 (0 Ω) with a capacitor. Note that the AD8315's RF input is internally ac-coupled.	R2 = 52.3 Ω (Size 0603) R1 = 0 Ω (Size 0402)
R3, R4, C2	Output Interface. R4 and C2 can be used to check the response of VAPC to capacitive and resistive loading. R3, R4 can be used to reduce the slope of VAPC.	R4 = C2 = Open (Size 0603) R3 = 0 Ω (Size 0603)
C1	Power Supply Decoupling. The nominal supply decoupling consists of a 0.1 µF capacitor.	C1 = 0.1 µF (Size 0603)
C4	Filter Capacitor. The response time of VAPC can be modified by placing a capacitor between FLTR (Pin 4) and ground.	C4 = Open (Size 0603)
LK1, LK2	Measurement Mode. A quasi-measurement mode can be implemented by installing LK1 and LK2 (connecting an inverted VAPC to VSET) to yield the nominal relationship between RFIN and VSET. In this mode, a large capacitor (0.01 µF or greater) must be installed in C4.	LK1, LK2 = Installed

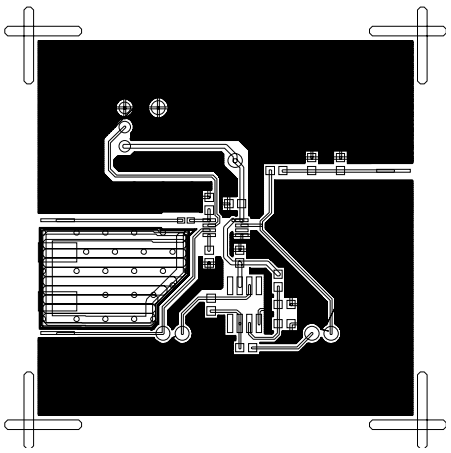

Figure 2. Layout of Component Side (MSOP)

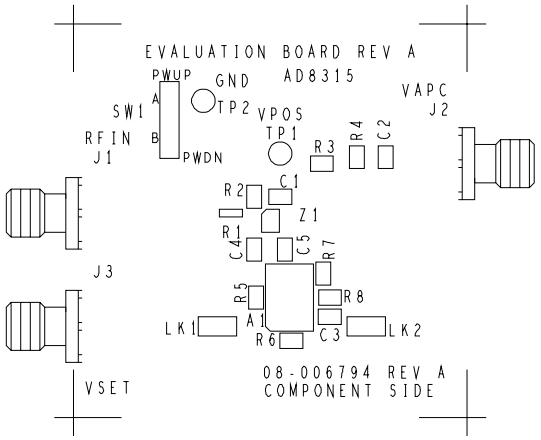

Figure 3. Silkscreen of Component Side (MSOP)