

## Dual-Port 10/100/1000BASE-T PHY with Synchronous Ethernet and QSGMII/SGMII/RGMII MAC Datasheet

### INTRODUCTION

VSC8552 is a low-power, dual-port Gigabit Ethernet transceiver with two SerDes interfaces for dual-port dual media capability. It also includes an integrated dual port two-wire serial multiplexer (MUX) to control SFPs or PoE modules. It has a low Electromagnetic Interference (EMI) line driver, and integrated line side termination resistors that conserve both power and Printed Circuit Board (PCB) space.

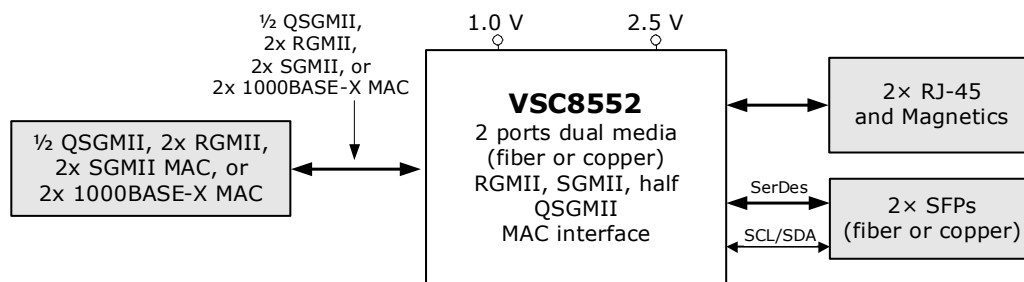
VSC8552 includes dual recovered clock outputs to support Synchronous Ethernet applications. Programmable clock squelch control is included to inhibit undesirable clocks from propagating and to help prevent timing loops. VSC8552 also supports a ring resiliency feature that allows a 1000BASE-T connected PHY port to switch between master and slave timing without having to interrupt the 1000BASE-T link.

Using Microchip's EcoEthernet v2.0 PHY technology, VSC8552 supports energy efficiency features such as Energy Efficient Ethernet (EEE), ActiPHY link down power savings, and PerfectReach that can adjust power based on the cable length. It also supports fully optimized power consumption in all link speeds.

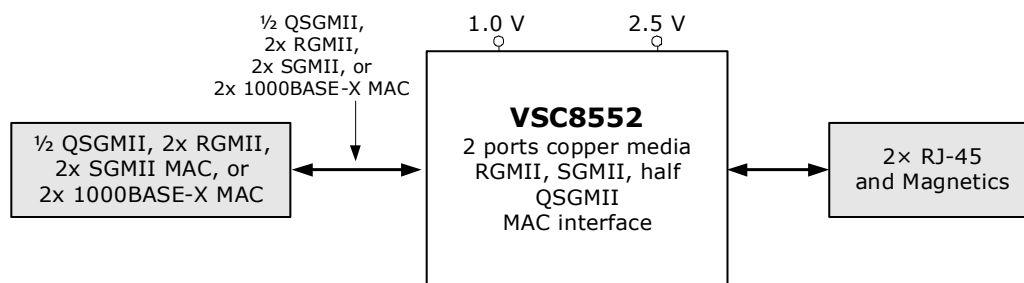
Microchip's mixed signal and Digital Signal Processing (DSP) architecture is a key operational feature of VSC8552, assuring robust performance even under less-than-favorable environmental conditions. It supports both half-duplex and full-duplex 10BASE-T, 100BASE-TX, and 1000BASE-T communication speeds over Category 5 (Cat5) Unshielded Twisted Pair (UTP) cable at distances greater than 100m, displaying excellent tolerance to NEXT, FEXT, echo, and other types of ambient environmental and system electronic noise. The device also supports two dual media ports that can support up to two 100BASE-FX, 1000BASE-X fiber, and/or triple-speed copper SFPs.

The following illustrations show a high-level, general view of typical VSC8552 applications.

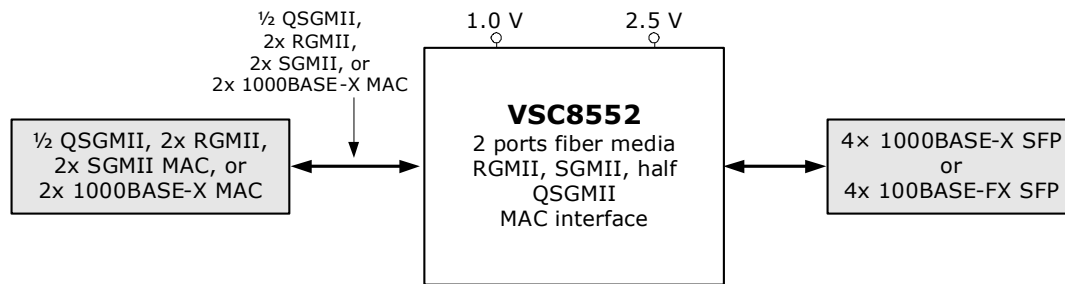
**FIGURE 1: DUAL MEDIA APPLICATION DIAGRAM**



**FIGURE 2: COPPER TRANSCEIVER APPLICATION DIAGRAM**



**FIGURE 3: FIBER MEDIA TRANSCEIVER APPLICATION DIAGRAM**



## Key Features

This section lists the main features and benefits of the VSC8552 device.

### LOW POWER

- Low power consumption of approximately 425 mW per port in 1000BASE-T mode, 200 mW per port in 100BASE-TX mode, 225 mW per port in 10BASE-T mode, and less than 115 mW per port in 100BASE-FX and 1000BASE-X modes
- ActiPHY™ link down power savings
- PerfectReach™ smart cable reach algorithm
- IEEE® 802.3az-2010 Energy Efficient Ethernet idle power savings

### ADVANCED CARRIER ETHERNET SUPPORT

- Recovered clock outputs with programmable clock squelch control and fast link failure indication (<1 ms; worst-case <3 ms) for G.8261 Synchronous Ethernet applications
- Ring resiliency for maintaining linkup integrity when switching between 1000BASE-T master and slave timing
- Supports IEEE 802.3bf timing and synchronization standard
- Integrated dual two-wire serial mux to control SFP and PoE modules
- Support for IEEE 802.3ah unidirectional transport for 100BASE-FX and 1000BASE-X fiber media

### WIDE RANGE OF SUPPORT

- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, 1000BASE-T, 100BASE-FX, and 1000BASE-X) specifications
- Support for >16 kB jumbo frames in all speeds with programmable synchronization FIFOs
- Supports Cisco QSGMII v1.3, Cisco SGMII v1.9, RGMII versions 1.3 and 2.0 (2.5V), 1000BASE-X MACs, IEEE 1149.1 JTAG boundary scan, and IEEE 1149.6 AC-JTAG
- Available in a low-cost, 256-pin BGA package with a 17 mm × 17 mm body size

### FLEXIBILITY

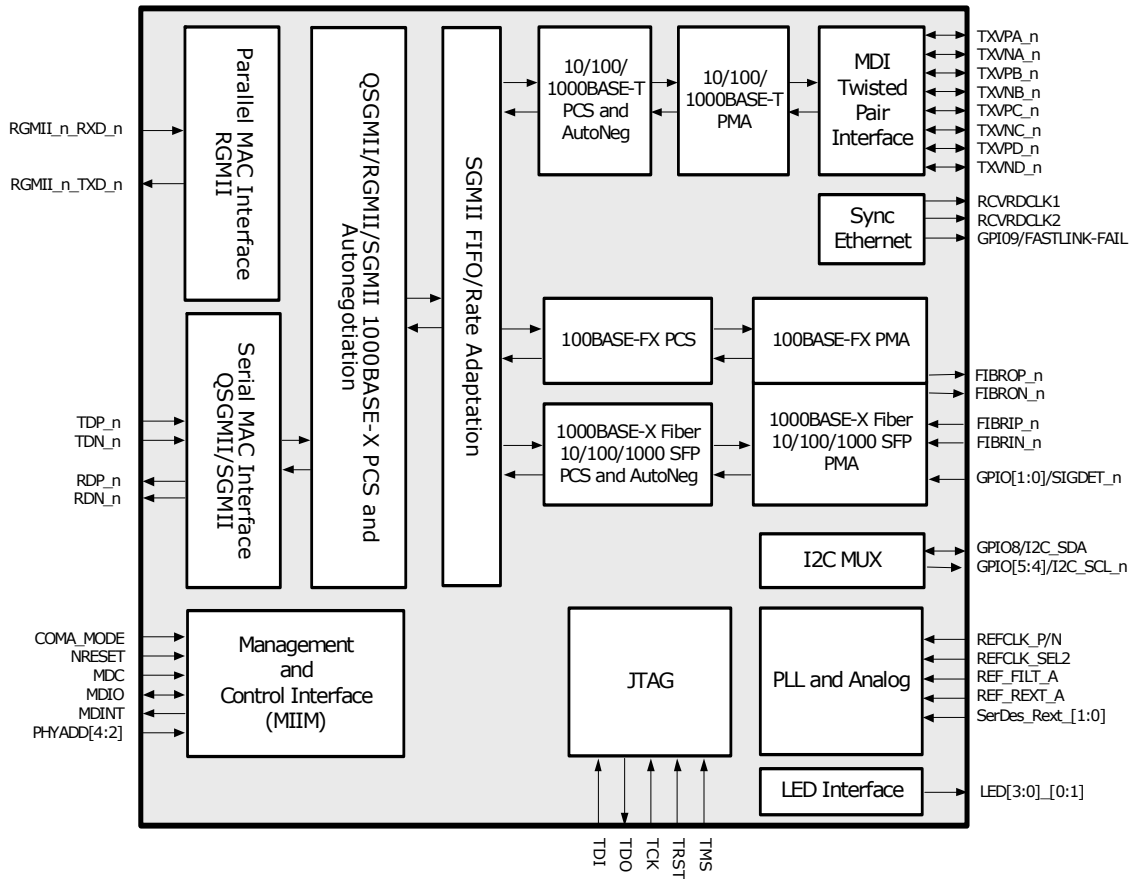
- VeriPHY® cable diagnostics suite provides extensive network cable information such as cable length, termination status, and open/short fault location
- Patented, low EMI line driver with integrated line side termination resistors
- Four programmable direct-drive LEDs per port with adjustable brightness levels using register controls; bi-color LED support using two LED pins
- Serial LED interface option
- Extensive test features including near end, far end, copper media connector, SerDes MAC/media loopback, and Ethernet packet generator with CRC error counter to decrease time-to-market

**Note:** All MAC interfaces must be the same—all QSGMII, RGMII, or SGMII.

## Block Diagram

The following illustration shows the primary functional blocks of the VSC8552 device.

**FIGURE 4: BLOCK DIAGRAM**



**Note:** All MAC interfaces must be the same—all QSGMII, RGMII, SGMII, or 1000BASE-X.

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## 1.0 FUNCTIONAL DESCRIPTIONS

This section describes the functional aspects of the VSC8552 device, including available configurations, operational features, and testing functionality. It also defines the device setup parameters that configure the device for a particular application.

### 1.1 Operating Modes

The following table lists the operating modes of the VSC8552 device.

**TABLE 1-1: OPERATING MODES**

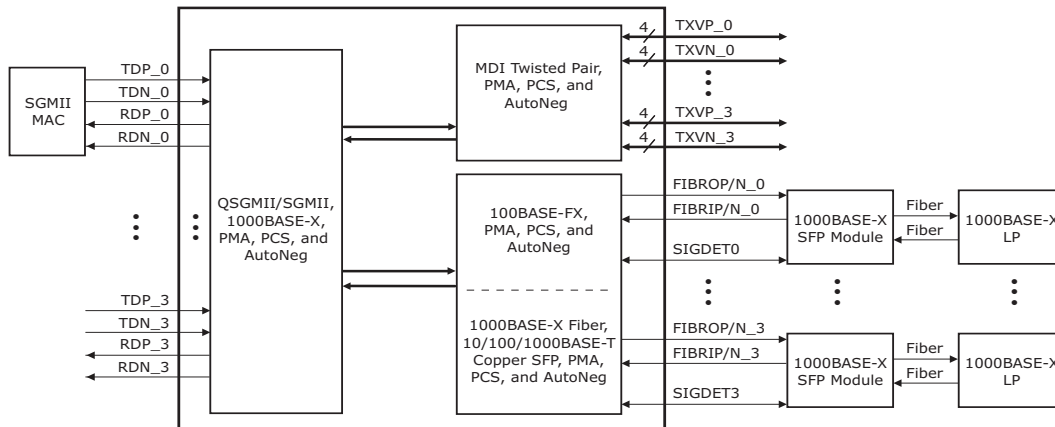
| Operating Mode                                              | Supported Media                                                                         | Notes                            |
|-------------------------------------------------------------|-----------------------------------------------------------------------------------------|----------------------------------|
| QSGMII/RGMII/SGMII<br>MAC-to-1000BASE-X Link Partner        | 1000BASE-X                                                                              | See <a href="#">Figure 1-1</a> . |
| QSGMII/RGMII/SGMII<br>MAC-to-100BASE-FX Link Partner        | 100BASE-FX                                                                              | See <a href="#">Figure 1-3</a> . |
| QSGMII/RGMII/SGMII MAC-to-AMS<br>and 1000BASE-X SerDes      | 1000BASE-X,<br>10/100/1000BASE-T                                                        | See <a href="#">Figure 1-4</a> . |
| QSGMII/RGMII/SGMII MAC-to-AMS<br>and 100BASE-FX SerDes      | 100BASE-FX,<br>10/100/1000BASE-T                                                        | See <a href="#">Figure 1-5</a> . |
| QSGMII/RGMII/SGMII MAC-to-AMS<br>and Protocol Transfer mode | SFP/Fiber Protocol<br>Transfer mode<br>(10/100/1000BASE-T Cu<br>SFP), 10/100/1000BASE-T | See <a href="#">Figure 1-6</a> . |
| QSGMII/RGMII/SGMII MAC-to-Cat5<br>Link Partner              | 10/100/1000BASE-T                                                                       | See <a href="#">Figure 1-7</a> . |
| QSGMII/RGMII/SGMII<br>MAC-to-Protocol Transfer mode         | SFP/Fiber Protocol<br>Transfer mode<br>(10/100/1000BASE-T<br>Cu SFP)                    | See <a href="#">Figure 1-8</a> . |
| 1000BASE-X MAC-to-Cat5 Link<br>Partner                      | 1000BASE-T only                                                                         | See <a href="#">Figure 1-9</a> . |

**Note:** All MAC interfaces must be the same — all QSGMII, RGMII, or SGMII.

#### 1.1.1 QSGMII/SGMII MAC-TO-1000BASE-X LINK PARTNER

The following illustrations and sections show the register settings used to configure a QSGMII/SGMII MAC-to-1000BASE-X link partner.

**FIGURE 1-1: SGMII MAC-TO-1000BASE-X LINK PARTNER**

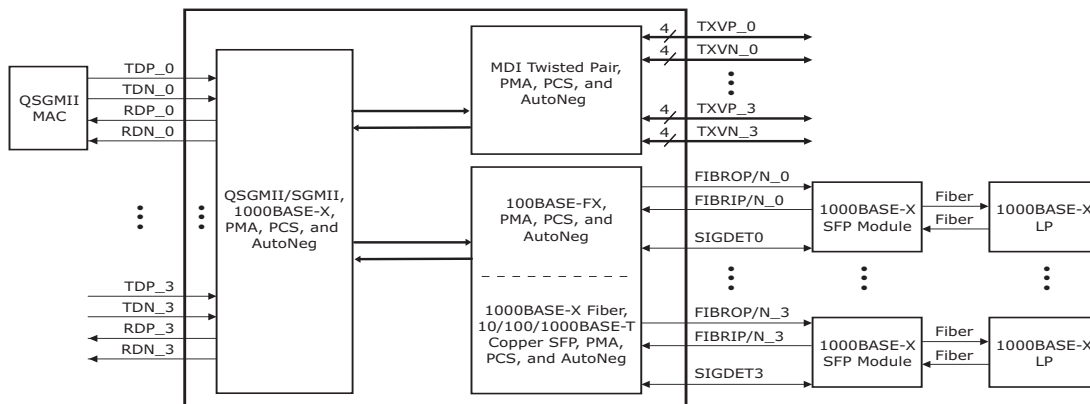


## 1.1.1.1 MAC Interface SGMII

Use the following settings to configure the SGMII MAC interface.

- Set register 19G bits 15:14 = 00.
- Set register 23 (main register) bit 12 = 0.
- Set register 18G = 0x80F0. For more information, see [Table 2-49](#).

**FIGURE 1-2: QSGMII MAC-TO-1000BASE-X LINK PARTNER**



## 1.1.1.2 MAC Interface QSGMII

Use the following settings to configure the QSGMII MAC interface.

- Set register 19G bits 15:14 = 01.
- Set register 23 (main register) bit 12 = 0.
- Set register 18G = 0x80F0. For more information, see [Table 2-49](#).

## 1.1.1.3 Media Interface 1000BASE-X SFP Fiber (1000BASE-X Link Partner)

Use the following settings to configure the 1000BASE-X SFP fiber media interface.

- Set register 23 bits 10:8 = 010.
- Set register 0 bit 12 = 1 (enable autonegotiation).
- Set register 18G = 0x8FC1. For more information, see [Table 2-49](#).

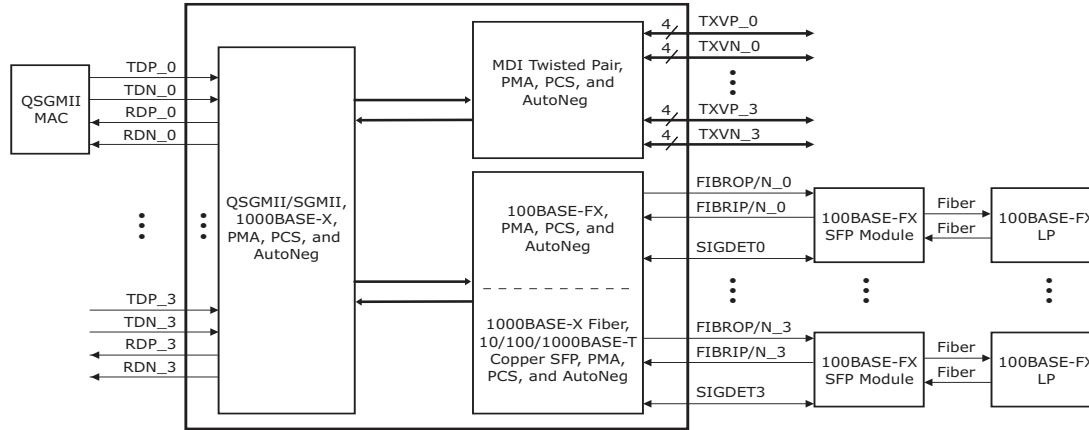
The F in 0x8FC1 identifies the port. To exclude a port from the configuration, set its bit to 0. For example, the configuration of port 0 and port 1 to 1000BASE-X is 0011 or 3, making the bit setting 0x83C1.

**Note:** Whenever there is a mode change a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

## 1.1.2 QSGMII/SGMII MAC-TO-100BASE-FX LINK PARTNER

The following illustration and sections show the register settings used to configure a QSGMII/SGMII MAC-to-100BASE-FX link partner.

**FIGURE 1-3: QSGMII/SGMII MAC-TO-100BASE-FX LINK PARTNER**



### 1.1.2.1 MAC Interface SGMII

Use the following settings to configure the SGMII MAC interface.

- Set register 19G bits 15:14 = 00.
- Set register 23 (main register) bit 12 = 0.
- Set register 18G = 0x80F0. For more information, see [Table 2-49](#).

### 1.1.2.2 Media Interface 100BASE-FX SFP Fiber (100BASE-FX Link Partner)

Use the following settings to configure the 100BASE-FX SFP fiber media interface.

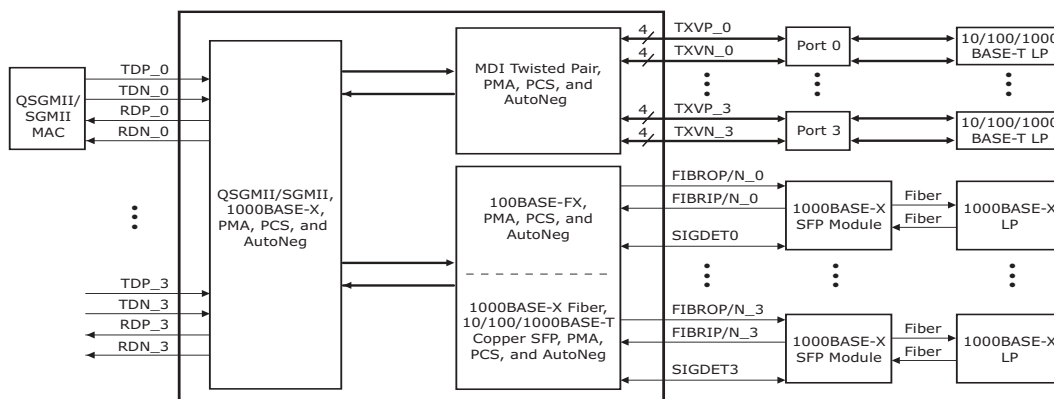
- Set register 23 bits 10:8 = 011.
- Set register 0 bit 12 = 0 (autonegotiation not present in 100BASE-FX PHY).
- Set register 18G = 0x8FD1. For more information, see [Table 2-49](#).

For QSGMII only port 0 is used.

**Note:** Whenever there is a mode change a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

### 1.1.3 QSGMII/SGMII MAC-TO-AMS AND 1000BASE-X MEDIA SERDES

The following illustration and sections show the register settings used to configure a QSGMII/SGMII MAC-to-AMS and 1000BASE-X media SerDes.

**FIGURE 1-4: QSGMII/SGMII MAC-TO-AMS AND 1000BASE-X MEDIA SERDES**

#### 1.1.3.1 MAC Interface SGMII

Use the following settings to configure the SGMII MAC interface.

- Set register 19G bits 15:14 = 00.
- Set register 23 (main register) bit 12 = 0.
- Set register 18G = 0x80F0. For more information, see [Table 2-49](#).

#### 1.1.3.2 Media Interface 1000BASE-X SFP Fiber (1000BASE-X Link Partner)

Use the following settings to configure the 1000BASE-X SFP fiber media interface.

- Set register 23 bits 10:8 = 010.
- Set register 0 bit 12 = 1 (enable autonegotiation).

#### 1.1.3.3 AMS Preference Setup

Use the following settings for the AMS preferences setup.

- Set register 23 bit 10 = 1 (enable AMS).
- Set register 23 bit 11 to the port preferences.

The media selected by AMS can be read from register 20E1 bits 7:6. For more information, see [Table 1-4](#).

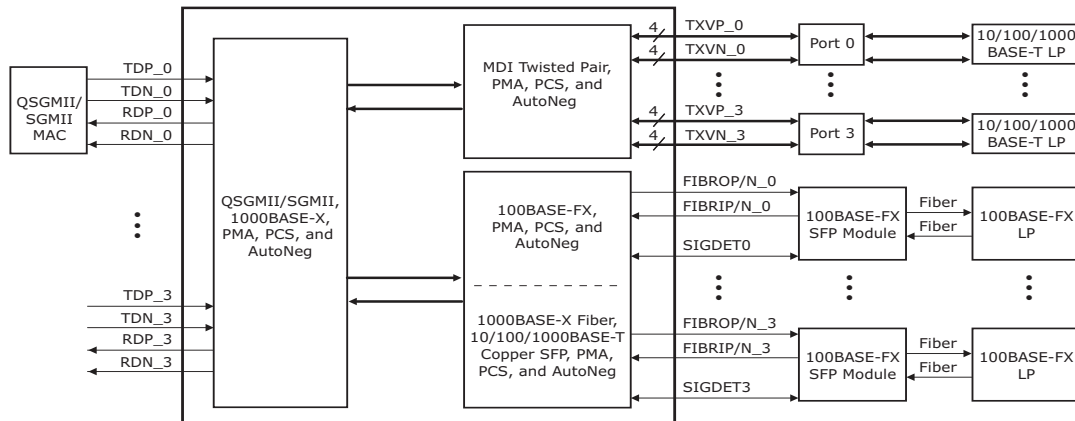
For QSGMII only port 0 is used.

**Note:** Whenever there is a mode change a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

#### 1.1.4 QSGMII/SGMII MAC-TO-AMS AND 100BASE-FX MEDIA SERDES

The following illustration and sections show the register settings used to configure a QSGMII/SGMII MAC-to-AMS and 100BASE-FX media SerDes.

**FIGURE 1-5: QSGMII/SGMII MAC-TO-AMS AND 100BASE-FX MEDIA SERDES**



## 1.1.4.1 MAC Interface SGMII

Use the following settings to configure the SGMII MAC interface.

- Set register 19G bits 15:14 = 00.
- Set register 23 (main register) bit 12 = 0.
- Set register 18G = 0x80F0. For more information, see [Table 2-49](#).

## 1.1.4.2 Media Interface 100BASE-FX SFP Fiber (100BASE-FX Link Partner)

Use the following settings to configure the 100BASE-FX SFP fiber media interface.

- Set register 23 bits 10:8 = 011.
- Set register 0 bit 12 = 1 (enable autonegotiation).

## 1.1.4.3 AMS Preference Setup

Use the following settings for the AMS preferences setup.

- Set register 23 bit 10 = 1 (enable AMS).
- Set register 23 bit 11 to the port preferences.

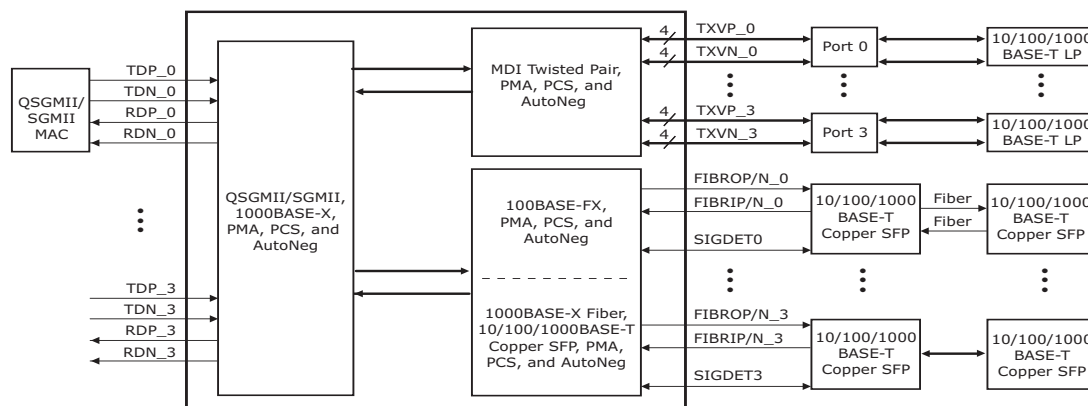
The media selected by AMS can be read from register 20E1 bits 7:6. For more information, see [Table 1-4](#).

For QSGMII only port 0 is used.

**Note:** Whenever there is a mode change a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

## 1.1.5 QSGMII/SGMII MAC-TO-AMS AND PROTOCOL TRANSFER MODE

The following illustration and sections show the register settings used to configure a QSGMII/SGMII MAC-to-AMS and Protocol Transfer mode.

**FIGURE 1-6: QSGMII/SGMII MAC-TO-AMS AND PROTOCOL TRANSFER MODE**

#### 1.1.5.1 MAC Interface SGMII

Use the following settings to configure the SGMII MAC interface.

- Set register 19G bits 15:14 = 00.
- Set register 23 (main register) bit 12 = 0.
- Set register 18G = 0x80F0. For more information, see [Table 2-49](#).

#### 1.1.5.2 Media Interface 10/100/1000BASE-T Cu-SFP

Use the following settings to configure the fiber/SFP media interface for protocol transfer mode.

- Set register 23 bits 10:8 = 001.
- Set register 0 bit 12 = 1 (enable autonegotiation).

#### 1.1.5.3 AMS Preference Setup

Use the following settings for the AMS preferences setup.

- Set register 23 bit 10 = 1 (enable AMS).
- Set register 23 bit 11 to the port preferences.

The media selected by AMS can be read from register 20E1 bits 7:6. For more information, see [Table 1-4](#).

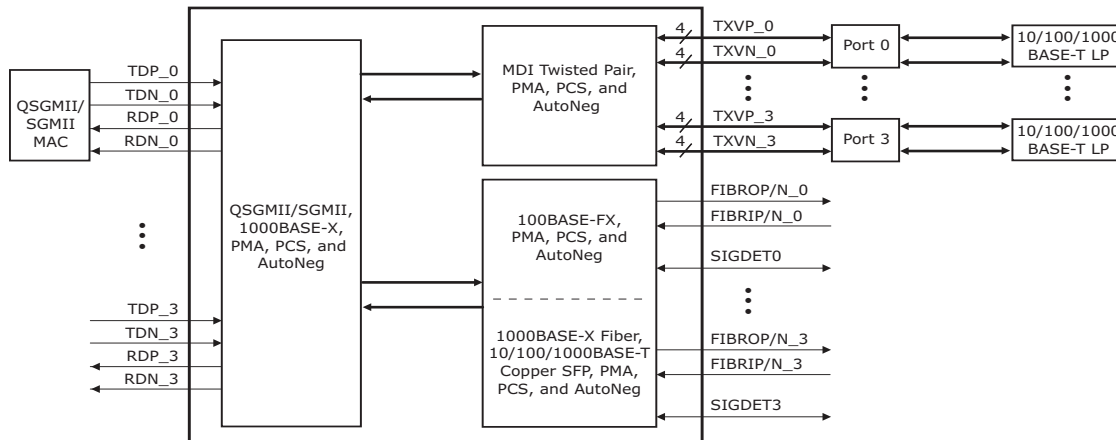
For QSGMII only port 0 is used.

**Note:** Whenever there is a mode change a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

#### 1.1.6 QSGMII/SGMII MAC-TO-CAT5 LINK PARTNER

The following illustration and sections show the register settings used to configure a QSGMII/SGMII MAC-to-Cat5 link partner.

**FIGURE 1-7: QSGMII/SGMII MAC-TO-CAT5 LINK PARTNER**



## 1.1.6.1 MAC Interface SGMII

Use the following settings to configure the SGMII MAC interface.

- Set register 19G bits 15:14 = 00.
- Set register 23 (main register) bit 12 = 0.
- Set register 18G = 0x80F0. For more information, see [Table 2-49](#).

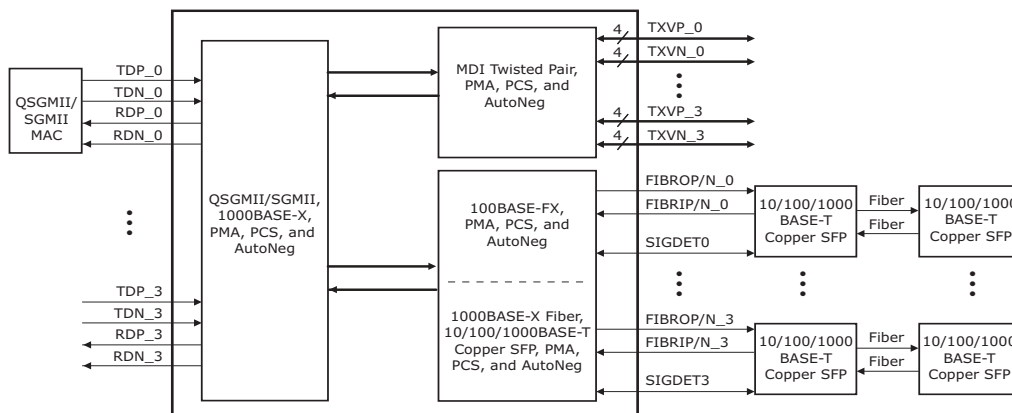
For QSGMII only port 0 is used.

**Note:** Whenever there is a mode change a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

## 1.1.7 QSGMII/SGMII MAC-TO-PROTOCOL TRANSFER MODE

The following illustration and sections show the register settings used to configure a QSGMII/SGMII MAC-to-Protocol Transfer mode.

**FIGURE 1-8: QSGMII/SGMII MAC-TO-PROTOCOL TRANSFER MODE**



## 1.1.7.1 MAC Interface SGMII

Use the following settings to configure the SGMII MAC interface.

- Set register 19G bits 15:14 = 00.
- Set register 23 (main register) bit 12 = 0.
- Set register 18G = 0x80F0. For more information, see [Table 2-49](#).

## 1.1.7.2 Media Interface 10/100/1000BASE-T Cu-SFP

Use the following settings to configure the fiber/SFP media interface for protocol transfer mode.

- Set register 23 bits 10:8 = 001.
- Set register 0 bit 12 = 1 (enable autonegotiation).

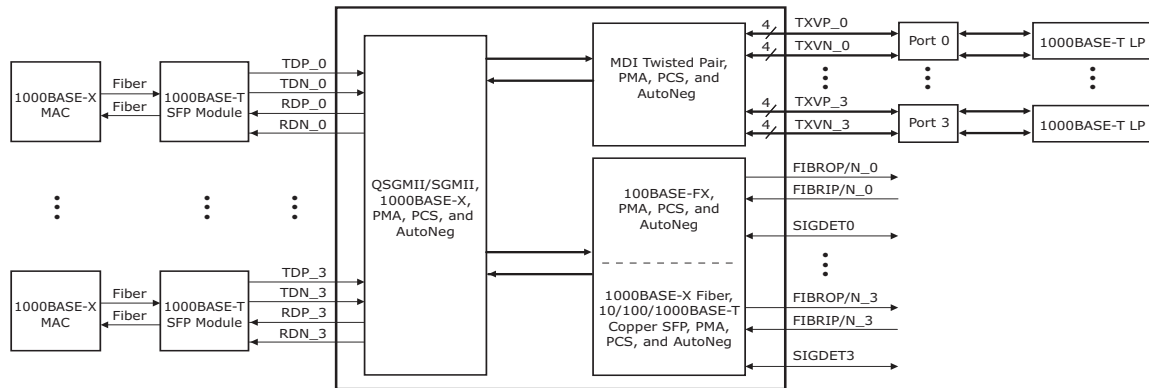
For QSGMII only port 0 is used.

**Note:** Whenever there is a mode change a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

## 1.1.8 1000BASE-X MAC-TO-CAT5 LINK PARTNER

The following illustration and sections show the register settings used to configure a 1000BASE-X MAC-to-Cat5 Link Partner.

**FIGURE 1-9: 1000BASE-X MAC-TO-CAT5 LINK PARTNER**



In this mode the device provides data throughput of 1000 Mbps only.

### 1.1.8.1 MAC Interface

Use the following settings to configure the MAC interface.

- Set register 19G bits 15:14 = 00.
- Set register 23 (main register) bit 12 = 1.

### 1.1.8.2 Clause 37 MAC Autonegotiation

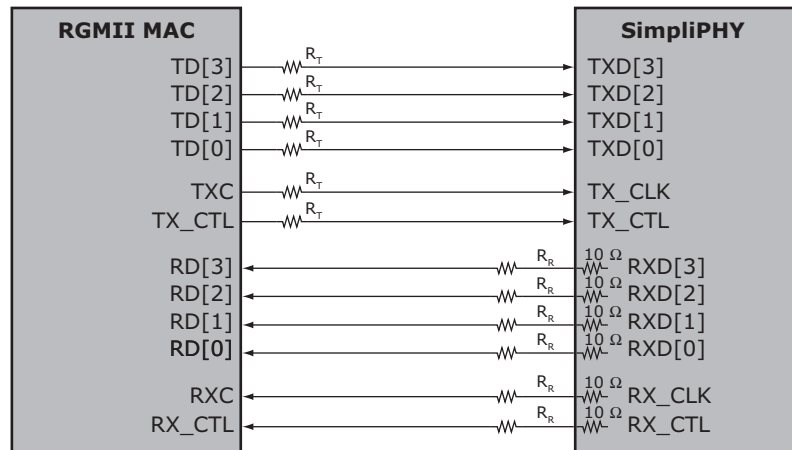
For clause 37 MAC autonegotiation, set register 16E3 bit 7 = 1.

**Note:** Whenever there is a mode change a software reset (register 0 bit 15) is required to make the mode change effective. This register is cleared when read.

## 1.2 RGMII MAC

The VSC8552 device supports RGMII versions 1.3 and 2.0 (2.5V). The RGMII interface supports all three speeds (10 Mbps, 100 Mbps, and 1000 Mbps) and is used as an interface to an RGMII-compatible MAC.

**FIGURE 1-10: RGMII MAC INTERFACE**



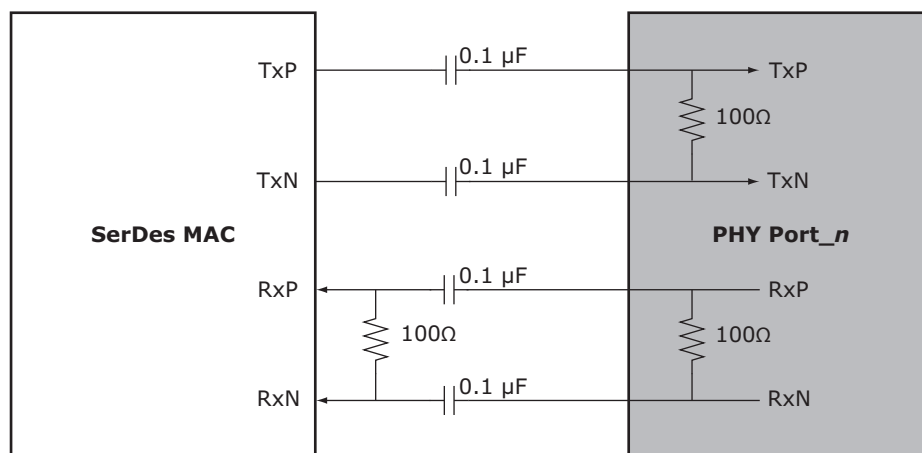
## 1.3 SerDes MAC Interface

The VSC8552 SerDes MAC interface performs data serialization and deserialization functions using an integrated SerDes block. The interface operates in 1000BASE-X compliant mode, QSGMII mode, or SGMII mode. The SerDes and enhanced SerDes blocks have the termination resistor integrated into the device. The SerDes block also has the AC decoupling capacitors integrated in the receive path. Integrated AC decoupling is not supported in the enhanced SerDes block (QSGMII SerDes). Register 19G is a global register and only needs to be set once to configure the device. The other register bits are configured on a per-port basis and the operation either needs to be repeated for each port, or a broadcast write needs to be used by setting register 22, bit 0 to configure all the ports simultaneously.

### 1.3.1 SERDES MAC

When connected to a SerDes MAC compliant to 1000BASE-X, the VSC8552 device provides data throughput at a rate of 1000 Mbps only; 10 Mbps and 100 Mbps rates are not supported. To configure the device for SerDes MAC mode, set register 19G, bits 15:14 = 0, and register 23, bit 12 = 1. The device also supports 1000BASE-X Clause 37 MAC-side autonegotiation and is enabled through register 16E3, bit 7. To configure the rest of the device for 1000 Mbps operation, select 1000BASE-T only by disabling the 10BASE-T/100BASE-TX advertisements in register 4.

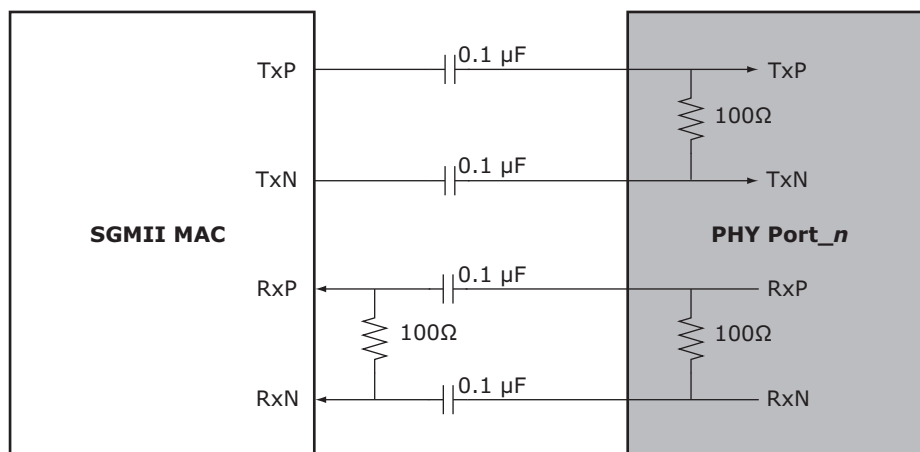
**FIGURE 1-11: SERDES MAC INTERFACE**



### 1.3.2 SGMII MAC

When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the VSC8552 device can be connected to an SGMII-compatible MAC. To configure the device for SGMII MAC mode, set register 19G, bits 15:14 = 00 and register 23, bit 12 = 0. In addition, set register 18G as desired. This device also supports SGMII MAC-side autonegotiation and is enabled through register 16E3, bit 7.

**FIGURE 1-12: SGMII MAC INTERFACE**

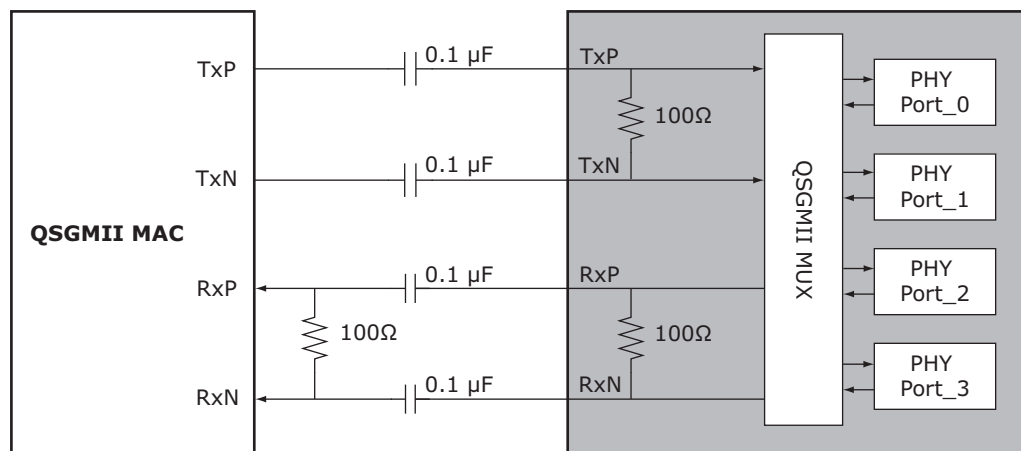


### 1.3.3 QSGMII MAC

The VSC8552 device supports a QSGMII MAC to convey two ports of network data and port speed between 10BASE-T, 100BASE-T, and 1000BASE-T data rates and operates in both half-duplex and full-duplex at all port speeds. The MAC interface protocol for each port within QSGMII can be either 1000BASE-X or SGMII, if the QSGMII MAC that the VSC8552 is connecting to supports this functionality. To configure the device for QSGMII MAC mode, set register 19G, bits 15:14 = 01. In addition, set register 18G as desired. The device also supports SGMII MAC-side autonegotiation on each individual port and is enabled through register 16E3, bit 7, of that port.

**Note:** Two of the four QSGMII channels contain data. The windows for the other two channels remain present and need to be supported in both directions by the MAC. This support is called “half QSGMII.”

**FIGURE 1-13: QSGMII MAC INTERFACE**



## 1.4 SerDes Media Interface

The VSC8552 device SerDes media interface performs data serialization and deserialization functions using an integrated SerDes block in the SerDes media interface. The interface operates at 1.25 Gbps speed, providing full-duplex and half-duplex for 10/100/1000 Mbps bandwidth that can connect directly to 100BASE-FX/1000BASE-X-compliant optical devices as well as to 10/100/1000BASE-T copper SFP devices. The interface also provides support for unidirectional transport as defined in IEEE 802.3-2008, Clause 66. The SerDes interface has the following operating modes:

- QSGMII/RGMII/SGMII to 1000BASE-X
- QSGMII/RGMII/SGMII to 100BASE-FX
- QSGMII/RGMII/SGMII to SGMII/1000BASE-X protocol transfer

The SerDes media block has the termination resistor integrated into the device. It also has the AC decoupling capacitors integrated in the receive path.

A software reset through register 0, bit 15 is required when changing operating modes between 100BASE-FX and 1000BASE-X.

## 1.4.1 QSGMII/RGMII/SGMII TO 1000BASE-X

The 1000BASE-X SerDes media in QSGMII/RGMII/SGMII mode supports IEEE 802.3 Clause 36 and Clause 37, which describe 1000BASE-X fiber autonegotiation. In this mode, control and status of the SerDes media is displayed in the VSC8552 device registers 0 through 15 in a manner similar to what is described in IEEE 802.3 Clause 28. In this mode, connected copper SFPs can only operate at 1000BASE-T speed. A link in this mode is established using autonegotiation (enabled or disabled) between the PHY and the link partner. To configure the PHY in this mode, set register 23, bits 10:8 = 010. To configure 1000BASE-X autonegotiation for this mode, set register 0, bit 12. Setting this mode and configurations can be performed individually on each of the two ports. Ethernet packet generator (EPG), cyclical redundancy check (CRC) counters, and loopback modes are supported in 1000BASE-X mode.

## 1.4.2 QSGMII/RGMII/SGMII TO 100BASE-FX

The VSC8552 supports 100BASE-FX communication speed for connecting to fiber modules such as GBICs and SFPs. This capability is facilitated by using the connections on the SerDes pins when connected to a MAC through QSGMII/RGMII/SGMII. Ethernet packet generator (EPG), cyclical redundancy check (CRC) counters, and loopback modes are supported in the 100BASE-FX mode. Setting this mode and configurations can be performed individually on each of the two ports. To configure the PHY in this mode, set register 23, bits 10:8 = 011.

## 1.4.3 QSGMII TO SGMII PROTOCOL CONVERSION

QSGMII to SGMII (protocol transfer) mode is a feature that links a fiber module or triple speed 10/100/1000-T copper SFP to the QSGMII MAC through the VSC8552 device. SGMII can be converted to QSGMII with protocol conversion using this mode.

To configure the PHY in this mode, set register 23, bits 10:8 = 001. To establish the link, assert the relevant signal-detect pin.

All relevant LED modes are supported except for collision, duplex, and autonegotiation fault. The triple-speed copper SFP's link status and data type plugged into the port can be indicated by the PHY's LEDs. Setting this particular mode and configuration can be performed individually on each of the two ports within a QSGMII grouping.

## 1.4.4 UNIDIRECTIONAL TRANSPORT FOR FIBER MEDIA

The VSC8552 device supports IEEE 802.3ah for unidirectional transport across its 1000BASE-X and 100BASE-FX fiber media. This feature enables transmission across fiber media, regardless of whether the PHY has determined that a valid link has been established (register 1, bit 2). The only valid operating modes for unidirectional fiber mode are 100BASE-FX or 1000BASE-X fiber media.

To enable this feature, set register 0, bit 5 to 1. For status of the unidirectional ability, read register 1, bit 7.

**Note:** Automatic media sensing does not work with this feature. In addition, because unidirectional fiber media must have autonegotiation disabled, RGMII/SGMII autonegotiation must also be disabled (register 16E3, bit 7 = 0).

## 1.5 PHY Addressing and Port Mapping

This section contains information about PHY addressing and port mapping.

### 1.5.1 PHY ADDRESSING

The VSC8552 includes three external PHY address pins, PHYADD[4:2], to allow control of multiple PHY devices on a system board sharing a common management bus. These pins set the most significant bits of the PHY address port map. The lower two bits of the address for each port are derived from the physical address of the port (0 to 1) and the setting of the PHY address reversal bit in register 20E1, bit 9.

The VSC8552 includes seven 1.25 GHz SerDes macros and one 5 GHz enhanced SerDes macro. Three of the seven SerDes macros are configured as SGMII MAC interfaces and the remaining four are configured as 1000BASE-X/100BASE-FX SerDes media interfaces. The enhanced SerDes macro can be configured as either a QSGMII MAC interface or the fourth SGMII MAC interface. The following table shows the different operating modes based on the settings of register 19G, bits 15:14.

| 19G[15:14] | Operating Mode |
|------------|----------------|
| 00         | SGMII          |
| 01         | QSGMII         |
| 10         | RGMII          |
| 11         | Reserved       |

The VSC8552 twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az-2010 standard for energy efficient Ethernet.

Unlike many other gigabit PHYs, the VSC8552 uses a patented voltage mode line driver that allows it to fully integrate the series termination resistors, which are required to connect the PHY's Cat5 interface to an external 1:1 transformer. Also, the interface does not require the user to place an external voltage on the center tap of the magnetic. The following illustration shows the connections.

## 1.6.2 CAT5 AUTONEGOTIATION AND PARALLEL DETECTION

The VSC8552 supports twisted pair autonegotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az-2010. The autonegotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, autonegotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-TX. Autonegotiation also enables a connected MAC to communicate with its link partner MAC through the VSC8552 using optional next pages, which set attributes that may not otherwise be defined by the IEEE standard.

If the Category 5 (Cat5) link partner does not support autonegotiation, the VSC8552 automatically uses parallel detection to select the appropriate link speed.

Autonegotiation is disabled by clearing register 0, bit 12. When autonegotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode.

**Note:** While 10BASE-T and 100BASE-TX do not require autonegotiation, Clause 40 has defined 1000BASE-T to require autonegotiation.

## 1.6.3 AUTOMATIC CROSSOVER AND POLARITY DETECTION

For trouble-free configuration and management of Ethernet links, the VSC8552 includes a robust automatic crossover detection feature for all three speeds on the twisted pair interface (10BASE-T, 100BASE-T, and 1000BASE T). Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs—a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

**Note:** The VSC8552 can be configured to perform HP Auto-MDIX, even when autonegotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To use the feature, also set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table, which shows that twisted pair A (of four twisted pairs A, B, C, and D) is connected to the RJ45 connector 1 and 2 in normal MDI mode.

**TABLE 1-3: SUPPORTED MDI PAIR COMBINATIONS**

| RJ45 Connections |      |      |      |                                             |
|------------------|------|------|------|---------------------------------------------|
| 1, 2             | 3, 6 | 4, 5 | 7, 8 | Mode                                        |
| A                | B    | C    | D    | Normal MDI                                  |
| B                | A    | D    | C    | Normal MDI-X                                |
| A                | B    | D    | C    | Normal MDI with pair swap on C and D pair   |
| B                | A    | C    | D    | Normal MDI-X with pair swap on C and D pair |

## 1.6.4 MANUAL HP AUTO-MDIX SETTING

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

## 1.6.5 LINK SPEED DOWNSHIFT

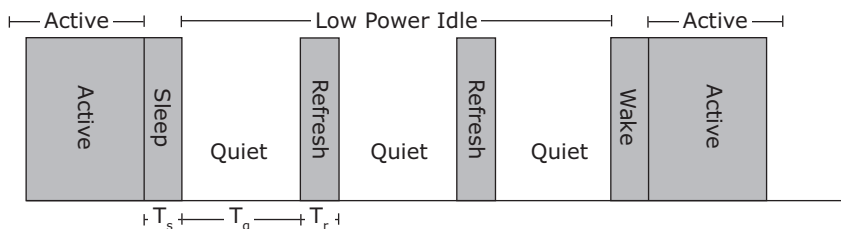
For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8552 provides an automatic link speed downshift option. When enabled, the device automatically changes its 1000BASE-T autonegotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state when a subsequent link partner with 1000BASE-T support is connected. This feature is useful in setting up in networks using older cable installations that include only pairs A and B, and not pairs C and D.

To configure and monitor link speed downshifting, set register 20E1, bits 4:1. For more information, see [Table 2-14](#).

### 1.6.6 ENERGY EFFICIENT ETHERNET

The VSC8552 supports the IEEE 802.3az-2010 Energy Efficient Ethernet standard. This standard provides a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low power idles (LPI) to achieve this objective.

**FIGURE 1-15: LOW POWER IDLE OPERATION**



Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization.

The VSC8552 uses LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T modes of operation. In addition, the IEEE 802.3az-2010 standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5V peak-to-peak to approximately 3.3V peak-to-peak. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T compliant PHYs over 100m Cat5 cable or better.

To configure the VSC8552 in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional energy efficient Ethernet features are controlled through Clause 45 registers. For more information, see [Section 6.0, Design Considerations](#).

### 1.6.7 RING RESILIENCY

Ring resiliency changes the timing reference between the master and slave PHYs without altering the master/slave configuration in 1000BASE-T mode. The master PHY transmitter sends data based on the local clock and initiates timing recovery in the receiver. The slave PHY instructs node to switch the local timing reference to the recovered clock from other PHYs in the box, freezes timing recovery, and locks clock frequency for the transmitter. The master PHY makes a smooth transition to transmission from local clock to recovered clock after timing lock is achieved.

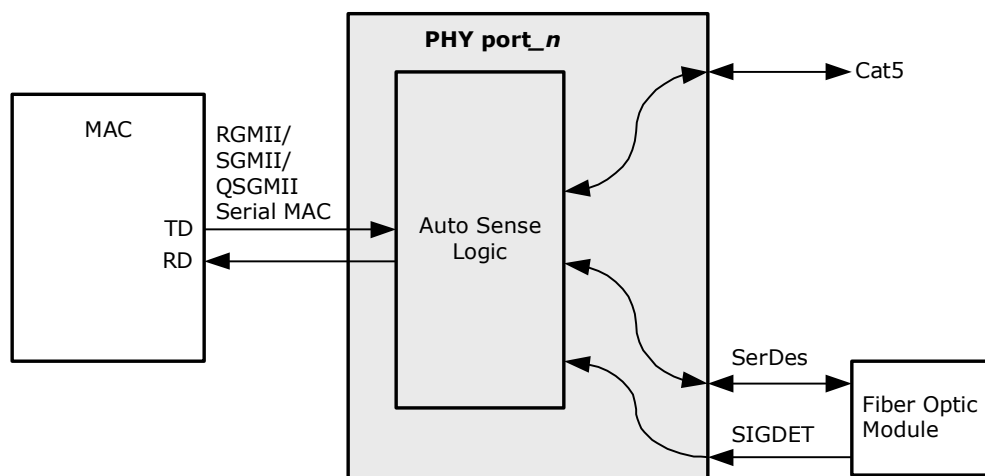
Ring resiliency can be used in synchronous Ethernet systems, because the local clocks in each node are synchronized to a grandmaster clock.

**Note:** For ring resiliency to successfully exchange master/slave timing over 1000BASE-T, the link partner must also support ring resiliency.

## 1.7 Automatic Media Sense Interface Mode

Automatic media sense (AMS) mode automatically sets the media interface to Cat5 mode or SerDes mode. The active media mode chosen is based on the automatic media sense preferences set in the device register 23, bit 11. The following illustration shows a block diagram of AMS functionality on ports 0 through 3 of the VSC8552 device.

**FIGURE 1-16: AUTOMATIC MEDIA SENSE BLOCK DIAGRAM**



When both the SerDes and Cat5 media interfaces attempt to establish a link, the preferred media interface overrides a linkup of the nonpreferred media interface. For example, if the preference is set for SerDes mode and Cat5 media establishes a link, Cat5 becomes the active media interface. However, after the SerDes media interface establishes a link, the Cat5 interface drops its link because the preference was set for SerDes mode. In this scenario, the SerDes preference determines the active media source until the SerDes link is lost. Also, Cat5 media cannot link up unless there is no SerDes media link established. The following table shows the possible link conditions based on preference settings.

**TABLE 1-4: AMS MEDIA PREFERENCES**

| Preference Setting | Cat5 Linked, Fiber Not Linked | SerDes Linked, Cat5 Not Linked | Cat5 Linked, SerDes Attempts to Link | SerDes Linked, Cat5 Attempts to Link | Both Cat5 and SerDes Attempt to Link |
|--------------------|-------------------------------|--------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|
| SerDes             | Cat5                          | SerDes                         | SerDes                               | SerDes                               | SerDes                               |
| Cat5               | Cat5                          | SerDes                         | Cat5                                 | Cat5                                 | Cat5                                 |

The status of the media mode selected by the AMS can be read from device register 20E1, bits 7:6. It indicates whether copper media, SerDes media, or no media is selected. Each PHY has four automatic media sense modes. The difference between the modes is based on the SerDes media modes:

- SGMII or QSGMII MAC to AMS and 100BASE-X SerDes
- SGMII or QSGMII MAC to AMS and 100BASE-FX SerDes
- SGMII or QSGMII MAC to AMS and SGMII (protocol transfer)

For more information about SerDes media mode functionality with AMS enabled, see [Section 1.4, SerDes Media Interface](#).

## 1.8 Reference Clock

The device reference clock supports both 25 MHz and 125 MHz clock signals. The reference clock can be either differential or single-ended. If differential, it must be capacitively coupled and LVDS compatible.

### 1.8.1 CONFIGURING THE REFERENCE CLOCK

The REFCLK\_SEL2 pin configures the reference clock speed. The following table shows the functionality and associated reference clock frequency.

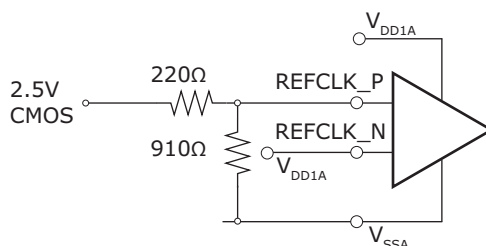
**TABLE 1-5: REFCLK FREQUENCY SELECTION**

| REFCLK_SEL2 | Frequency |
|-------------|-----------|
| 0           | 25 MHz    |
| 1           | 125 MHz   |

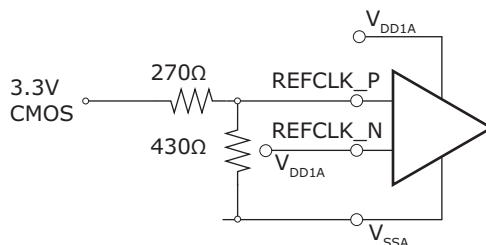
### 1.8.2 SINGLE-ENDED REFCLK INPUT

To use a single-ended reference clock, an external resistor network is required. The purpose of the network is to limit the amplitude and to adjust the center of the swing. The configurations for a single-ended REFCLK, with the clock centered at 1V and a 500 mV peak-to-peak swing, are shown in the following illustrations.

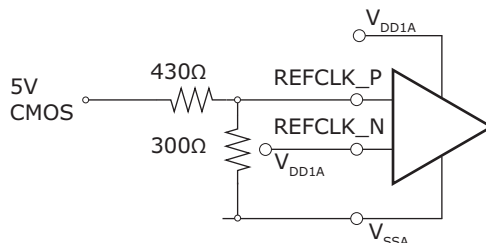
**FIGURE 1-17: 2.5V CMOS SINGLE-ENDED REFCLK INPUT RESISTOR NETWORK**



**FIGURE 1-18: 3.3V CMOS SINGLE-ENDED REFCLK INPUT RESISTOR NETWORK**



**FIGURE 1-19: 5V CMOS SINGLE-ENDED REFCLK INPUT RESISTOR NETWORK**

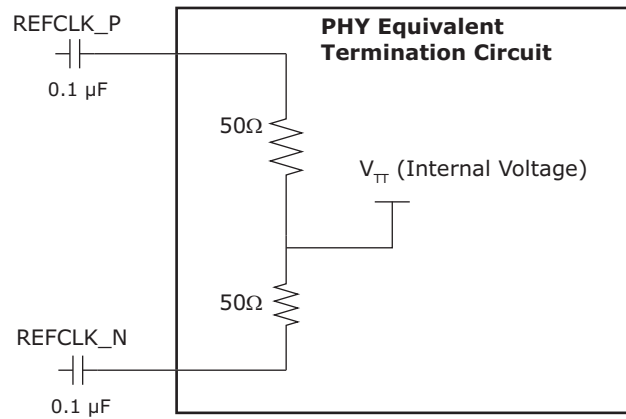


**Note:** A single-ended 25 MHz reference clock is not guaranteed to meet requirements for QSGMII MAC operation.

### 1.8.3 DIFFERENTIAL REFCLK INPUT

AC coupling is required when using a differential REFCLK. Differential clocks must be capacitively coupled and LVDS compatible. The following illustration shows the configuration.

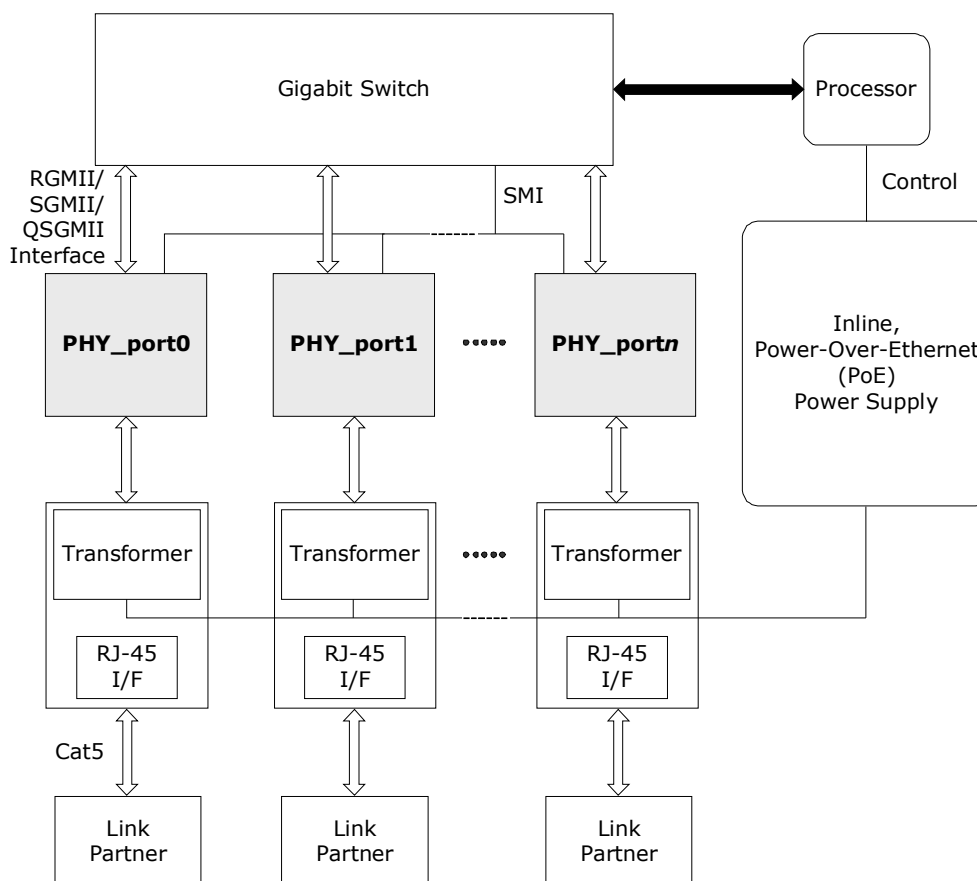
FIGURE 1-20: AC COUPLING FOR REFCLK INPUT



## 1.8.4 ETHERNET INLINE POWERED DEVICES

The VSC8552 can detect legacy inline powered devices in Ethernet network applications. Inline powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline powered device to remain active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptable power source.

For more information about legacy inline powered device detection, visit the Cisco Web site at [www.cisco.com](http://www.cisco.com). The following illustration shows an example of an inline powered Ethernet switch application.

**FIGURE 1-21: INLINE POWERED ETHERNET SWITCH DIAGRAM**

The following procedure describes the process that an Ethernet switch must perform to process inline power requests made by a link partner (LP) that is, in turn, capable of receiving inline power:

1. Enable the inline powered device detection mode on each VSC8552 PHY using its serial management interface. Set register bit 23E1.10 to 1.
2. Ensure that the VSC8552 autonegotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special fast link pulse (FLP) signal to the LP. Reading register bit 23E1.9:8 returns 00 during the search for devices that require power over Ethernet (PoE).
3. The VSC8552 PHY monitors its inputs for the FLP signal looped back by the LP. An LP capable of receiving PoE loops back the FLP pulses when the LP is in a powered down state. This is reported when VSC8552 register bit 23E1.9:8 reads back 01. It can also be verified as an inline power detection interrupt by reading VSC8552 register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read. When an LP device does not loop back the FLP after a specific time, VSC8552 register bit 23E1.9:8 automatically resets to 10.
4. If the VSC8552 PHY reports that the LP requires PoE, the Ethernet switch must enable inline power on this port, externally of the PHY.
5. The PHY automatically disables inline powered device detection when the VSC8552 register bits 23E1.9:8 automatically reset to 10, and then automatically changes to its normal autonegotiation process. A link is then autonegotiated and established when the link status bit is set (register bit 1.2 is set to 1).
6. In the event of a link failure (indicated when VSC8552 register bit 1.2 reads 0), it is recommended that the inline power be disabled to the inline powered device external to the PHY. The VSC8552 PHY disables its normal autonegotiation process and re-enables its inline powered device detection mode.

## 1.9 IEEE 802.3af PoE Support

The VSC8552 device is compatible with designs that are intended for use in systems that supply power to data terminal equipment (DTE) by means of the MDI or twisted pair cable, as described in IEEE 802.3af Clause 33.

## 1.10 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the device also includes an ActiPHY power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY wakes up at a programmable interval and attempts to wake up the link partner PHY by sending a burst of FLP over copper media.

The ActiPHY power management mode in the VSC8552 is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

The following operating states are possible when ActiPHY mode is enabled:

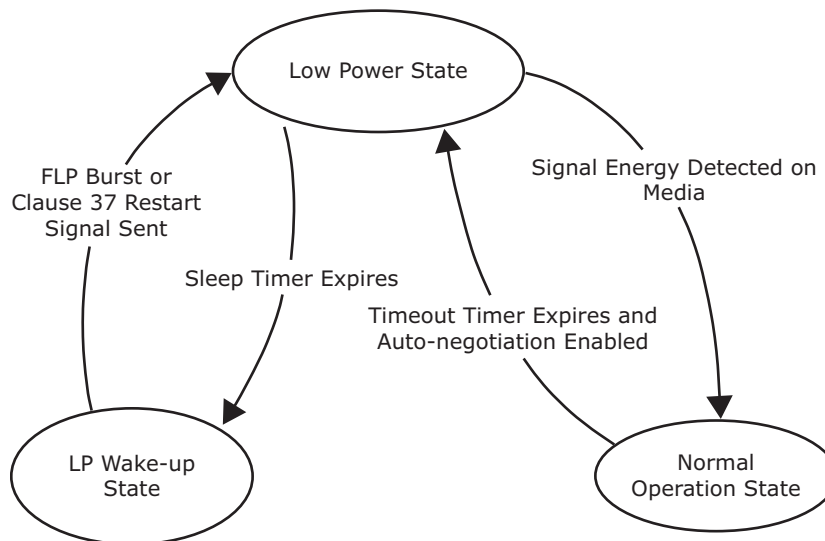
- Low power state
- Link partner wake-up state
- Normal operating state (link-up state)

The VSC8552 switches between the low power state and LP wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When autonegotiation is enabled in the PHY, the ActiPHY state machine operates as described. When autonegotiation is disabled and the link is forced to use 10BASE-T or 100BASE-TX modes while the PHY is in its low power state, the PHY continues to transition between the low power and LP wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. When autonegotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

**FIGURE 1-22: ACTIPHY STATE DIAGRAM**



### 1.10.1 LOW POWER STATE

In the low power state, all major digital blocks are powered down. However, the SMI interface (MDC, MDIO, and MDINT) functionality is provided.

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Autonegotiation-capable link partner
- Another PHY in enhanced ActiPHY LP wake-up state

In the absence of signal energy on the media pins, the PHY periodically transitions from low-power state to LP wake-up state, based on the programmable sleep timer (register bits 20E1.14:13). The actual sleep time duration is randomized from –80 ms to 60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

### 1.10.2 LINK PARTNER WAKE-UP STATE

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete FLP bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

In this state, SMI interface (MDC, MDIO, and MDINT) functionality is provided.

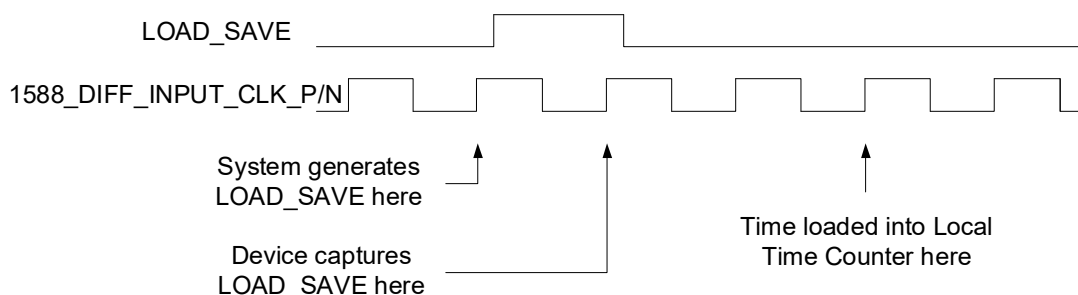
After sending signal energy on the relevant media, the PHY returns to the low power state.

### 1.10.3 NORMAL OPERATING STATE

In the normal operating state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

When the 1588\_DIFF\_INPUT\_CLK\_P/N pins are the clock source for the local time counter, and the LOAD\_SAVE strobe is synchronous to 1588\_DIFF\_INPUT\_CLK\_P/N, the LTC\_LOAD\* registers are loaded into the local time counter, as shown in the following illustration.

**FIGURE 1-23: LOCAL TIME COUNTER LOAD/SAVE TIMING**



## 1.11 Media Recovered Clock Outputs

For Synchronous Ethernet applications, the VSC8552 includes two recovered clock output pins, `RCVRDCLK1` and `RCVRDCLK2`, controlled by registers 23G and 24G, respectively. The recovered clock pins are synchronized to the clock of the active media link.

To enable recovered clock output, set register 23G or 24G, bit 15, to 1. By default, the recovered clock output pins are disabled and held low, including when `NRESET` is asserted. Registers 23G and 24G also control the PHY port for clock output, the clock source, the clock frequency (either 25 MHz, 31.25 MHz, or 125 MHz), and squelch conditions.

**Note:** When `EEE` is enabled on a link, the use of the recovered clock output is not recommended due to long hold-overs occurring during `EEE` Quiet/Refresh cycles.

### 1.11.1 CLOCK SELECTION SETTINGS

On each pin, the recovered clock supports the following sources, as set by registers 23G or 24G, bits 2:0:

- Fiber SerDes media recovered clock
- Copper PHY recovered clock
- Copper PHY media transmitter `TCLK` output (`RCVRDCLK1` only.) For more information, see [Table 2-54](#) and [Table 2-55](#).

**Note:** When using the automatic media sense feature, the recovered clock output cannot automatically change between each active media. Changing the media source must be managed through the recovered clock register settings.

Adjust the squelch level to enable 1000BASE-T master mode recovered clock for SyncE operation. This is accomplished by changing the 23G and 24G register bits 5:4 to 01. This setting also provides clock out for 10BASE-T operation. For 1000BASE-T master mode, the clock is based on the VSC8552 `REFCLK` input, which is a local clock.

## 1.11.2 CLOCK OUTPUT SQUELCH

Under certain conditions, the PHY outputs a clock based on the REFCLK\_P and REFCLK\_N pins, such as when there is no link present or during autonegotiation. To prevent an undesirable clock from appearing on the recovered clock pins, the VSC8552 squelches, or inhibits, the clock output based on any of the following criteria:

- No link is detected (the link status register 1, bit 2 = 0). In fiber media modes, sync status is required to unsquelch the recovered clock output instead of link status.
- The link is found to be unstable using the fast link failure detection feature. The GPIO9/FASTLINK-FAIL pin is asserted high when enabled.
- The active link is in 10BASE-T or in 1000BASE-T master mode. These modes produce unreliable recovered clock sources.
- CLK\_SQUELCH\_IN is enabled to squelch the clock.

Use registers 23G or 24G, bits 5:4 to configure the clock squelch criteria. These registers can also disable the squelch feature. The CLK\_SQUELCH\_IN pin controls the squelching of the clock. Both RCVRDCLK1 and RCVRDCLK2 are squelched when the CLK\_SQUELCH\_IN pin is high.

## 1.12 Serial Management Interface

The VSC8552 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.

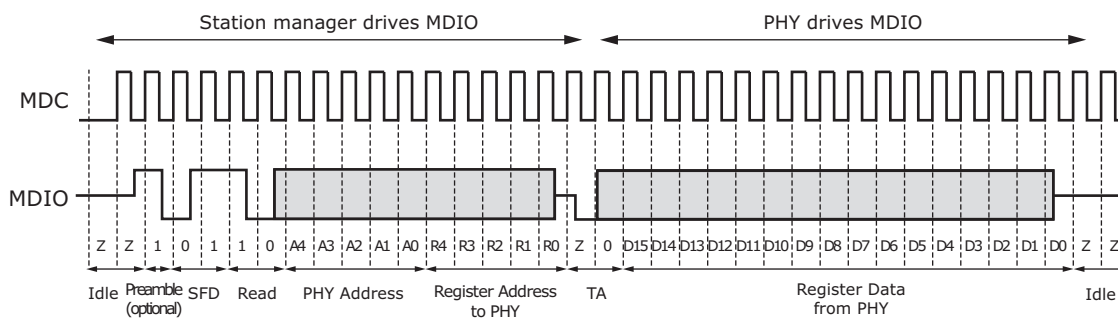
Energy efficient Ethernet control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14. For more information, see [Table 1-7](#) and [Table 2-58](#).

The SMI is a synchronous serial interface with input data to the VSC8552 on the MDIO pin that is clocked on the rising edge of the MDC pin. The output data is sent on the MDIO pin on the rising edge of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2-k $\Omega$  pull-up resistor is required on the MDIO pin.

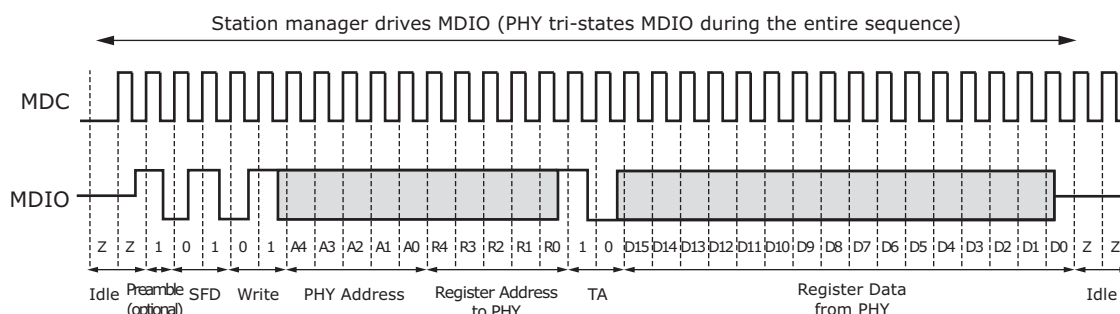
### 1.12.1 SMI FRAMES

Data is transferred over the SMI using 32-bit frames with an optional, arbitrary-length preamble. Before the first frame can be sent, at least two clock pulses on MDC must be provided with the MDIO signal at logic one to initialize the SMI state machine. The following illustrations show the SMI frame format for read and write operations.

**FIGURE 1-24: SMI READ FRAME**



**FIGURE 1-25: SMI WRITE FRAME**



The following list provides additional information about the terms used in the SMI read and write timing diagrams.

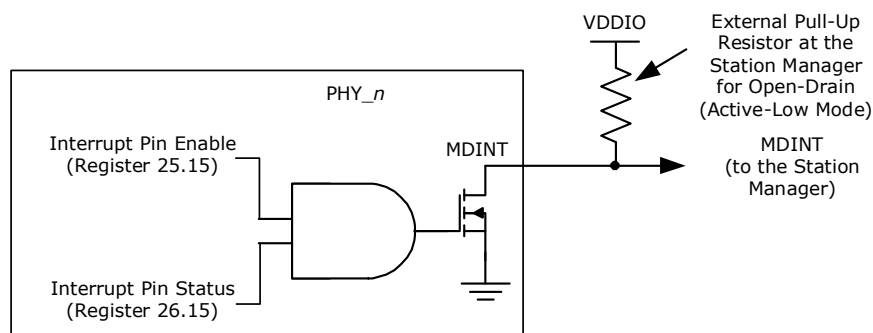
- **Idle**—During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode does not contain any transitions on MDIO, the number of bits is undefined during idle.
- **Preamble**—By default, preambles are not expected or required. The preamble is a string of ones. If it exists, the preamble must be at least 1 bit; otherwise, it can be of an arbitrary length.
- **Start of Frame (SFD)**—A pattern of 01 indicates the start of frame. If the pattern is not 01, all following bits are ignored until the next preamble pattern is detected.
- **Read or Write Opcode**—A pattern of 10 indicates a read. A 01 pattern indicates a write. If the bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.
- **PHY Address**—The particular VSC8552 responds to a message frame only when the received PHY address matches its physical address. The physical address is 5 bits long (4:0).
- **Register Address**—The next five bits are the register address.
- **Turnaround**—The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turnaround (TA) bits. During read operations, the VSC8552 drives the second TA bit, a logical 0.
- **Data**—The 16-bits read from or written to the device are considered the data or data stream. When data is read from a PHY, it is valid at the output from one rising edge of MDC to the next rising edge of MDC. When data is written to the PHY, it must be valid around the rising edge of MDC.
- **Idle**—The sequence is repeated.

## 1.12.2 SMI INTERRUPT

The SMI includes an output interrupt signal, MDINT, for signaling the station manager when certain events occur in the VSC8552.

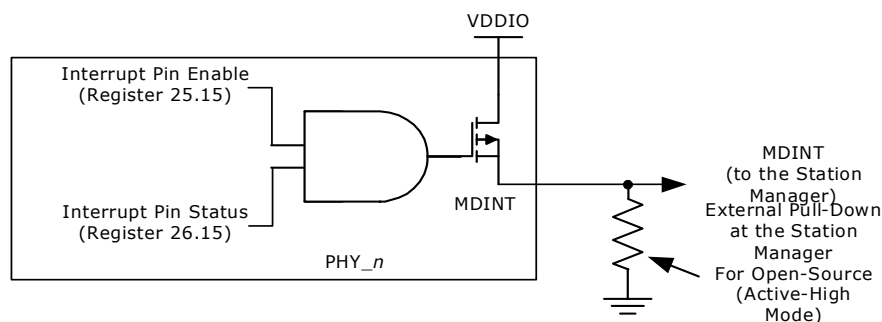
The MDINT pin can be configured for open-drain (active-low) by tying the pin to a pull-up resistor and to VDDIO. The following illustration shows this configuration.

**FIGURE 1-26: MDINT CONFIGURED AS AN OPEN-DRAIN (ACTIVE-LOW) PIN**



Alternatively, the MDINT pin can be configured for open-source (active-high) by tying the pin to a pull-down resistor and to VSS. The following illustration shows this configuration.

**FIGURE 1-27: MDINT CONFIGURED AS AN OPEN-SOURCE (ACTIVE-HIGH) PIN**



When a PHY generates an interrupt, the MDINT pin is asserted (driven high or low, depending on resistor connection) if the interrupt pin enable bit (MII register 25.15) is set.

## 1.13 LED Interface

The LED interface supports the following configurations: direct drive, basic serial LED mode, and enhanced serial LED mode. The polarity of the LED outputs is programmable and can be changed through register 17E2, bits 13:10. The default polarity is active low.

Direct drive mode provides four LED signals per port, LED0\_[0:3] through LED3\_[0:3]. The mode and function of each LED signal can be configured independently. When serial LED mode is enabled, the direct drive pins not used by the serial LED interface remain available.

In basic serial LED mode, all signals that can be displayed on LEDs are sent as LED\_Data and LED\_CLK for external processing. In enhanced serial LED mode, up to four LED signals per port can be sent as LED\_Data, LED\_CLK, LED\_LD, and LED\_Pulse. The following sections provide detailed information about the various LED modes.

**Note:** LED number is listed using the convention, LED<LED#>\_<Port#>.

The following table shows the bit 9 settings for register 14G that are used to control the LED behavior for all the LEDs in VSC8552.

**Note:** Enhanced serial LED mode will use the  $V_{DD}$  LED drive state (alternate setting), regardless of the setting in register 14G.9.

**TABLE 1-6: LED DRIVE STATE**

| Setting                       | Active | Not Active |
|-------------------------------|--------|------------|
| 14G.9 = 1 (default)           | Ground | Tristate   |
| 14G.9 = 0 (alternate setting) | Ground | $V_{DD}$   |

### 1.13.1 LED MODES

Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. The modes listed in the following table are equivalent to the setting used in register 29 to configure each LED pin. The default LED state is active low and can be changed by modifying the value in register 17E2, bits 13:10. The blink/pulse-stretch is dependent on the LED behavior setting in register 30.

The following table provides a summary of the LED modes and functions.

**TABLE 1-7: LED MODE AND FUNCTION SUMMARY**

| Mode | Function Name                        | LED State and Description                                                                                                                                                                                                                         |
|------|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0    | Link/Activity                        | 1: No link in any speed on any media interface.<br>0: Valid link at any speed on any media interface.<br>Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.                                           |
| 1    | Link1000/Activity                    | 1: No link in 1000BASE-T or 1000BASE-X.<br>0: Valid 1000BASE-T or 1000BASE-X.<br>Blink or pulse-stretch = Valid 1000BASE-T or 1000BASE-X link with activity present.                                                                              |
| 2    | Link100/Activity                     | 1: No link in 100BASE-TX or 100BASE-FX.<br>0: Valid 100BASE-TX or 100BASE-FX.<br>Blink or pulse-stretch = Valid 100BASE-TX or 100BASE-FX link with activity present.                                                                              |
| 3    | Link10/Activity                      | 1: No link in 10BASE-T.<br>0: Valid 10BASE-T link.<br>Blink or pulse-stretch = Valid 10BASE-T link with activity present.                                                                                                                         |
| 4    | Link100/1000/Activity                | 1: No link in 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T.<br>0: Valid 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T link. Blink or pulse-stretch = Valid 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T link with activity present. |
| 5    | Link10/1000/Activity                 | 1: No link in 10BASE-T, 1000BASE-X, or 1000BASE-T.<br>0: Valid 10BASE-T, 1000BASE-X, or 1000BASE-T link.<br>Blink or pulse-stretch = Valid 10BASE-T, 1000BASE-X, or 1000BASE-T link with activity present.                                        |
| 6    | Link10/100/Activity                  | 1: No link in 10BASE-T, 100BASE-FX, or 100BASE-TX.<br>0: Valid 10BASE-T, 100BASE-FX, or 100BASE-TX link.<br>Blink or pulse-stretch = Valid 10BASE-T, 100BASE-FX, or 100BASE-TX link with activity present.                                        |
| 7    | Link100BASE-FX/1000BASE-X/Activity   | 1: No link in 100BASE-FX or 1000BASE-X.<br>0: Valid 100BASE-FX or 1000BASE-X link.<br>Blink or pulse-stretch = Valid 100BASE-FX or 1000BASE-X link with activity present.                                                                         |
| 8    | Duplex/Collision                     | 1: Link established in half-duplex mode, or no link established.<br>0: Link established in full-duplex mode.<br>Blink or pulse-stretch = Link established in half-duplex mode but collisions are present.                                         |
| 9    | Collision                            | 1: No collision detected.<br>Blink or pulse-stretch = Collision detected.                                                                                                                                                                         |
| 10   | Activity                             | 1: No activity present.<br>Blink or pulse-stretch = Activity present (becomes TX activity present when register bit 30.14 is set to 1).                                                                                                           |
| 11   | 100BASE-FX/1000BASE-X Fiber Activity | 1: No 100BASE-FX or 1000BASE-X activity present.<br>Blink or pulse-stretch = 100BASE-FX or 1000BASE-X activity present (becomes RX activity present when register bit 30.14 is set to 1).                                                         |

**TABLE 1-7: LED MODE AND FUNCTION SUMMARY (CONTINUED)**

| Mode | Function Name         | LED State and Description                                                                                                         |
|------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 12   | Autonegotiation Fault | 1: No autonegotiation fault present.<br>0: Autonegotiation fault occurred.                                                        |
| 13   | Serial Mode           | Serial stream. See <a href="#">Section 1.13.4, Basic Serial LED Mode</a> .<br>Only relevant on PHY port 0 and reserved in others. |
| 14   | Force LED Off         | 1: De-asserts the LED <sup>1</sup> .                                                                                              |
| 15   | Force LED On          | 0: Asserts the LED <sup>1</sup> .                                                                                                 |

1. Setting this mode suppresses LED blinking after reset.

## 1.13.2 EXTENDED LED MODES

In addition to the LED modes in register 29, there are also additional LED modes that are enabled on the LED0\_[1:0] pins whenever the corresponding register 19E1, bits 15 to 12 are set to 1. Each of these bits enables extended modes on a specific LED pin and these extended modes are shown in the following table. For example, LED0 = mode 17 means that register 19E1 bit 12 = 1 and register 29 bits 3 to 0 = 0001.

The following table provides a summary of the extended LED modes and functions.

**TABLE 1-8: EXTENDED LED MODE AND FUNCTION SUMMARY**

| Mode | Function Name           | LED State and Description                                                                   |
|------|-------------------------|---------------------------------------------------------------------------------------------|
| 16   | Link1000BASE-X Activity | 1: No link in 1000BASE-X.<br>0: Valid 1000BASE-X link.                                      |
| 17   | Link100BASE-FX Activity | 1: No link in 100BASE-FX.<br>0: Valid 100BASE-FX link.                                      |
| 18   | 1000BASE-X Activity     | 1: No 1000BASE-X activity present.<br>Blink or pulse-stretch = 1000BASE-X activity present. |
| 19   | 100BASE-FX Activity     | 1: No 100BASE-FX activity present.<br>Blink or pulse-stretch = 100BASE-FX activity present. |
| 20   | Force LED Off           | 1: De-asserts the LED.                                                                      |
| 21   | Force LED On            | 0: Asserts the LED. LED pulsing is disabled in this mode.                                   |
| 22   | Fast Link Fail          | 1: Enable fast link fail on the LED pin<br>0: Disable                                       |

## 1.13.3 LED BEHAVIOR

Several LED behaviors can be programmed into the VSC8552. Use the settings in register 30 and 19E1 to program LED behavior, which includes the following.

### 1.13.3.1 LED Combine

Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 1000BASE-T mode and activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display when the combine feature is disabled.

### 1.13.3.2 LED Blink or Pulse-Stretch

This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin. Activity and collision events can occur randomly and intermittently throughout the link-up period. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin. Pulse-stretch guarantees that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

### 1.13.3.3 Rate of LED Blink or Pulse-Stretch

This behavior controls the LED blink rate or pulse-stretch length when blink/pulse-stretch is enabled on an LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.

### 1.13.3.4 LED Pulsing Enable

To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz with a programmable duty cycle through register 25G bits 15:8. For duty cycle details, see [Table 2-77](#).

### 1.13.3.5 LED Blink After Reset

The LEDs will blink for one second after power-up and after any time all resets have been de-asserted. This can be disabled through register 19E1, bit 11 = 0.

### 1.13.3.6 Fiber LED Disable

This bit controls whether the LEDs indicate the fiber and copper status (default) or the copper status only.

### 1.13.3.7 Pulse Programmable Control

These bits add the ability to width and frequency of LED pulses. This feature facilitates power reduction options.

### 1.13.3.8 Fast Link Failure

For more information about this feature, see [Section 1.14, Fast Link Failure Indication](#).

## 1.13.4 BASIC SERIAL LED MODE

Optionally, the VSC8552 can be configured so that access to all its LED signals is available through two pins. This option is enabled by setting LED0 on PHY0 to serial LED mode in register 29, bits 7:0 to 0xDD. When setting 3:0 to 0xD on the serial data signal is enabled, setting 7:4 to 0xD enables the serial clock. When serial LED mode is enabled, the LED0\_0 pin becomes the serial data pin, and the LED1\_0 pin becomes the serial clock pin. All other LED pins can still be configured normally. The serial LED mode clocks the 48 LED status bits on the rising edge of the serial clock where bits 25:48 are ignored.

The LED behavior settings can also be used in serial LED mode. The controls are used on a per-PHY basis, where the LED combine and LED blink or pulse-stretch setting of LED0\_n for each PHY is used to control the behavior of each bit of the serial LED stream for each corresponding PHY. To configure LED behavior, set device register 30.

The following table shows the 48-bit serial output bitstream of each LED signal where bits 25:48 are ignored. The individual signals can be clocked in the following order.

**TABLE 1-9: LED SERIAL BITSTREAM ORDER**

| Output              | PHY0 | PHY1 |
|---------------------|------|------|
| Link/activity       | 1    | 13   |
| Link1000/activity   | 2    | 14   |
| Link100/activity    | 3    | 15   |
| Link10/activity     | 4    | 16   |
| Fiber link/activity | 5    | 17   |
| Duplex/collision    | 6    | 18   |
| Collision           | 7    | 19   |

**TABLE 1-9: LED SERIAL BITSTREAM ORDER (CONTINUED)**

| Output                | PHY0 | PHY1 |
|-----------------------|------|------|
| Activity              | 8    | 20   |
| Fiber activity        | 9    | 21   |
| Tx activity           | 10   | 22   |
| Rx activity           | 11   | 23   |
| Autonegotiation fault | 12   | 24   |

**TABLE 1-10: ENHANCED SERIAL LED MODE**

VSC8552 can be configured to output up to four LED signals per port on a serial stream that can be de-serialized externally to drive LEDs on the system board. In enhanced serial LED mode, the port 0 and port 1 LED output pins serve the following functions:

- LED0\_0/LED0\_1: LED\_DATA
- LED1\_0/LED1\_1: LED\_CLK
- LED2\_0/LED2\_1: LED\_LD
- LED3\_0/LED3\_1: LED\_PULSE

The serial LED\_DATA is shifted out on the falling edge of LED\_CLK and is latched in the external serial-to-parallel converter on the rising edge of LED\_CLK. The falling edge of LED\_LD signal can be used to shift the data from the shift register in the converter to the parallel output drive register. When a separate parallel output drive register is not used in the external serial-to-parallel converter, the LEDs will blink at a high frequency as the data bits are being shifted through, which may be undesirable. LED pin functionality is controlled by setting register 25G, bits 7:1.

The LED\_PULSE signal provides a 5 kHz pulse stream whose duty cycle can be modulated to turn on/off LEDs at a high rate. This signal can be tied to the output enable signal of the serial-to-parallel converter to provide the LED dimming functionality to save energy. The LED\_PULSE duty cycle is controlled by setting register 25G, bits 15:8.

### 1.13.5 LED PORT SWAPPING

For additional hardware configurations, the VSC8552 can have its LED port order swapped. This is a useful feature to help simplify PCB layout design. Register 25G bit 0 controls the LED port swapping mode.

**Note:** LED port swapping only applies to the parallel LED outputs and does not affect the serial LED outputs.

## 1.14 Fast Link Failure Indication

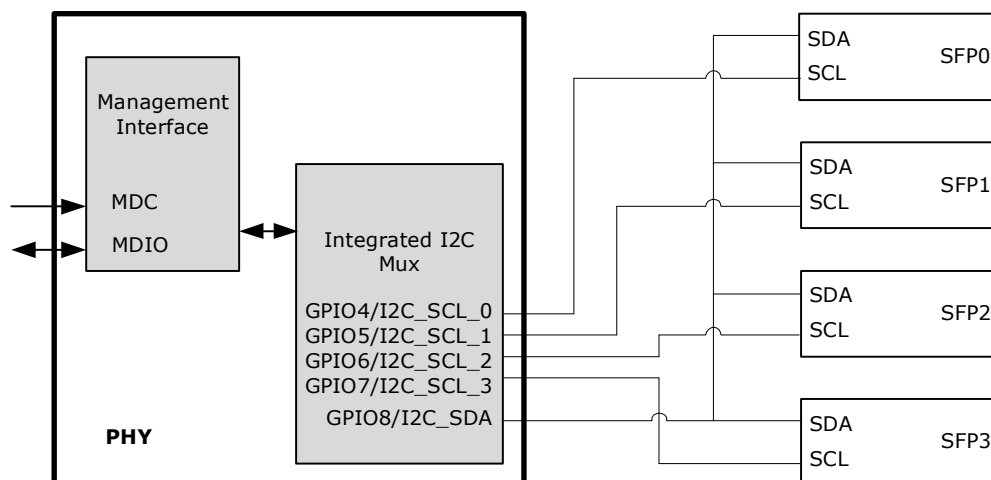
To aid Synchronous Ethernet applications, the VSC8552 can indicate the onset of a link failure in less than 1 ms (worst-case <3 ms). By comparison, the IEEE 802.3 standard establishes a delay of up to 750 ms before indicating that a 1000BASE-T link is no longer present. A fast link failure indication is critical to support ports used in a synchronization timing link application. The fast link failure indication works for all copper media speeds, but not for fiber media. Fast link failure is supported for each PHY port through the GPIO9/FASTLINK-FAIL pin. For details on how to use the FAST-LINK-FAIL pin, see [Table 2-35](#) and [Table 2-71](#).

**Note:** For all links except 1000BASE-T, the fast link failure indication matches the link status register (address 1, bit 2). For 1000BASE-T links, the link failure is based on a circuit that analyzes the integrity of the link, and at the indication of failure, will assert.

**Note:** The Fast Link Failure Indication should not be used when EEE is enabled on a link.

## 1.15 Integrated Two-Wire Serial Multiplexer

The VSC8552 includes an integrated dual two-wire serial multiplexer (MUX), eliminating the need for an external two-wire serial device for the control and status of SFP or PoE modules. There are three two-wire serial controller pins: two clocks and one shared data pin. Each SFP or PoE connects to the multipurpose GPIO[5:4]\_I2C\_SCL\_[1:0] and GPIO8/I2C\_SDA device pins, which must be configured to the corresponding two-wire serial function. For more information about configuring the pins, see [Section 2.6.9, Two-Wire Serial MUX Control 1](#). For SFP modules, VSC8552 can also provide control for the MODULE\_DETECT and TX\_DIS module pins using the multipurpose LED and GPIO pins.

**FIGURE 1-28: TWO-WIRE SERIAL MUX WITH SFP CONTROL AND STATUS**

### 1.15.1 READ/WRITE ACCESS USING THE TWO-WIRE SERIAL MUX

Using the integrated two-wire serial MUX, the VSC8552 device can read and write to an SFP or PoE module through the SCL and SDA pins. If the ability is required to write to the slave two-wire serial device, refer to the device's specific datasheet for more information.

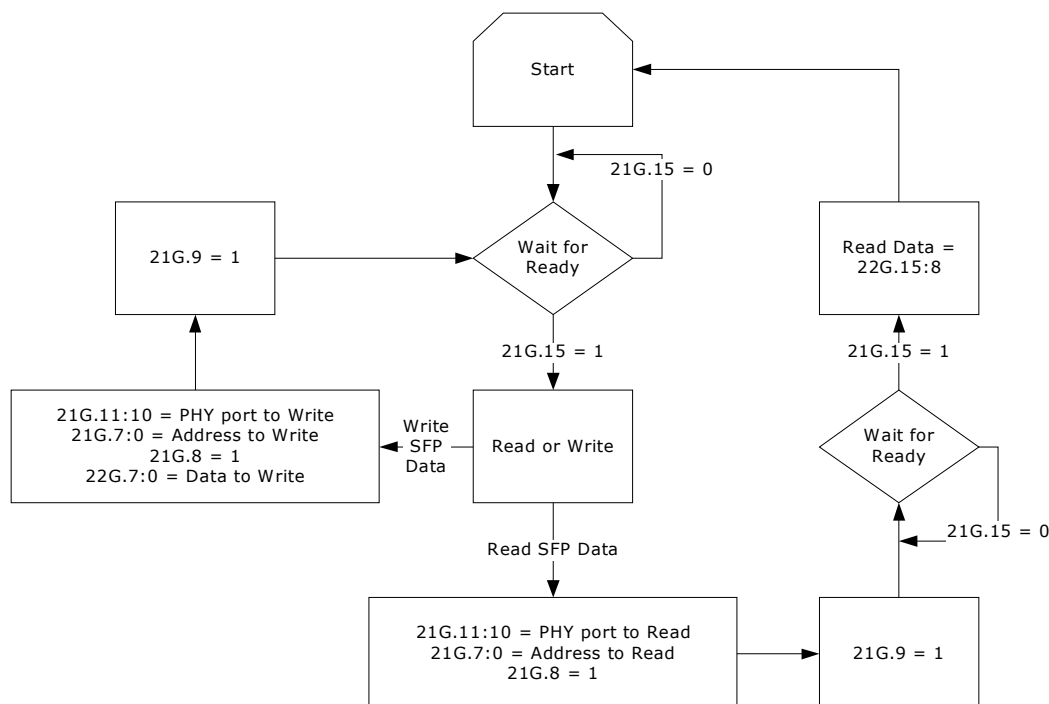
**Note:** The VSC8552 device does not automatically increment the two-wire serial address. Each desired address must be intentionally set.

Main control of the integrated two-wire serial MUX is available through register 20G. The two-wire serial MUX pins are enabled or disabled using register 20G bits 3:0. Register 20G bits 15:9 set the two-wire serial device address (the default is 0xA0). Using register 20G bits 5:4, the two-wire serial frequency can be changed from 100 kHz to other speeds, such as 50 kHz, 100 kHz (the default), 400 kHz, and 2 MHz.

**Note:** The frequencies listed are available when the PHY API is used.

Registers 21G and 22G provide status and control of the read/write process. The following illustration shows the read and write register flow.

**FIGURE 1-29: TWO-WIRE SERIAL MUX READ AND WRITE REGISTER FLOW**



To read a value from a specific address of the two-wire serial slave device:

1. Read the VSC8552 device register 21G bit 15, and ensure that it is set.
2. Write the PHY port address to be read to register 21G bits 11:10.
3. Write the two-wire serial address to be read to register 21G bits 7:0.
4. Set both register 21G bits 8 and 9 to 1.
5. When register 21G bit 15 changes to 1, read the 8-bit data value found at register 22G bits 15:8. This is the contents of the address just read by the PHY.

To write a value to a specific address of the two-wire serial slave device:

1. Read the VSC8552 device register 21G bit 15 and ensure that it is set.
2. Write the PHY port address to be written to register 21G bits 11:10.
3. Write the address to be written to register 21G bits 7:0.
4. Set register 21 bit 8 to 0.
5. Set register 22G bits 7:0 with the 8-bit value to be written to the slave device.
6. Set register 21G bit 9 to 1.

To avoid collisions during read and write transactions on the two-wire serial bus, always wait until register 21G bit 15 changes to 1 before performing another two-wire serial read or write operation.

## 1.16 GPIO Pins

The VSC8552 provides 14 multiplexed general purpose input/output (GPIO) pins. All device GPIO pins and their behavior are controlled using registers. The following table shows an overview of the register controls for GPIO pins. For more information, see [Section 2.6, General Purpose Registers](#).

**TABLE 1-11: REGISTER BITS FOR GPIO CONTROL AND STATUS**

| GPIO Pin        | GPIO_ctrl | GPIO Input | GPIO Output | GPIO Output Enable |
|-----------------|-----------|------------|-------------|--------------------|
| GPIO0/SIGDET0   | 13G.1:0   | 15G.0      | 16G.0       | 17G.0              |
| GPIO1/SIGDET1   | 13G.3:2   | 15G.1      | 16G.1       | 17G.1              |
| GPIO4/I2C_SCL_0 | 13G.9:8   | 15G.4      | 16G.4       | 17G.4              |

**TABLE 1-11: REGISTER BITS FOR GPIO CONTROL AND STATUS (CONTINUED)**

| GPIO Pin            | GPIO_ctrl | GPIO Input | GPIO Output | GPIO Output Enable |
|---------------------|-----------|------------|-------------|--------------------|
| GPIO5/I2C_SCL_1     | 13G.11:10 | 15G.5      | 16G.5       | 17G.5              |
| GPIO8/I2C_SDA       | 14G.1:0   | 15G.8      | 16G.8       | 17G.8              |
| GPIO9/FASTLINK_FAIL | 14G.3:2   | 15G.9      | 16G.9       | 17G.9              |

## 1.17 Testing Features

The VSC8552 device includes several testing features designed to facilitate performing system-level debugging and in-system production testing. This section describes the available features.

### 1.17.1 ETHERNET PACKET GENERATOR

The Ethernet packet generator (EPG) can be used at each of the 10/100/1000BASE-T speed settings for copper Cat5 media and fiber media to isolate problems between the MAC and the VSC8552, or between a locally connected PHY and its remote link partner. Enabling the EPG feature effectively disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface. This feature is not used when the SerDes media is set to pass-through mode.

**Important** The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the VSC8552 is connected to a live network.

To enable the VSC8552 EPG feature, set the device register bit 29E1.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output pins to the MAC are still active when the EPG is enabled. When it is necessary to disable the MAC receive pins as well, set the register bit 0.10 to 1.

When the device register bit 29E1.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E1 and 30E1. These registers set:

- Source and destination addresses for each packet
- Packet size
- Interpacket gap
- FCS state
- Transmit duration
- Payload pattern

When register bit 29E1.13 is set to 0, register bit 29E1.14 is cleared automatically after 30,000,000 packets are transmitted.

### 1.17.2 CRC COUNTERS

Two sets of cyclical redundancy check (CRC) counters are available in all PHYs in VSC8552. One set monitors traffic on the copper interface and the other set monitors traffic on the SerDes interface.

The device CRC counters operate in the 100BASE-FX/1000BASE-X over SerDes mode as well as in the 10/100/1000BASE-T mode as follows:

After receiving a packet on the media interface, register bit 15 in register 18E1 or register 28E3 is set and cleared after being read.

The packet then is counted by either the good CRC counter or the bad CRC counter.

Both CRC counters are also automatically cleared when read.

The good CRC counter's highest value is 9,999 packets. After this value is reached, the counter clears on the 10,000<sup>th</sup> packet and continues to count additional packets beyond that value. The bad CRC counter stops counting when it reaches its maximum counter limit of 255 packets.

#### 1.17.2.1 Copper Interface CRC Counters

Two separate CRC counters are available and reside between the copper interface PCSs and SerDes MAC interface. There is a 14-bit good CRC counter available through register bits 18E1.13:0 and a separate 8-bit bad CRC counter available in register bits 23E1.7:0.

## 1.17.2.2 SerDes Interface CRC Counters

Two separate CRC counters are available and reside between the SerDes media interface PCSs and SerDes MAC interface. There is a 14-bit good CRC counter available through register bits 28E3.13:0 and a separate 8-bit bad CRC counter available in register bits 29E3.7:0.

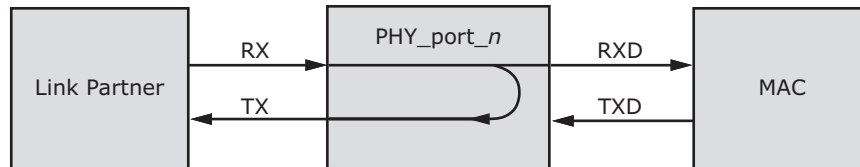
## 1.17.2.3 SerDes Fiber Media Transmit Counters

Two fiber media transmit counters are available to verify packets being transmitted on the fiber media. Register bits 21E3.13:0 are the good CRC packet counters and register bits 22E3.7:0 are the CRC error counters.

## 1.17.3 FAR-END LOOPBACK

The far-end loopback testing feature is enabled by setting register bit 23.3 to 1. When enabled, it forces incoming data from a link partner on the current media interface, into the MAC interface of the PHY, to be retransmitted back to the link partner on the media interface as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

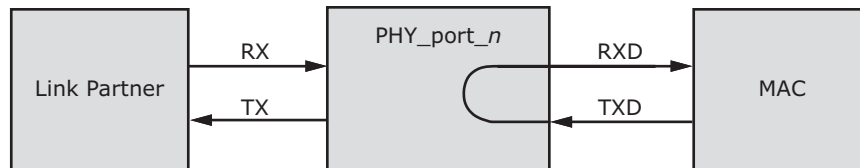
**FIGURE 1-30: FAR-END LOOPBACK DIAGRAM**



## 1.17.4 NEAR-END LOOPBACK

When the near-end loopback testing feature is enabled, transmitted data (TXD) is looped back in the PCS block onto the receive data signals (RXD), as shown in the following illustration. When using this testing feature, no data is transmitted over the network. To enable near-end loopback, set the device register bit 0.14 to 1.

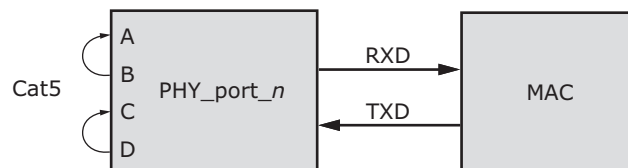
**FIGURE 1-31: NEAR-END LOOPBACK DIAGRAM**



## 1.17.5 CONNECTOR LOOPBACK

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Connect pair A to pair B, and pair C to pair D, as shown in the following illustration. The connector loopback feature functions at all available interface speeds.

**FIGURE 1-32: CONNECTOR LOOPBACK DIAGRAM**



When using the connector loopback testing feature, the device autonegotiation, speed, and duplex configuration is set using device registers 0, 4, and 9. For 1000BASE-T connector loopback, the following additional writes are required. Execute the additional writes in the following order:

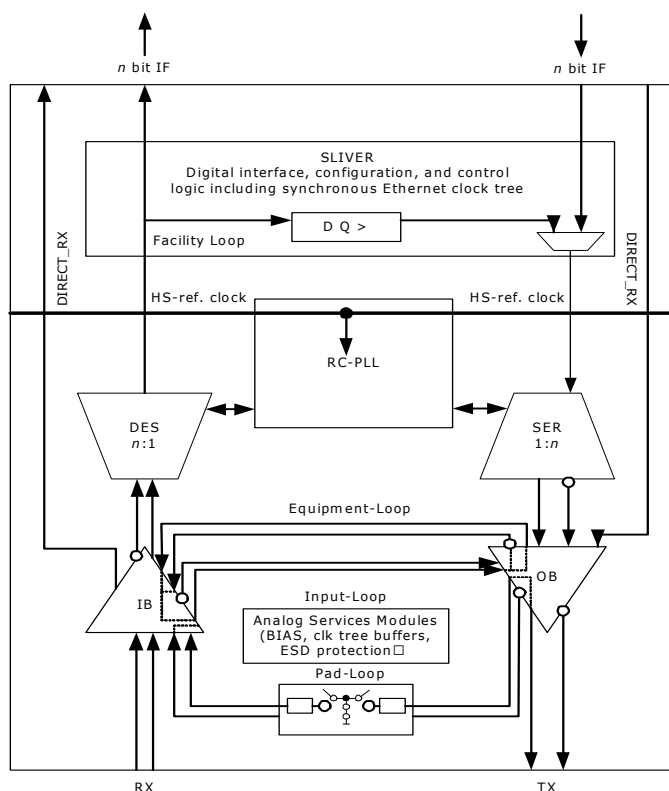
1. Enable the 1000BASE-T connector loopback. Set register bit 24.0 to 1.

2. Disable pair swap correction. Set register bit 18.5 to 1.

### 1.17.6 SERDES LOOPBACKS

For test purposes, the SerDes and SerDes macro interfaces provides several data loops. The following illustration shows the SerDes loopbacks.

**FIGURE 1-33: DATA LOOPS OF THE SERDES MACRO**



#### 1.17.6.1 RGMII/SGMII Mode

When the MAC interface is configured in RGMII/SGMII mode, write the following 16-bit value to register 18G:

- Bits 15:12 0x9
- Bits 11:8: Port address (0x0 to 0x3)
- Bits 7:4: Loopback type
- Bits 3:0: 0x2

where loopback type is:

- 0x0: No loopback
- 0x2: Input loopback
- 0x4: Facility loopback
- 0x8: Equipment loopback

#### 1.17.6.2 QSGMII Mode

When the MAC interface is configured in QSGMII mode, write the following 16-bit value to register 18G:

- Bits 15:12 0x9
- Bits 11:8: Port address (0x0)
- Bits 7:4: Loopback type
- Bits 3:0: 0x2

where loopback type is:

- 0x0: No loopback
- 0x2: Input loopback
- 0x4: Facility loopback
- 0x8: Equipment loopback

**Note:** Loopback configuration affects all ports associated with a QSGMII. Individual port loopback within a QSGMII is not possible.

### 1.17.6.3 Fiber Media Port Mode

When the SerDes is configured as a fiber media port, write the following 16-bit value to register 18G:

- Bits 15:12: 0x8
- Bits 11:8: Port address
- Bits 7:4: Loopback type
- Bits 3:0: 0x2

where port address is:

- 0x1: Fiber0 port
- 0x2: Fiber1 port
- 0x4: Fiber2 port
- 0x8: Fiber3 port

Port addresses for fiber media SerDes can be OR'ed together to address multiple ports using a single command. bit 18G.15 will be cleared when the internal configuration is complete.

### 1.17.6.4 Facility Loop

The recovered and de-multiplexer deserializer data output is looped back to the serializer data input and replaces the data delivered by the digital core. This test loop provides the possibility to test the complete analog macro data path from outside including input buffer, clock and data recovery, serialization and output buffer. The data received by the input buffer must be transmitted by the output buffer after some delay.

Additional configuration of the macro is required for facility loopback mode. When entering facility loopback mode, the set = 1 option should be run; when exiting facility loopback mode, the set = 0 option should be run.

```
PhyWrite(PhyBaseAddr, 31, 0x0010);
PhyWrite(PhyBaseAddr, 18, 0x8s03);
// where "s" is the physical address of the SerDes macro
PhyWrite(PhyBaseAddr, 18, 0xd7cb);
PhyWrite(PhyBaseAddr, 18, 0x8007);
tmp1 = PhyRead(PhyBaseAddr, 18);
tmp2 = tmp1 & 0x0ff0;
if (set)
    tmp3 = tmp2 | 0x0010;
else
    tmp3 = tmp2 & 0x0fe0;
tmp4 = tmp3 | 0x8006;
PhyWrite(PhyBaseAddr, 18, tmp4);
if (SGMII)
    PhyWrite(PhyBaseAddr, 18, 0x9p40);
// where "p" is the logical address of the SGMII interface
else
    PhyWrite(PhyBaseAddr, 18, 0x8p40);
// where "p" is the logical address of the Fiber media interface
// PhyBaseAddr is the 5-bit base address of the internal PHYs.
// The upper 3 bits are set by the PHYADD[4:2] pins and the
// lower 2 bits are 0.
```

Additional configuration of the enhanced SerDes macro is required for facility loopback mode. When entering facility loopback mode, the set = 1 option should be run; when exiting facility loopback mode, the set = 0 option should be run.

```
PhyWrite(PhyBaseAddr, 31, 0x0010);
PhyWrite(PhyBaseAddr, 18, 0x8013);
PhyWrite(PhyBaseAddr, 18, 0xd7cb);
PhyWrite(PhyBaseAddr, 18, 0x8007);
```

```

tmp1 = PhyRead(PhyBaseAddr, 18);
tmp2 = tmp1 & 0x0ff0;
if (set)
    tmp3 = tmp2 | 0x0100;
else
    tmp3 = tmp2 & 0x0ef0;
tmp4 = tmp3 | 0x8006;
PhyWrite(PhyBaseAddr, 18, tmp4);
PhyWrite(PhyBaseAddr, 18, 0x9c40);
// PhyBaseAddr is the 5-bit base address of the internal PHYs.
// The upper 3 bits are set by the PHYADD[4:2] pins and the
// lower 2 bits are 0.

```

#### 1.17.6.5 Equipment Loop

The 1-bit data stream at the serializer output is looped back to the deserializer and replaces the received data stream from the input buffer. This test loop provides the possibility to verify the digital data path internally. The transmit data goes through the serialization, the clock and data recovery and deserialization before the data is fed back to the digital core.

**Note:** After entering equipment loopback mode, the following workaround should be run with set = 1 option in case external signal is not present; when exiting equipment loopback mode, the set = 0 option should be run:

#### SGMII/QSGMII SerDes

```

PhyWrite(<phy>, 31, 0x52b5);
PhyWrite(<phy>, 16, 0xa68c);
tmp17 = PhyRead(<phy>, 17);
if (set)
    tmp17 |= 0x0010; //Set SigDet as desired, Set bit 4
else // clear SigDet
    tmp17 &= 0xffef; //Clear SigDet, bit 4
PhyWrite(<phy>, 17, tmp17);
PhyWrite(<phy>, 16, 0x868c);
PhyWrite(<phy>, 31, 0x0);

```

#### Fiber media SerDes

```

PhyWrite(<phy>, 31, 0x52b5);
PhyWrite(<phy>, 16, 0xa68a);
tmp17 = PhyRead(<phy>, 17);
if (set)
    tmp17 |= 0x0010; //Set SigDet as desired, Set bit 4
else // clear SigDet
    tmp17 &= 0xffef; //Clear SigDet, bit 4
PhyWrite(<phy>, 17, tmp17);
PhyWrite(<phy>, 16, 0x868a);
PhyWrite(<phy>, 31, 0x0);

```

#### 1.17.6.6 Input Loop

The received 1-bit data stream of the input buffer is looped back asynchronously to the output buffer. This test loop provides the possibility to test only the analog parts of the RGMII/SGMII interface because only the input and output buffer are part of this loop.

**Note:** When the enhanced SerDes macro is in input loopback, the output is inverted relative to the input.

The following table shows the SerDes macro address map.

**TABLE 1-12: SERDES MACRO ADDRESS MAP**

| SerDes Macro | Physical Address (s) | Interface Logical Type (p) | Address |
|--------------|----------------------|----------------------------|---------|
| SerDes0      | 0x0                  | Fiber0                     | 0x1     |
| SerDes1      | 0x1                  | SGMII1                     | 0x1     |
| SerDes2      | 0x2                  | Fiber1                     | 0x2     |
| SerDes3      | 0x3                  | SGMII2                     | 0x2     |

**TABLE 1-12: SERDES MACRO ADDRESS MAP (CONTINUED)**

| SerDes Macro | Physical Address (s) | Interface Logical Type (p) | Address |
|--------------|----------------------|----------------------------|---------|
| SerDes4      | 0x4                  | Fiber2                     | 0x4     |
| SerDes5      | 0x5                  | SGMII3                     | 0x3     |
| SerDes6      | 0x6                  | Fiber3                     | 0x8     |

## 1.17.7 VERIPHY CABLE DIAGNOSTICS

The VSC8552 includes a comprehensive suite of cable diagnostic functions that are available using SMI reads and writes. These functions enable a variety of cable operating conditions and status to be accessed and checked. The VeriPHY suite has the ability to identify the cable length and operating conditions and to isolate a variety of common faults that can occur on the Cat5 twisted pair cabling.

**Note:** When a link is established on the twisted pair interface in the 1000BASE-T mode, VeriPHY can run without disrupting the link or disrupting any data transfer. However, when a link is established in 100BASE-TX or 10BASE-T modes, VeriPHY causes the link to drop while the diagnostics are running. After diagnostics are finished, the link is re-established.

The following diagnostic functions are part of the VeriPHY suite:

- Detecting coupling between cable pairs
- Detecting cable pair termination
- Determining cable length

### 1.17.7.1 Coupling Between Cable Pairs

Shorted wires, improper termination, or high crosstalk resulting from an incorrect wire map can cause error conditions, such as anomalous coupling between cable pairs. These conditions can prevent the device from establishing a link in any speed.

### 1.17.7.2 Cable Pair Termination

Proper termination of Cat5 cable requires a 100  $\Omega$  differential impedance between the positive and negative cable terminals. IEEE 802.3 allows for a termination of 115  $\Omega$  maximum and 85  $\Omega$  minimum. VeriPHY diagnostics can report anomalous termination that falls outside of this range. The diagnostics can also determine the presence of an open or shorted cable pair.

### 1.17.7.3 Cable Length

When the Cat5 cable in an installation is properly terminated, VeriPHY reports the approximate cable length in meters. If there is a cable fault the distance to the fault is reported.

### 1.17.7.4 Mean Square Error Noise

The average absolute error can be read out when either a 100BASE-TX or 1000BASE-T link is established. In the case of 1000BASE-T link, there are two average absolute error terms, one for each twisted pair over which signal is received. Use the following script to read average absolute error for 100BASE-TX:

```
PhyWrite(<phy>, 31, 0x52b5);
PhyWrite(<phy>, 16, 0xa3c0);
PhyRead(<phy>, 16);
tmp17 = PhyRead(<phy>, 17);
tmp18 = PhyRead(<phy>, 18);
mse = (tmp18 << 4) | (tmp17 >> 12);
PhyWrite(<phy>, 31, 0);
```

The returned average absolute error is in units of 1/2,048 and can be found in the mse variable.

```
PhyWrite(<phy>, 31, 0x52b5);
PhyWrite(<phy>, 16, 0xa3c0);
PhyRead(<phy>, 16);
tmp17 = PhyRead(<phy>, 17);
tmp18 = PhyRead(<phy>, 18);
mseA = (tmp18 << 4) | (tmp17 >> 12);
mseB = tmp17 & 0x0fff;
```

```

PhyWrite(<phy>, 16, 0xa3c2);
PhyRead(<phy>, 16);
tmp17 = PhyRead(<phy>, 17);
tmp18 = PhyRead(<phy>, 18);
mseC = (tmp18 << 4) | (tmp17 >> 12);
mseD = tmp17 & 0x0fff;
PhyWrite(<phy>, 31, 0);

```

The returned average absolute error is in units of 1/2,048 and can be found in the mseA, mseB, mseC, and mseD variables for each twisted pair.

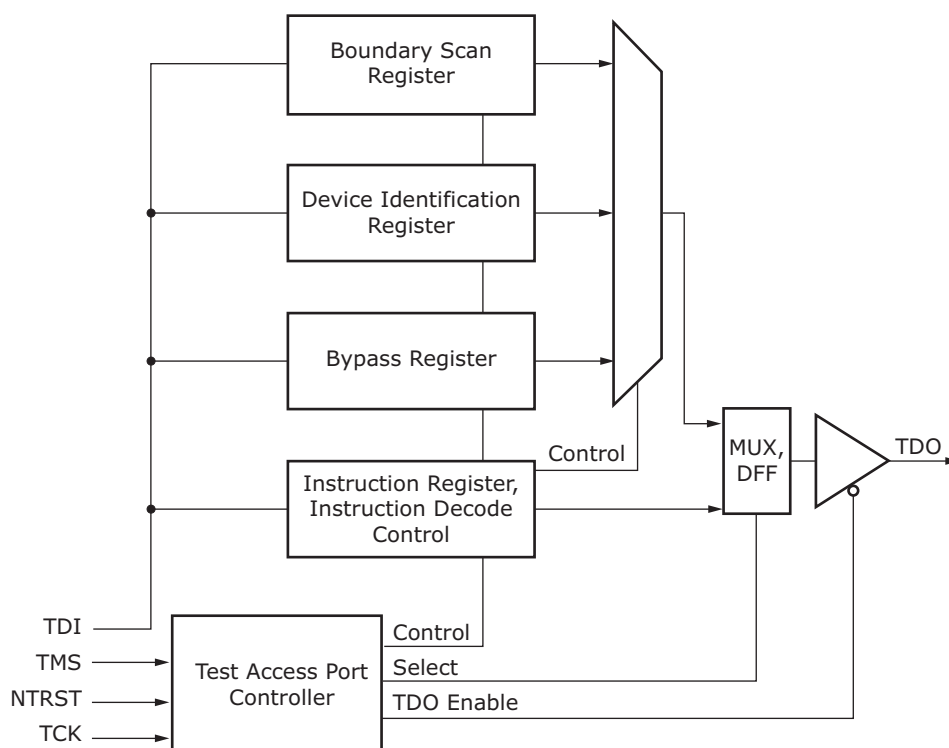
### 1.17.8 JTAG BOUNDARY SCAN

The VSC8552 supports the test access port (TAP) and boundary scan architecture described in IEEE 1149.1. The device includes an IEEE 1149.1-compliant test interface, referred to as a JTAG TAP interface.

The JTAG boundary scan logic on the VSC8552, accessed using its TAP interface, consists of a boundary scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal TRST. The following illustration shows the TAP and boundary scan architecture.

**Important** When JTAG is not in use, the TRST pin must be tied to ground with a pull-down resistor for normal operation.

**FIGURE 1-34: TEST ACCESS PORT AND BOUNDARY SCAN ARCHITECTURE**



After a TAP reset, the device identification register is serially connected between TDI and TDO by default. The TAP instruction register is loaded either from a shift register when a new instruction is shifted in, or, if there is no new instruction in the shift register, a default value of 6'b100000 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

## 1.17.9 JTAG INSTRUCTION CODES

The VSC8552 supports the following instruction codes:

**TABLE 1-13: JTAG INSTRUCTION CODES**

| Instruction Code | Description                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BYPASS           | The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.                                                                                                                                                                                            |
| CLAMP            | Allows the state of the signals driven from the component pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins do not change.                                                                                                              |
| EXTEST           | Allows tests of the off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary scan cells, which have to be updated with valid values, with the PRELOAD instruction, prior to the EXTEST instruction.                                                                                                   |
| HIGHZ            | Places the component in a state in which all of its system logic outputs are placed in a high-impedance state. In this state, an in-circuit test system can drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard. |
| IDCODE           | Provides the version number (bits 31:28), device family ID (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.                                                                                                                                                                                                                                                       |
| SAMPLE/PRELOAD   | Allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary scan cells prior to the selection of other boundary scan test instructions.                                                                                                                                                                        |
| USERCODE         | Provides the version number (bits 31:28), part number (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.                                                                                                                                                                                                                                                            |

The following tables provide information about the IDCODE and USERCODE binary values stored in the device JTAG registers.

**TABLE 1-14: IDCODE JTAG DEVICE IDENTIFICATION REGISTER DESCRIPTIONS**

| Description  | Device Version | Family ID           | Manufacturing Identity | LSB |
|--------------|----------------|---------------------|------------------------|-----|
| Bit field    | 31–28          | 27–12               | 11–1                   | 0   |
| Binary value | 0000           | 1000 0101 0111 0100 | 000 0111 0100          | 1   |

**TABLE 1-15: USERCODE JTAG DEVICE IDENTIFICATION REGISTER DESCRIPTIONS**

| Description  | Device Version | Model Number        | Manufacturing Identity | LSB |
|--------------|----------------|---------------------|------------------------|-----|
| Bit field    | 31–28          | 27–12               | 11–1                   | 0   |
| Binary value | 0010           | 1000 0101 0101 0010 | 000 0111 0100          | 1   |

The following table provides information about the location and IEEE compliance of the JTAG instruction codes used in the VSC8552. Instructions not explicitly listed in the table are reserved. For more information about these IEEE specifications, visit the IEEE Web site at [www.IEEE.org](http://www.IEEE.org).

**TABLE 1-16: JTAG INSTRUCTION CODE IEEE COMPLIANCE**

| Instruction    | Code      | Selected Register     | Register Width | IEEE 1149.1 |
|----------------|-----------|-----------------------|----------------|-------------|
| EXTEST         | 6'b000000 | Boundary Scan         | 161            | Mandatory   |
| SAMPLE/PRELOAD | 6'b000001 | Boundary Scan         | 161            | Mandatory   |
| IDCODE         | 6'b100000 | Device Identification | 32             | Optional    |
| USERCODE       | 6'b100101 | Device Identification | 32             | Optional    |
| CLAMP          | 6'b000010 | Bypass Register       | 1              | Optional    |
| HIGHZ          | 6'b000101 | Bypass Register       | 1              | Optional    |
| BYPASS         | 6'b111111 | Bypass Register       | 1              | Mandatory   |

#### 1.17.10 BOUNDARY SCAN REGISTER CELL ORDER

All inputs and outputs are observed in the boundary scan register cells. All outputs are additionally driven by the contents of boundary scan register cells. Bidirectional pins have all three related boundary scan register cells: input, output, and control.

The complete boundary scan cell order is available as a BSDL file format on the Microchip Web site at [www.Microchip.com](http://www.Microchip.com).

### 1.18 100BASE-FX Halt Code Transmission and Reception

The VSC8552 device supports transmission and reception of halt code words in 100BASE-FX mode. There are three separate scripts provided to initiate transmission of halt code words, stop transmission of halt code words and detect reception of halt code words. Use the following scripts to implement each of these functions:

**Sending the HALT codeword:**

```
PhyWrite(<phy>, 31, 0x52b5);
PhyWrite(<phy>, 16, 0xac82);
reg18 = PhyRead(<phy>, 18);
reg18 = (reg18 & 0xf0) | 0x0c;
PhyWrite(<phy>, 18, reg18);
PhyWrite(<phy>, 17, 0xe739);
PhyWrite(<phy>, 16, 0x8c82);
```

```
PhyWrite(<phy>, 16, 0xbe80);
reg17 = PhyRead(<phy>, 17);
reg18 = PhyRead(<phy>, 18);
reg17 = reg17 | 0x0040;
PhyWrite(<phy>, 18, reg18);
PhyWrite(<phy>, 17, reg17);
PhyWrite(<phy>, 16, 0x9e80);
PhyWrite(<phy>, 31, 0);
```

**Stop sending the HALT codeword:**

```
PhyWrite(<phy>, 31, 0x52b5);
PhyWrite(<phy>, 16, 0xbe80);
reg17 = PhyRead(<phy>, 17);
reg18 = PhyRead(<phy>, 18);
reg17 = reg17 & ~0x0040;
PhyWrite(<phy>, 18, reg18);
PhyWrite(<phy>, 17, reg17);
PhyWrite(<phy>, 16, 0x9e80);
PhyWrite(<phy>, 31, 0);
```

Detecting whether the HALT codeword is being sent by the link partner:

```
long patternset[5] = {
    0xce739,
    0xe739c,
    0x739ce,
    0x39ce7,
    0x9ce73
};
```

#### Turning on the pattern checker:

```
PhyWrite(<phy>, 31, 0x52b5);
PhyWrite(<phy>, 16, 0xbe80);
reg18 = PhyRead(<phy>, 18);
reg17 = PhyRead(<phy>, 17);
reg17 = reg17 | 4;
PhyWrite(<phy>, 18, reg18);
PhyWrite(<phy>, 17, reg17);
PhyWrite(<phy>, 16, 0x9e80);
```

#### Sweeping through all five pattern shifts checking for a match:

```
for (i = 0, matchfailed = 1; i < 5 && matchfailed; ++i) {
    PhyWrite(<phy>, 16, 0xac84);
    reg18 = PhyRead(<phy>, 18);
    reg18 = (reg18 & 0xf0) | (patternset[i] >> 16);
    PhyWrite(<phy>, 18, reg18);
    PhyWrite(<phy>, 17, patternset[i] & 0xffff);
    PhyWrite(<phy>, 16, 0x8c84);

    PhyWrite(<phy>, 16, 0xbe84); // Dummy read to clear latched mismatch
    PhyWrite(<phy>, 16, 0xbe84); // Read pattern check failure status
    matchfailed = PhyRead(<phy>, 17) & 1; // Extract pattern check failure status
}
```

#### Turning off the pattern checker:

```
PhyWrite(<phy>, 16, 0xbe80);
reg18 = PhyRead(<phy>, 18);
reg17 = PhyRead(<phy>, 17);
reg17 = reg17 & ~4;
PhyWrite(<phy>, 18, reg18);
PhyWrite(<phy>, 17, reg17);
PhyWrite(<phy>, 16, 0x9e80);

PhyWrite(<phy>, 31, 0);

HALT_codeword_detected = !matchfailed;
```

## 1.19 Configuration

The VSC8552 can be configured by setting internal memory registers using the management interface. To configure the device, perform the following steps:

1. COMA\_MODE active, drive high (optional).
2. Apply power.
3. Apply RefClk.
4. Release reset, drive high. Power and clock must be stable before releasing reset.
5. Wait 120 ms minimum.
6. Apply patch from PHY\_API (required for production released optional for board testing).
7. Configure register 19G for MAC mode (to access register 19G, register 31 must be 0x10). Read register 19G. Set bits 15:14, MAC configuration as follows:
  - 00: SGMII
  - 01: QSGMII
  - 10: RGMII

11: Reserved  
Write new register 19G.

8. Set RGMII (optional)

**TABLE 1-17: REGISTER 18E2 SETTINGS FOR RGMII**

| Bit | Name          | Setting |
|-----|---------------|---------|
| 6:4 | rgmii_skew_tx | 000     |
| 3:1 | rgmii_skew_rx | 000     |
| 0   | rgmii_bit_rev | 0       |

9. Configure register 18G for MAC on all 4 PHYs write:  
SGMII: 0x80F0  
QSGMII: 0x80E0  
RGMII: set 19G[15:14] = 0x10 to set PHY0 and PHY1 MAC to be RGMII
  10. Read register 18G until bit 15 equals 0.
  11. If Fiber Media on all 4 PHYs configure register 18G by writing:  
Media 1000BASE-X: 0x8FC1  
Media 100BASE-FX: 0x8FD1
  12. If Fiber Media read register 18G till bit 15 equals 0.
  13. Configure register 23 for MAC and Media mode (to access register 23, register 31 must be 0). Read register 23.  
Set bits 10:8 as follows:  
000: Copper  
010: 1000BASE-X  
011: 100BASE-FX  
Write new register 23.
  14. Software reset. Read register 0 (to access register 0, register 31 must be 0). Set bit 15 to 1.  
Write new register 0.
  15. Read register 0 until bit 15 equals 0.
  16. Release the COMA\_MODE pin, drive low (only necessary if COMA\_MODE pin is driven high or unconnected).
- Note:** All MAC interfaces must be the same — all QSGMII, RGMII, or SGMII.

### 1.19.1 INITIALIZATION

The COMA\_MODE pin provides an optional feature that may be used to control when the PHYs become active. The typical usage is to keep the PHYs from becoming active before they have been fully initialized. For more information, see [Section 1.19, Configuration](#). By not being active until after complete initialization keeps links from going up and down. Alternatively the COMA\_MODE pin may be connected low (ground) and the PHYs will be fully active once out of reset.

## 2.0 REGISTERS

This section provides information about how to configure the VSC8552 using its internal memory registers and the management interface. The registers marked reserved and factory test should not be read or written to, because doing so may produce undesired effects.

The default value documented for registers is based on the value at reset; however, in some cases, that value may change immediately after reset.

The access type for each register is shown using the following abbreviations:

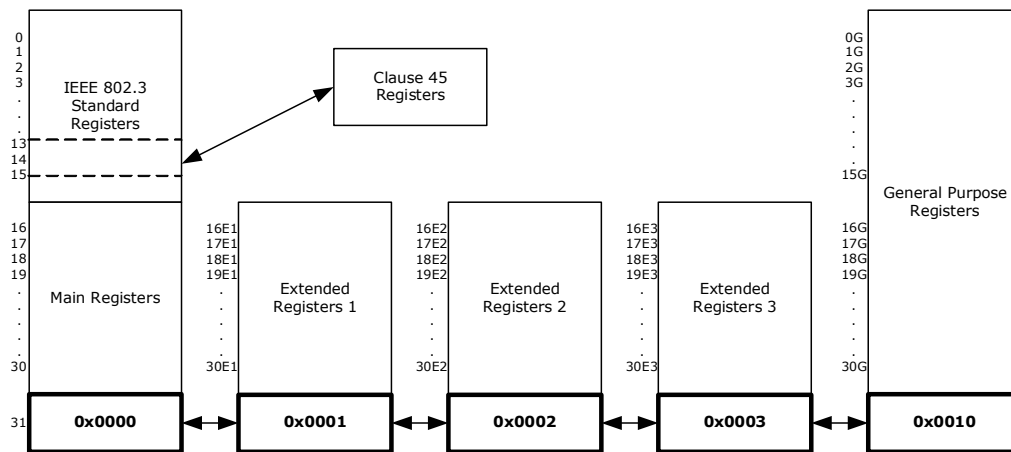
- RO: Read Only
- ROCR: Read Only, Clear on Read
- RO/LH: Read Only, Latch High
- RO/LL: Read Only, Latch Low
- R/W: Read and Write
- RWSC: Read Write Self Clearing

The VSC8552 uses several different types of registers:

- IEEE Clause 22 device registers with addresses from 0 to 31
- Three pages of extended registers with addresses from 16E1–30E1, 16E2–30E2, and 16E3–30E3
- General-purpose registers with addresses from 0G to 30G
- IEEE Clause 45 devices registers accessible through the Clause 22 registers 13 and 14 to support IEEE 802.3az-2010 energy efficient Ethernet registers

The following illustration shows the relationship between the device registers and their address spaces.

**FIGURE 2-1: REGISTER SPACE DIAGRAM**



**Reserved Registers**—For main registers 16–31, extended registers 16E1–30E1, 16E2–30E2, 16E3–30E3, and general purpose registers 0G–30G, any bits marked as Reserved should be processed as read-only and their states as undefined.

**Reserved Bits**—In writing to registers with reserved bits, use a read-modify-then-write technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and their read state cannot be considered static or unchanging.

### 2.1 Register and Bit Conventions

Registers are referred to by their address and bit number in decimal notation. A range of bits is indicated with a colon. For example, a reference to address 26, bits 15 through 14 is shown as 26.15:14.

A register with an E and a number attached (example 27E1) means it is a register contained within extended register page number 1. A register with a G attached (example 13G) means it is a GPIO page register.

Bit numbering follows the IEEE standard with bit 15 being the most significant bit and bit 0 being the least significant bit.

## 2.2 IEEE 802.3 and Main Registers

In the VSC8552, the page space of the standard registers consists of the IEEE 802.3 standard registers and the Microchip standard registers. The following table lists the names of the registers associated with the addresses as specified by IEEE 802.3.

**TABLE 2-1: IEEE 802.3 REGISTERS**

| Address | Name                                                                                  |
|---------|---------------------------------------------------------------------------------------|
| 0       | Mode Control                                                                          |
| 1       | Mode Status                                                                           |
| 2       | PHY Identifier 1                                                                      |
| 3       | PHY Identifier 2                                                                      |
| 4       | Autonegotiation Advertisement                                                         |
| 5       | Autonegotiation Link Partner Ability                                                  |
| 6       | Autonegotiation Expansion                                                             |
| 7       | Autonegotiation Next-Page Transmit                                                    |
| 8       | Autonegotiation Link Partner Next-Page Receive                                        |
| 9       | 1000BASE-T Control                                                                    |
| 10      | 1000BASE-T Status                                                                     |
| 11–12   | Reserved                                                                              |
| 13      | Clause 45 Access Registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D |
| 14      | Clause 45 Access Registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D |
| 15      | 1000BASE-T Status Extension 1                                                         |

The following table lists the names of the registers in the main page space of the device. These registers are accessible only when register address 31 is set to 0x0000.

**TABLE 2-2: MAIN REGISTERS**

| Address | Name                          |
|---------|-------------------------------|
| 16      | 100BASE-TX status extension   |
| 17      | 1000BASE-T status extension 2 |
| 18      | Bypass control                |
| 19      | Error Counter 1               |
| 20      | Error Counter 2               |
| 21      | Error Counter 3               |
| 22      | Extended control and status   |
| 23      | Extended PHY control 1        |
| 24      | Extended PHY control 2        |
| 25      | Interrupt mask                |
| 26      | Interrupt status              |
| 27      | Reserved                      |

**TABLE 2-2: MAIN REGISTERS (CONTINUED)**

| Address | Name                          |
|---------|-------------------------------|
| 28      | Auxiliary control and status  |
| 29      | LED mode select               |
| 30      | LED behavior                  |
| 31      | Extended register page access |

## 2.2.1 MODE CONTROL

The device register at memory address 0 controls several aspects of VSC8552 functionality. The following table shows the available bit settings in this register and what they control.

**TABLE 2-3: MODE CONTROL, ADDRESS 0 (0X00)**

| Bit | Name                       | Access | Description                                                                                                                                                                                                                                                | Default |
|-----|----------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15  | Software reset             | R/W    | Self-clearing. Restores all serial management interface (SMI) registers to default state, except for sticky and super-sticky bits.<br>1: Reset asserted.<br>0: Reset de-asserted. Wait [X] after setting this bit to initiate another SMI register access. | 0       |
| 14  | Loopback                   | R/W    | 1: Loopback enabled.<br>0: Loopback disabled. When loop back is enabled, the device functions at the current speed setting and with the current duplex mode setting (bits 6, 8, and 13 of this register).                                                  | 0       |
| 13  | Forced speed selection LSB | R/W    | Least significant bit. MSB is bit 6.<br>00: 10 Mbps.<br>01: 100 Mbps.<br>10: 1000 Mbps.<br>11: Reserved.                                                                                                                                                   | 0       |
| 12  | Autonegotiation enable     | R/W    | 1: Autonegotiation enabled.<br>0: Autonegotiation disabled.                                                                                                                                                                                                | 1       |
| 11  | Power-down                 | R/W    | 1: Power-down enabled.                                                                                                                                                                                                                                     | 0       |
| 10  | Isolate                    | R/W    | 1: Disconnect the MAC-side interface of the device from the rest of the datapath. Traffic entering the PHY from either the MAC-side or media-side interface will terminate inside the PHY.                                                                 | 0       |
| 9   | Restart autonegotiation    | R/W    | Self-clearing bit.<br>1: Restart autonegotiation on media interface.                                                                                                                                                                                       | 0       |
| 8   | Duplex                     | R/W    | 1: Full-duplex.<br>0: Half-duplex.                                                                                                                                                                                                                         | 0       |
| 7   | Collision test enable      | R/W    | 1: Collision test enabled.                                                                                                                                                                                                                                 | 0       |

**TABLE 2-3: MODE CONTROL, ADDRESS 0 (0X00) (CONTINUED)**

| Bit | Name                          | Access | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Default |
|-----|-------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 6   | Forced speed selection<br>MSB | R/W    | Most significant bit. LSB is bit 13. <sup>1</sup><br>00: 10 Mbps.<br>01: 100 Mbps.<br>10: 1000 Mbps.<br>11: Reserved.                                                                                                                                                                                                                                                                                                                                                                             | 10      |
| 5   | Unidirectional enable         | R/W    | When bit 0.12 = 1 or bit 0.8 = 0, this bit is ignored. When bit 0.12 = 0 and bit 0.8 = 1, the behavior is as follows:<br>1: Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established.<br>0: Enable transmit from media independent interface only when the PHY has determined that a valid link has been established.<br><br><b>Note:</b> This bit is only applicable in 100BASE-FX and 1000BASE-X fiber media modes. | 0       |
| 4:0 | Reserved                      | —      | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 00000   |

- Before selecting the 1000 Mbps forced speed mode, manually configure the PHY as master or slave by setting bit 11 in register 9 (1000BASE-T Control). Each time the link drops, the PHY needs to be powered down manually to enable it to link up again using the master/slave setting specified in register 9.11.

### 2.2.2 MODE STATUS

The register at address 1 in the device main registers space allows you to read the currently enabled mode setting. The following table shows possible readouts of this register.

**TABLE 2-4: MODE STATUS, ADDRESS 1 (0X01)**

| Bit | Name                      | Access | Description                                            | Default |
|-----|---------------------------|--------|--------------------------------------------------------|---------|
| 15  | 100BASE-T4 capability     | RO     | 1: 100BASE-T4 capable.                                 | 0       |
| 14  | 100BASE-TX FDX capability | RO     | 1: 100BASE-TX FDX capable.                             | 1       |
| 13  | 100BASE-TX HDX capability | RO     | 1: 100BASE-TX HDX capable.                             | 1       |
| 12  | 10BASE-T FDX capability   | RO     | 1: 10BASE-T FDX capable.                               | 1       |
| 11  | 10BASE-T HDX capability   | RO     | 1: 10BASE-T HDX capable.                               | 1       |
| 10  | 100BASE-T2 FDX capability | RO     | 1: 100BASE-T2 FDX capable.                             | 0       |
| 9   | 100BASE-T2 HDX capability | RO     | 1: 100BASE-T2 HDX capable.                             | 0       |
| 8   | Extended status enable    | RO     | 1: Extended status information present in register 15. | 1       |

**TABLE 2-4: MODE STATUS, ADDRESS 1 (0X01) (CONTINUED)**

| Bit | Name                            | Access | Description                                                                                                                                                                                                                                                                                                                                                                        | Default |
|-----|---------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | Unidirectional ability          | RO     | 1: PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established.<br>0: PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established.<br><br><b>Note:</b> This bit is only applicable to 100BASE-FX and 1000BASE-X fiber media modes. | 1       |
| 6   | Preamble suppression capability | RO     | 1: MF preamble can be suppressed.<br>0: MF required.                                                                                                                                                                                                                                                                                                                               | 1       |
| 5   | Autonegotiation complete        | RO     | 1: Autonegotiation complete.                                                                                                                                                                                                                                                                                                                                                       | 0       |
| 4   | Remote fault                    | RO     | Latches high.<br>1: Far-end fault detected.                                                                                                                                                                                                                                                                                                                                        | 0       |
| 3   | Autonegotiation capability      | RO     | 1: Autonegotiation capable.                                                                                                                                                                                                                                                                                                                                                        | 1       |
| 2   | Link status                     | RO     | Latches low.<br>1: Link is up.                                                                                                                                                                                                                                                                                                                                                     | 0       |
| 1   | Jabber detect                   | RO     | Latches high.<br>1: Jabber condition detected.                                                                                                                                                                                                                                                                                                                                     | 0       |
| 0   | Extended capability             | RO     | 1: Extended register capable.                                                                                                                                                                                                                                                                                                                                                      | 1       |

## 2.2.3 DEVICE IDENTIFICATION

All 16 bits in both register 2 and register 3 in the VSC8552 are used to provide information associated with aspects of the device identification. The following tables list the expected readouts.

**TABLE 2-5: IDENTIFIER 1, ADDRESS 2 (0X02)**

| Bit  | Name                                     | Access | Description                      | Default |
|------|------------------------------------------|--------|----------------------------------|---------|
| 15:0 | Organizationally unique identifier (OUI) | RO     | OUI most significant bits (3:18) | 0×0007  |

**TABLE 2-6: IDENTIFIER 2, ADDRESS 3 (0X03)**

| Bit   | Name                   | Access | Description                                                               | Default |
|-------|------------------------|--------|---------------------------------------------------------------------------|---------|
| 15:10 | OUI                    | RO     | OUI least significant bits (19:24)                                        | 000001  |
| 9:4   | Microchip model number | RO     | VSC8552 (0xE)                                                             | 001110  |
| 3:0   | Device revision number | RO     | See register 30G for the extended revision identification of this device. | 0010    |

### 2.2.4 AUTONEGOTIATION ADVERTISEMENT

The bits in address 4 in the main registers space control the VSC8552 ability to notify other devices of the status of its autonegotiation feature. The following table shows the available settings and readouts.

**TABLE 2-7: DEVICE AUTONEGOTIATION ADVERTISEMENT, ADDRESS 4 (0X04)**

| Bit | Name                           | Access | Description                    | Default |
|-----|--------------------------------|--------|--------------------------------|---------|
| 15  | Next page transmission request | R/W    | 1: Request enabled             | 0       |
| 14  | Reserved                       | RO     | Reserved                       | 0       |
| 13  | Transmit remote fault          | R/W    | 1: Enabled                     | 0       |
| 12  | Reserved                       | R/W    | Reserved                       | 0       |
| 11  | Advertise asymmetric pause     | R/W    | 1: Advertises asymmetric pause | 0       |
| 10  | Advertise symmetric pause      | R/W    | 1: Advertises symmetric pause  | 0       |
| 9   | Advertise100BASE-T4            | R/W    | 1: Advertises 100BASE-T4       | 0       |
| 8   | Advertise100BASE-TX FDX        | R/W    | 1: Advertise 100BASE-TX FDX    | 1       |
| 7   | Advertise100BASE-TX HDX        | R/W    | 1: Advertises 100BASE-TX HDX   | 1       |
| 6   | Advertise10BASE-T FDX          | R/W    | 1: Advertises 10BASE-T FDX     | 1       |
| 5   | Advertise10BASE-T HDX          | R/W    | 1: Advertises 10BASE-T HDX     | 1       |
| 4:0 | Advertise selector             | R/W    | —                              | 00001   |

### 2.2.5 LINK PARTNER AUTONEGOTIATION CAPABILITY

The bits in main register 5 can be used to determine if the Cat5 link partner (LP) used with the VSC8552 is compatible with the autonegotiation functionality.

**TABLE 2-8: AUTONEGOTIATION LINK PARTNER ABILITY, ADDRESS 5 (0X05)**

| Bit | Name                              | Access | Description                    | Default |
|-----|-----------------------------------|--------|--------------------------------|---------|
| 15  | LP next page transmission request | RO     | 1: Requested                   | 0       |
| 14  | LP acknowledge                    | RO     | 1: Acknowledge                 | 0       |
| 13  | LP remote fault                   | RO     | 1: Remote fault                | 0       |
| 12  | Reserved                          | RO     | Reserved                       | 0       |
| 11  | LP advertise asymmetric pause     | RO     | 1: Capable of asymmetric pause | 0       |
| 10  | LP advertise symmetric pause      | RO     | 1: Capable of symmetric pause  | 0       |
| 9   | LP advertise 100BASE-T4           | RO     | 1: Capable of 100BASE-T4       | 0       |
| 8   | LP advertise 100BASE-TX FDX       | RO     | 1: Capable of 100BASE-TX FDX   | 0       |
| 7   | LP advertise 100BASE-TX HDX       | RO     | 1: Capable of 100BASE-TX HDX   | 0       |
| 6   | LP advertise 10BASE-T FDX         | RO     | 1: Capable of 10BASE-T FDX     | 0       |
| 5   | LP advertise 10BASE-T HDX         | RO     | 1: Capable of 10BASE-T HDX     | 0       |
| 4:0 | LP advertise selector             | RO     |                                | 00000   |

## 2.2.6 AUTONEGOTIATION EXPANSION

The bits in main register 6 work together with those in register 5 to indicate the status of the LP autonegotiation functioning. The following table shows the available settings and readouts.

**TABLE 2-9: AUTONEGOTIATION EXPANSION, ADDRESS 6 (0X06)**

| Bit  | Name                          | Access | Description                                            | Default   |
|------|-------------------------------|--------|--------------------------------------------------------|-----------|
| 15:5 | Reserved                      | RO     | Reserved.                                              | All zeros |
| 4    | Parallel detection fault      | RO     | This bit latches high.<br>1: Parallel detection fault. | 0         |
| 3    | LP next page capable          | RO     | 1: LP is next page capable.                            | 0         |
| 2    | Local PHY next page capable   | RO     | 1: Local PHY is next page capable.                     | 1         |
| 1    | Page received                 | RO     | This bit latches low.<br>1: New page is received.      | 0         |
| 0    | LP is autonegotiation capable | RO     | 1: LP is capable of autonegotiation.                   | 0         |

## 2.2.7 TRANSMIT AUTONEGOTIATION NEXT PAGE

The settings in register 7 in the main registers space provide information about the number of pages in an autonegotiation sequence. The following table shows the settings available.

**TABLE 2-10: AUTONEGOTIATION NEXT PAGE TRANSMIT, ADDRESS 7 (0X07)**

| Bit  | Name                     | Access | Description                                                        | Default    |
|------|--------------------------|--------|--------------------------------------------------------------------|------------|
| 15   | Next page                | R/W    | 1: More pages follow                                               | 0          |
| 14   | Reserved                 | RO     | Reserved                                                           | 0          |
| 13   | Message page             | R/W    | 1: Message page<br>0: Unformatted page                             | 1          |
| 12   | Acknowledge 2            | R/W    | 1: Complies with request<br>0: Cannot comply with request          | 0          |
| 11   | Toggle                   | RO     | 1: Previous transmitted LCW = 0<br>0: Previous transmitted LCW = 1 | 0          |
| 10:0 | Message/unformatted code | R/W    | —                                                                  | 0000000001 |

## 2.2.8 AUTONEGOTIATION LINK PARTNER NEXT PAGE RECEIVE

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP autonegotiation. The following table shows the possible readouts.

**TABLE 2-11: AUTONEGOTIATION LP NEXT PAGE RECEIVE, ADDRESS 8 (0X08)**

| Bit  | Name                        | Access | Description                                                        | Default   |
|------|-----------------------------|--------|--------------------------------------------------------------------|-----------|
| 15   | LP next page                | RO     | 1: More pages follow                                               | 0         |
| 14   | Acknowledge                 | RO     | 1: LP acknowledge                                                  | 0         |
| 13   | LP message page             | RO     | 1: Message page<br>0: Unformatted page                             | 0         |
| 12   | LP acknowledge 2            | RO     | 1: LP complies with request                                        | 0         |
| 11   | LP toggle                   | RO     | 1: Previous transmitted LCW = 0<br>0: Previous transmitted LCW = 1 | 0         |
| 10:0 | LP message/unformatted code | RO     | —                                                                  | All zeros |

## 2.2.9 1000BASE-T CONTROL

The VSC8552's 1000BASE-T functionality is controlled by the bits in register 9 of the main register space. The following table shows the settings and readouts available.

**TABLE 2-12: 1000BASE-T CONTROL, ADDRESS 9 (0X09)**

| Bit   | Name                              | Access | Description                                                                                                                                                                                                      | Default |
|-------|-----------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:13 | Transmitter test mode             | R/W    | 000: Normal<br>001: Mode 1: Transmit waveform test<br>010: Mode 2: Transmit jitter test as master<br>011: Mode 3: Transmit jitter test as slave<br>100: Mode 4: Transmitter distortion test<br>101–111: Reserved | 000     |
| 12    | Master/slave manual configuration | R/W    | 1: Master/slave manual configuration enabled                                                                                                                                                                     | 0       |
| 11    | Master/slave value                | R/W    | This register is only valid when bit 9.12 is set to 1.<br>1: Configure PHY as master during negotiation<br>0: Configure PHY as slave during negotiation                                                          | 0       |
| 10    | Port type                         | R/W    | 1: Multi-port device<br>0: Single-port device                                                                                                                                                                    | 1       |
| 9     | 1000BASE-T FDX capability         | R/W    | 1: PHY is 1000BASE-T FDX capable                                                                                                                                                                                 | 1       |
| 8     | 1000BASE-T HDX capability         | R/W    | 1: PHY is 1000BASE-T HDX capable                                                                                                                                                                                 | 1       |
| 7:0   | Reserved                          | R/W    | Reserved                                                                                                                                                                                                         | 0x00    |

**Note:** Transmitter test mode (bits 15:13) operates in the manner described in IEEE 802.3 section 40.6.1.1.2. When using any of the transmitter test modes, the automatic media sense feature must be disabled. For more information, see [Section 2.2.21, Extended PHY Control Set 1](#).

## 2.2.10 1000BASE-T STATUS

The bits in register 10 of the main register space can be read to obtain the status of the 1000BASE-T communications enabled in the device. The following table shows the readouts.

**TABLE 2-13: 1000BASE-T STATUS, ADDRESS 10 (0X0A)**

| Bit | Name                                  | Access | Description                                                                                                               | Default |
|-----|---------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------|---------|
| 15  | Master/slave configuration fault      | RO     | This bit latches high.<br>1: Master/slave configuration fault detected<br>0: No master/slave configuration fault detected | 0       |
| 14  | Master/slave configuration resolution | RO     | 1: Local PHY configuration resolved to master<br>0: Local PHY configuration resolved to slave                             | 1       |
| 13  | Local receiver status                 | RO     | 1: Local receiver is operating normally                                                                                   | 0       |
| 12  | Remote receiver status                | RO     | 1: Remote receiver OK                                                                                                     | 0       |
| 11  | LP 1000BASE-T FDX capability          | RO     | 1: LP 1000BASE-T FDX capable                                                                                              | 0       |

**TABLE 2-13: 1000BASE-T STATUS, ADDRESS 10 (0X0A) (CONTINUED)**

| Bit | Name                         | Access | Description                  | Default |
|-----|------------------------------|--------|------------------------------|---------|
| 10  | LP 1000BASE-T HDX capability | RO     | 1: LP 1000BASE-T HDX capable | 0       |
| 9:8 | Reserved                     | RO     | Reserved                     | 00      |
| 7:0 | Idle error count             | RO     | Self-clearing register       | 0x00    |

## 2.2.11 MMD ACCESS CONTROL REGISTER

The bits in register 13 of the main register space are a window to the EEE registers as defined in IEEE 802.3az-2010 Clause 45.

**TABLE 2-14: MMD EEE ACCESS, ADDRESS 13 (0X0D)**

| Bit   | Name     | Access | Description                                                                                                                          |
|-------|----------|--------|--------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | Function | R/W    | 00: Address<br>01: Data, no post increment<br>10: Data, post increment for read and write<br>11: Data, post increment for write only |
| 13:5  | Reserved | R/W    | Reserved                                                                                                                             |
| 4:0   | DVAD     | R/W    | Device address as defined in IEEE 802.3az-2010 table 45–1                                                                            |

## 2.2.12 MMD ADDRESS OR DATA REGISTER

The bits in register 14 of the main register space are a window to the EEE registers as defined in IEEE 802.3az-2010 Clause 45.

**TABLE 2-15: MMD ADDRESS OR DATA REGISTER, ADDRESS 14 (0X0E)**

| Bit  | Name                  | Access | Description                                                                                                                                                    |
|------|-----------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | Register Address/Data | R/W    | When register 13.15:14 = 2'b00, address of register of the device that is specified by 13.4:0. Otherwise, the data to be written to or read from the register. |

## 2.2.13 1000BASE-T STATUS EXTENSION 1

Register 15 provides additional information about the operation of the device 1000BASE-T communications. The following table shows the readouts available.

**TABLE 2-16: 1000BASE-T STATUS EXTENSION 1, ADDRESS 15 (0X0F)**

| Bit  | Name                      | Access | Description                      | Default |
|------|---------------------------|--------|----------------------------------|---------|
| 15   | 1000BASE-X FDX capability | RO     | 1: PHY is 1000BASE-X FDX capable | 1       |
| 14   | 1000BASE-X HDX capability | RO     | 1: PHY is 1000BASE-X HDX capable | 1       |
| 13   | 1000BASE-T FDX capability | RO     | 1: PHY is 1000BASE-T FDX capable | 1       |
| 12   | 1000BASE-T HDX capability | RO     | 1: PHY is 1000BASE-T HDX capable | 1       |
| 11:0 | Reserved                  | RO     | Reserved                         | 0x000   |

### 2.2.14 100BASE-TX/FX STATUS EXTENSION

Register 16 in the main registers page space of the VSC8552 provides additional information about the status of the device's 100BASE-TX/100BASE-FX operation.

**TABLE 2-17: 100BASE-TX/FX STATUS EXTENSION, ADDRESS 16 (0X10)**

| Bit | Name                              | Access | Description                                                       | Default |
|-----|-----------------------------------|--------|-------------------------------------------------------------------|---------|
| 15  | 100BASE-TX/FX Descrambler         | RO     | 1: Descrambler locked                                             | 0       |
| 14  | 100BASE-TX/FX lock error          | RO     | Self-clearing bit.<br>1: Lock error detected                      | 0       |
| 13  | 100BASE-TX/FX disconnect state    | RO     | Self-clearing bit.<br>1: PHY 100BASE-TX link disconnect detected  | 0       |
| 12  | 100BASE-TX/FX current link status | RO     | 1: PHY 100BASE-TX link active                                     | 0       |
| 11  | 100BASE-TX/FX receive error       | RO     | Self-clearing bit.<br>1: Receive error detected                   | 0       |
| 10  | 100BASE-TX/FX transmit error      | RO     | Self-clearing bit.<br>1: Transmit error detected                  | 0       |
| 9   | 100BASE-TX/FX SSD error           | RO     | Self-clearing bit.<br>1: Start-of-stream delimiter error detected | 0       |
| 8   | 100BASE-TX/FX ESD error           | RO     | Self-clearing bit.<br>1: End-of-stream delimiter error detected   | 0       |
| 7:0 | Reserved                          | RO     | Reserved                                                          | —       |

### 2.2.15 1000BASE-T STATUS EXTENSION 2

The second status extension register is at address 17 in the device main registers space. It provides information about another set of parameters associated with 1000BASE-T communications. For information about the first status extension register, see [Table 2-16](#).

**TABLE 2-18: 1000BASE-T STATUS EXTENSION 2, ADDRESS 17 (0X11)**

| Bit | Name                           | Access | Description                                                       | Default |
|-----|--------------------------------|--------|-------------------------------------------------------------------|---------|
| 15  | 1000BASE-T descrambler         | RO     | 1: Descrambler locked.                                            | 0       |
| 14  | 1000BASE-T lock error          | RO     | Self-clearing bit.<br>1: Lock error detected                      | 0       |
| 13  | 1000BASE-T disconnect state    | RO     | Self-clearing bit.<br>1: PHY 1000BASE-T link disconnect detected  | 0       |
| 12  | 1000BASE-T current link status | RO     | 1: PHY 1000BASE-T link active                                     | 0       |
| 11  | 1000BASE-T receive error       | RO     | Self-clearing bit.<br>1: Receive error detected                   | 0       |
| 10  | 1000BASE-T transmit error      | RO     | Self-clearing bit.<br>1: Transmit error detected                  | 0       |
| 9   | 1000BASE-T SSD error           | RO     | Self-clearing bit.<br>1: Start-of-stream delimiter error detected | 0       |

**TABLE 2-18: 1000BASE-T STATUS EXTENSION 2, ADDRESS 17 (0X11) (CONTINUED)**

| Bit | Name                               | Access | Description                                                     | Default |
|-----|------------------------------------|--------|-----------------------------------------------------------------|---------|
| 8   | 1000BASE-T ESD error               | RO     | Self-clearing bit.<br>1: End-of-stream delimiter error detected | 0       |
| 7   | 1000BASE-T carrier extension error | RO     | Self-clearing bit.<br>1: Carrier extension error detected       | 0       |
| 6   | Non-compliant BCM5400 detected     | RO     | 1: Non-compliant BCM5400 link partner detected                  | 0       |
| 5   | MDI crossover error                | RO     | 1: MDI crossover error was detected                             | 0       |
| 4:0 | Reserved                           | RO     | Reserved                                                        | —       |

## 2.2.16 BYPASS CONTROL

The bits in this register control aspects of functionality in effect when the device is disabled for the purpose of traffic bypass. The following table shows the settings available.

**TABLE 2-19: BYPASS CONTROL, ADDRESS 18 (0X12)**

| Bit | Name                                                                     | Access | Description                                                                        | Default |
|-----|--------------------------------------------------------------------------|--------|------------------------------------------------------------------------------------|---------|
| 15  | Transmit disable                                                         | R/W    | 1: PHY transmitter disabled                                                        | 0       |
| 14  | 4B5B encoder/decoder                                                     | R/W    | 1: Bypass 4B/5B encoder/decoder                                                    | 0       |
| 13  | Scrambler                                                                | R/W    | 1: Bypass scrambler                                                                | 0       |
| 12  | Descrambler                                                              | R/W    | 1: Bypass descrambler                                                              | 0       |
| 11  | PCS receive                                                              | R/W    | 1: Bypass PCS receiver                                                             | 0       |
| 10  | PCS transmit                                                             | R/W    | 1: Bypass PCS transmit                                                             | 0       |
| 9   | LFI timer                                                                | R/W    | 1: Bypass Link Fail Inhibit (LFI) timer                                            | 0       |
| 8   | Reserved                                                                 | RO     | Reserved                                                                           | —       |
| 7   | HP Auto-MDIX at forced 10/100                                            | R/W    | Sticky bit.<br>1: Disable HP Auto-MDIX at forced 10/100 speeds                     | 1       |
| 6   | Non-compliant BCM5400 detect disable                                     | R/W    | Sticky bit.<br>1: Disable non-compliant BCM5400 detection                          | 0       |
| 5   | Disable pair swap correction (HP Auto-MDIX when autonegotiation enabled) | R/W    | Sticky bit.<br>1: Disable the automatic pair swap correction                       | 0       |
| 4   | Disable polarity correction                                              | R/W    | Sticky bit.<br>1: Disable polarity inversion correction on each subchannel         | 0       |
| 3   | Parallel detect control                                                  | R/W    | Sticky bit.<br>1: Do not ignore advertised ability<br>0: Ignore advertised ability | 1       |
| 2   | Pulse shaping filter                                                     | R/W    | 1: Disable pulse shaping filter                                                    | 0       |
| 1   | Disable automatic 1000BASE-T next page exchange                          | R/W    | Sticky bit.<br>1: Disable automatic 1000BASE T next page exchanges                 | 0       |
| 0   | Reserved                                                                 | RO     | Reserved                                                                           | —       |

**Note:** If bit 18.1 is set to 1 in this register, automatic exchange of next pages is disabled, and control is returned to the user through the SMI after the base page is exchanged. The user then must send the correct sequence of next pages to the link partner, determine the common capabilities, and force the device into the correct configuration following the successful exchange of pages.

### 2.2.17 ERROR COUNTER 1

The bits in register 19 provide an error counter. The following table shows the settings available.

**TABLE 2-20: ERROR COUNTER 1, ADDRESS 19 (0X13)**

| Bit  | Name                           | Access | Description                                                                               | Default |
|------|--------------------------------|--------|-------------------------------------------------------------------------------------------|---------|
| 15:8 | Reserved                       | RO     | Reserved.                                                                                 | —       |
| 7:0  | 100/1000 receive error counter | RO     | 8-bit counter that saturates when it reaches 255. These bits are self-clearing when read. | 0x00    |

### 2.2.18 ERROR COUNTER 2

The bits in register 20 provide an error counter. The following table shows the settings available.

**TABLE 2-21: ERROR COUNTER 2, ADDRESS 20 (0X14)**

| Bit  | Name                           | Access | Description                                                                               | Default |
|------|--------------------------------|--------|-------------------------------------------------------------------------------------------|---------|
| 15:8 | Reserved                       | RO     | Reserved.                                                                                 | —       |
| 7:0  | 100/1000 false carrier counter | RO     | 8-bit counter that saturates when it reaches 255. These bits are self-clearing when read. | 0x00    |

### 2.2.19 ERROR COUNTER 3

The bits in register 21 provide an error counter. The following table shows the settings available.

**TABLE 2-22: ERROR COUNTER 3, ADDRESS 21 (0X15)**

| Bit  | Name                                 | Access | Description                                                                               | Default |
|------|--------------------------------------|--------|-------------------------------------------------------------------------------------------|---------|
| 15:8 | Reserved                             | RO     | Reserved.                                                                                 | —       |
| 7:0  | Copper media link disconnect counter | RO     | 8-bit counter that saturates when it reaches 255. These bits are self-clearing when read. | 0x00    |

### 2.2.20 EXTENDED CONTROL AND STATUS

The bits in register 22 provide additional device control and readouts. The following table shows the settings available.

**TABLE 2-23: EXTENDED CONTROL AND STATUS, ADDRESS 22 (0X16)**

| Bit | Name                     | Access | Description                                                                   | Default |
|-----|--------------------------|--------|-------------------------------------------------------------------------------|---------|
| 15  | Force 10BASE-T link high | R/W    | Sticky bit.<br>1: Bypass link integrity test<br>0: Enable link integrity test | 0       |
| 14  | Jabber detect disable    | R/W    | Sticky bit.<br>1: Disable jabber detect                                       | 0       |
| 13  | Disable 10BASE-T echo    | R/W    | Sticky bit.<br>1: Disable 10BASE-T echo                                       | 1       |
| 12  | Disable SQE mode         | R/W    | Sticky bit.<br>1: Disable SQE mode                                            | 1       |

**TABLE 2-23: EXTENDED CONTROL AND STATUS, ADDRESS 22 (0X16) (CONTINUED)**

| Bit   | Name                      | Access | Description                                                                              | Default |
|-------|---------------------------|--------|------------------------------------------------------------------------------------------|---------|
| 11:10 | 10BASE-T squelch control  | R/W    | Sticky bit.<br>00: Normal squelch<br>01: Low squelch<br>10: High squelch<br>11: Reserved | 00      |
| 9     | Sticky reset enable       | R/W    | Super-sticky bit.<br>1: Enabled                                                          | 1       |
| 8     | EOF Error                 | RO     | This bit is self-clearing.<br>1: EOF error detected                                      | 0       |
| 7     | 10BASE-T disconnect state | RO     | This bit is self-clearing.<br>1: 10BASE-T link disconnect detected                       | 0       |
| 6     | 10BASE-T link status      | RO     | 1: 10BASE-T link active                                                                  | 0       |
| 5:1   | Reserved                  | RO     | Reserved                                                                                 | —       |
| 0     | SMI broadcast write       | R/W    | Sticky bit.<br>1: Enabled                                                                | 0       |

The following information applies to the extended control and status bits:

- When bit 22.15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.
- When bits 22.11:10 are set to 00, the squelch threshold levels are based on the IEEE standard for 10BASE-T. When set to 01, the squelch level is decreased, which can improve the bit error rate performance on long loops. When set to 10, the squelch level is increased and can improve the bit error rate in high-noise environments.
- When bit 22.9 is set, all sticky register bits retain their values during a software reset. Clearing this bit causes all sticky register bits to change to their default values upon software reset. Super-sticky bits retain their values upon software reset regardless of the setting of bit 22.9.
- When bit 22.0 is set, if a write to any PHY register (registers 0–31, including extended registers), the same write is broadcast to all PHYs. For example, if bit 22.0 is set to 1 and a write to PHY0 is executed (register 0 is set to 0x1040), all PHYs' register 0s are set to 0x1040. This bit must be disabled before performing a software reset of any PHY port (see register 0 bit 15, [Table 2-3](#)). Disabling this bit restores normal PHY write operation. Reads are still possible when this bit is set, but the value that is read corresponds only to the particular PHY being addressed.

## 2.2.21 EXTENDED PHY CONTROL SET 1

The following table shows the settings available.

**TABLE 2-24: EXTENDED PHY CONTROL 1, ADDRESS 23 (0X17)**

| Bit   | Name               | Access | Description                                                                                                                               | Default |
|-------|--------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:13 | Reserved           | R/W    | Reserved                                                                                                                                  | 0       |
| 12    | MAC interface mode | R/W    | Super-sticky bit.<br>0: RGMII/SGMII<br>1: 1000BASE-X.<br><br><b>Note:</b> Register 19G.15:14 must be = 00 for this selection to be valid. | 0       |
| 11    | AMS preference     | R/W    | Super-sticky bit.<br>1: Cat5 copper preferred.<br>0: SerDes fiber/SFP preferred.                                                          | 0       |

**TABLE 2-24: EXTENDED PHY CONTROL 1, ADDRESS 23 (0X17) (CONTINUED)**

| Bit  | Name                  | Access | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Default |
|------|-----------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 10:8 | Media operating mode  | R/W    | Super-sticky bits.<br>000: Cat5 copper only.<br>001: SerDes fiber/SFP protocol transfer mode only.<br>010: 1000BASE-X fiber/SFP media only with autonegotiation performed by the PHY.<br>011: 100BASE-FX fiber/SFP on the fiber media pins only.<br>101: Automatic media sense (AMS) with Cat5 media or SerDes fiber/SFP protocol transfer mode.<br>110: AMS with Cat5 media or 1000BASE-X fiber/SFP media with autonegotiation performed by PHY.<br>111: AMS with Cat5 media or 100BASE-FX fiber/SFP media.<br>100: AMS. | 000     |
| 7:6  | Force AMS override    | R/W    | Sticky bits.<br>00: Normal AMS selection<br>01: Force AMS to select SerDes media only<br>10: Force AMS to select copper media only<br>11: Reserved                                                                                                                                                                                                                                                                                                                                                                        | 00      |
| 5:4  | Reserved              | RO     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | —       |
| 3    | Far-end loopback mode | R/W    | 1: Enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0       |
| 2:0  | Reserved              | RO     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | —       |

**Note:** After configuring bits 13:8 of the extended PHY control register set 1, a software reset (register 0, bit 15) must be written to change the device operating mode. On read, these bits only indicate the actual operating mode and not the pending operating mode setting before a software reset has taken place.

## 2.2.22 EXTENDED PHY CONTROL SET 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table shows the settings and readouts available.

**TABLE 2-25: EXTENDED PHY CONTROL 2, ADDRESS 24 (0X18)**

| Bit   | Name                          | Access | Description                                                                                                                                                                                                  | Default |
|-------|-------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:13 | 100BASE-TX edge rate control  | R/W    | Sticky bit.<br>011: +5 edge rate (slowest)<br>010: +4 edge rate<br>001: +3 edge rate<br>000: +2 edge rate<br>111: +1 edge rate<br>110: Default edge rate<br>101: –1 edge rate<br>100: –2 edge rate (fastest) | 001     |
| 12    | PICMG 2.16 reduced power mode | R/W    | Sticky bit.<br>1: Enabled                                                                                                                                                                                    | 0       |
| 11:6  | Reserved                      | RO     | Reserved                                                                                                                                                                                                     | —       |

**TABLE 2-25: EXTENDED PHY CONTROL 2, ADDRESS 24 (0X18) (CONTINUED)**

| Bit | Name                          | Access | Description                                                                                                                                                                                                                      | Default |
|-----|-------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 5:4 | Jumbo packet mode             | R/W    | Sticky bit.<br>00: Normal IEEE 1.5 kB packet length<br>01: 9 kB jumbo packet length (12 kB with 60 ppm or better reference clock)<br>10: 12 kB jumbo packet length (16 kB with 70 ppm or better reference clock)<br>11: Reserved | 00      |
| 3:1 | Reserved                      | RO     | Reserved                                                                                                                                                                                                                         | —       |
| 0   | 1000BASE-T connector loopback | R/W    | 1: Enabled                                                                                                                                                                                                                       | 0       |

**Note:** When bits 5:4 are set to jumbo packet mode, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the bit description results in a higher jumbo packet length.

## 2.2.23 INTERRUPT MASK

These bits control the device interrupt mask. The following table shows the settings available.

**TABLE 2-26: INTERRUPT MASK, ADDRESS 25 (0X19)**

| Bit | Name                                            | Access | Description             | Default |
|-----|-------------------------------------------------|--------|-------------------------|---------|
| 15  | MDINT interrupt status enable                   | R/W    | Sticky bit. 1: Enabled. | 0       |
| 14  | Speed state change mask                         | R/W    | Sticky bit. 1: Enabled. | 0       |
| 13  | Link state change mask                          | R/W    | Sticky bit. 1: Enabled. | 0       |
| 12  | FDX state change mask                           | R/W    | Sticky bit. 1: Enabled. | 0       |
| 11  | Autonegotiation error mask                      | R/W    | Sticky bit. 1: Enabled. | 0       |
| 10  | Autonegotiation complete mask                   | R/W    | Sticky bit. 1: Enabled. | 0       |
| 9   | Inline powered device (PoE) detect mask         | R/W    | Sticky bit. 1: Enabled. | 0       |
| 8   | Symbol error interrupt mask                     | R/W    | Sticky bit. 1: Enabled. | 0       |
| 7   | Fast link failure interrupt mask <sup>(1)</sup> | R/W    | Sticky bit. 1: Enabled. | 0       |
| 6:5 | Reserved                                        | R/W    | —                       | 0       |
| 4   | AMS media changed mask <sup>(2)</sup>           | R/W    | Sticky bit. 1: Enabled. | 0       |
| 3   | False carrier interrupt mask                    | R/W    | Sticky bit. 1: Enabled. | 0       |
| 2   | Link speed downshift detect mask                | R/W    | Sticky bit. 1: Enabled. | 0       |
| 1   | Master/Slave resolution error mask              | R/W    | Sticky bit. 1: Enabled. | 0       |
| 0   | RX_ER interrupt mask                            | R/W    | Sticky bit. 1: Enabled. | 0       |

1. The interrupt is only valid for 100 Mbps and 1000 Mbps speeds. Notification at 10 Mbps speed requires use of the FASTLINK-FAIL pin.
2. If hardware interrupts are not used, the mask can still be set and the status polled for changes.

**Note:** When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted. Also, before enabling this bit, read register 26 to clear any previously inactive interrupts pending that will cause bit 25.15 to be set.

## 2.2.24 INTERRUPT STATUS

The status of interrupts already written to the device is available for reading from register 26 in the main registers space. The following table shows the expected readouts.

**TABLE 2-27: INTERRUPT STATUS, ADDRESS 26 (0X1A)**

| Bit | Name                                 | Access | Description                              | Default |
|-----|--------------------------------------|--------|------------------------------------------|---------|
| 15  | Interrupt status                     | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 14  | Speed state change status            | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 13  | Link state change status             | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 12  | FDX state change status              | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 11  | Autonegotiation error status         | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 10  | Autonegotiation complete status      | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 9   | Inline powered device detect status  | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 8   | Symbol error status                  | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 7   | Fast link failure detect status      | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 6:5 | Reserved                             | RO     | —                                        | 0       |
| 4   | AMS media changed mask <sup>1</sup>  | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 3   | False carrier interrupt status       | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 2   | Link speed downshift detect status   | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 1   | Master/Slave resolution error status | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |
| 0   | RX_ER interrupt status               | RO     | Self-clearing bit. 1: Interrupt pending. | 0       |

1. If hardware interrupts are not used, the mask can still be set and the status polled for changes.

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.2, bits 4.8:5 must be set for this interrupt to assert.
- For bit 26.0, this interrupt will not occur when RX\_ER is used for carrier-extension decoding of a link partner's data transmission.

## 2.2.25 DEVICE AUXILIARY CONTROL AND STATUS

Register 28 provides control and status information for several device functions not controlled or monitored by other device registers. The following table shows the settings available and the expected readouts.

**TABLE 2-28: AUXILIARY CONTROL AND STATUS, ADDRESS 28 (0X1C)**

| Bit             | Name                              | Access | Description                                    | Default |
|-----------------|-----------------------------------|--------|------------------------------------------------|---------|
| 15              | Autonegotiation complete          | RO     | Duplicate of bit 1.5                           | 0       |
| 14              | Autonegotiation disabled          | RO     | Inverted duplicate of bit 0.12                 | 0       |
| 13 <sup>1</sup> | HP Auto-MDIX crossover indication | RO     | 1: HP Auto-MDIX crossover performed internally | 0       |

**TABLE 2-28: AUXILIARY CONTROL AND STATUS, ADDRESS 28 (0X1C) (CONTINUED)**

| Bit | Name                                     | Access | Description                                                                                                                                                                  | Default |
|-----|------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 12  | CD pair swap                             | RO     | 1: CD pairs are swapped                                                                                                                                                      | 0       |
| 11  | A polarity inversion                     | RO     | 1: Polarity swap on pair A                                                                                                                                                   | 0       |
| 10  | B polarity inversion                     | RO     | 1: Polarity swap on pair B                                                                                                                                                   | 0       |
| 9   | C polarity inversion                     | RO     | 1: Polarity swap on pair C                                                                                                                                                   | 0       |
| 8   | D polarity inversion                     | RO     | 1: Polarity swap on pair D                                                                                                                                                   | 0       |
| 7   | ActiPHY link status time-out control [1] | R/W    | Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB.<br>00: 2.3 seconds<br>01: 3.3 seconds<br>10: 4.3 seconds<br>11: 5.3 seconds | 0       |
| 6   | ActiPHY mode enable                      | R/W    | Sticky bit.<br>1: Enabled                                                                                                                                                    | 0       |
| 5   | FDX status                               | RO     | 1: Full-duplex<br>0: Half-duplex                                                                                                                                             | 00      |
| 4:3 | Speed status                             | RO     | 00: Speed is 10BASE-T<br>01: Speed is 100BASE-TX or 100BASE-FX<br>10: Speed is 1000BASE-T or 1000BASE-X<br>11: Reserved                                                      | 0       |
| 2   | ActiPHY link status time-out control [0] | R/W    | Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB.<br>00: 2.3 seconds<br>01: 3.3 seconds<br>10: 4.3 seconds<br>11: 5.3 seconds | 1       |
| 1:0 | Media mode status                        | RO     | 00: No media selected<br>01: Copper media selected<br>10: SerDes (Fiber) media selected<br>11: Reserved                                                                      | 00      |

1. In 1000BT mode, if Force MDI crossover is performed while link is up, the 1000BT link must be re-negotiated in order for this bit to reflect the actual Auto-MDIX setting.

## 2.2.26 LED MODE SELECT

The device LED outputs are controlled using the bits in register 29 of the main register space. The following table shows the information needed to access the functionality of each of the outputs. For more information about LED modes, see [Table 1-7](#). For information about enabling the extended LED mode bits in Register 19E1 bits 13 to 12, see [Table 1-8](#).

**TABLE 2-29: LED MODE SELECT, ADDRESS 29 (0X1D)**

| Bit   | Name             | Access | Description                             | Default |
|-------|------------------|--------|-----------------------------------------|---------|
| 15:12 | LED3 mode select | R/W    | Sticky bit. Select from LED modes 0–15. | 1000    |
| 11:8  | LED2 mode select | R/W    | Sticky bit. Select from LED modes 0–15. | 0000    |
| 7:4   | LED1 mode select | R/W    | Sticky bit. Select from LED modes 0–15. | 0010    |
| 3:0   | LED0 mode select | R/W    | Sticky bit. Select from LED modes 0–15. | 0001    |

## 2.2.27 LED BEHAVIOR

The bits in register 30 control and enable you to read the status of the pulse or blink rate of the device LEDs. The following table shows the settings you can write to the register or read from the register.

**TABLE 2-30: LED BEHAVIOR, ADDRESS 30 (0X1E)**

| Bit   | Name                                 | Access | Description                                                                                                                                                                                                                                                                                      | Default |
|-------|--------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15    | Copper and fiber LED combine disable | R/W    | Sticky bit<br>0: Combine enabled (Copper/Fiber on link/linkXXXX/activity LED)<br>1: Disable combination (link/linkXXXX/activity LED; indicates copper only)                                                                                                                                      | 0       |
| 14    | Activity output select               | R/W    | Sticky bit<br>1: Activity LED becomes TX_Activity and fiber activity LED becomes RX_Activity<br>0: TX and RX activity both displayed on activity LEDs                                                                                                                                            | 0       |
| 13    | Reserved                             | RO     | Reserved                                                                                                                                                                                                                                                                                         | —       |
| 12    | LED pulsing enable                   | R/W    | Sticky bit<br>0: Normal operation<br>1: LEDs pulse with a 5 kHz, programmable duty cycle when active                                                                                                                                                                                             | 0       |
| 11:10 | LED blink/pulse-stretch rate         | R/W    | Sticky bit<br>00: 2.5 Hz blink rate/400 ms pulse-stretch<br>01: 5 Hz blink rate/200 ms pulse-stretch<br>10: 10 Hz blink rate/100 ms pulse-stretch<br>11: 20 Hz blink rate/50 ms pulse-stretch<br>The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports | 01      |
| 9     | Reserved                             | RO     | Reserved                                                                                                                                                                                                                                                                                         | —       |
| 8     | LED3 pulse-stretch/blink select      | R/W    | Sticky bit<br>1: Pulse-stretch<br>0: Blink                                                                                                                                                                                                                                                       | 0       |
| 7     | LED2 pulse-stretch/blink select      | R/W    | Sticky bit<br>1: Pulse-stretch<br>0: Blink                                                                                                                                                                                                                                                       | 0       |
| 6     | LED1 pulse-stretch/blink select      | R/W    | Sticky bit<br>1: Pulse-stretch<br>0: Blink                                                                                                                                                                                                                                                       | 0       |
| 5     | LED0 pulse-stretch/blink select      | R/W    | Sticky bit<br>1: Pulse-stretch<br>0: Blink                                                                                                                                                                                                                                                       | 0       |
| 4:2   | Reserved                             | RO     | Reserved                                                                                                                                                                                                                                                                                         | —       |
| 3     | LED3 combine feature disable         | R/W    | Sticky bit<br>0: Combine enabled (link/activity, duplex/collision)<br>1: Disable combination (link only, duplex only)                                                                                                                                                                            | 0       |

**TABLE 2-30: LED BEHAVIOR, ADDRESS 30 (0X1E) (CONTINUED)**

| Bit | Name                         | Access | Description                                                                                                           | Default |
|-----|------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------|---------|
| 2   | LED2 combine feature disable | R/W    | Sticky bit<br>0: Combine enabled (link/activity, duplex/collision)<br>1: Disable combination (link only, duplex only) | 0       |
| 1   | LED1 combine feature disable | R/W    | Sticky bit<br>0: Combine enabled (link/activity, duplex/collision)<br>1: Disable combination (link only, duplex only) | 0       |
| 0   | LED0 combine feature disable | R/W    | Sticky bit<br>0: Combine enabled (link/activity, duplex/collision)<br>1: Disable combination (link only, duplex only) | 0       |

**Note:** Bits 30.11:10 are active only in port 0 and affect the behavior of LEDs for all the ports.

## 2.2.28 EXTENDED PAGE ACCESS

To provide functionality beyond the IEEE 802.3-specified registers and main device registers, the VSC8552 includes an extended set of registers that provide an additional 15 register spaces.

The register at address 31 controls the access to the extended registers for the VSC8552. Accessing the GPIO page register space is similar to accessing the extended page registers. The following table shows the settings available.

**TABLE 2-31: EXTENDED/GPIO REGISTER PAGE ACCESS, ADDRESS 31 (0X1F)**

| Bit  | Name                               | Access | Description                                                                                                                                                                                                                                                                                                                                                    | Default |
|------|------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:0 | Extended/GPIO page register access | R/W    | 0x0000: Register 16–30 accesses main register space. Writing 0x0000 to register 31 restores the main register access.<br>0x0001: Registers 16–30 access extended register space 1<br>0x0002: Registers 16–30 access extended register space 2<br>0x0003: Registers 16–30 access extended register space 3<br>0x0010: Registers 0–30 access GPIO register space | 0x0000  |

## 2.3 Extended Page 1 Registers

To access the extended page 1 registers (16E1–30E1), enable extended register access by writing 0x0001 to register 31. Writing 0x0000 to register 31 restores the main register access.

When extended page 1 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E1–30E1 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

**TABLE 2-32: EXTENDED REGISTERS PAGE 1 SPACE**

| Address | Name                             |
|---------|----------------------------------|
| 16E1    | SerDes Media Control             |
| 17E1    | Reserved                         |
| 18E1    | Cu Media CRC good counter        |
| 19E1    | Extended mode and SIGDET control |
| 20E1    | Extended PHY control 3 (ActiPHY) |

**TABLE 2-32: EXTENDED REGISTERS PAGE 1 SPACE (CONTINUED)**

| Address   | Name                                               |
|-----------|----------------------------------------------------|
| 21E1–22E1 | Reserved                                           |
| 23E1      | Extended PHY control 4 (PoE and CRC error counter) |
| 24E1      | VeriPHY 1                                          |
| 25E1      | VeriPHY 2                                          |
| 26E1      | VeriPHY 3                                          |
| 27E1–28E1 | Reserved                                           |
| 29E1      | Ethernet packet generator (EPG) 1                  |
| 30E1      | EPG 2                                              |

### 2.3.1 SERDES MEDIA CONTROL

Register 16E1 controls some functions of the SerDes media interface on ports 0–3. These settings are only valid for those ports. The following table shows the setting available in this register.

**TABLE 2-33: SERDES MEDIA CONTROL, ADDRESS 16E1 (0X10)**

| Bit   | Name                                 | Access | Description                                                                                                                | Default |
|-------|--------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------|---------|
| 15:14 | Transmit remote fault                | R/W    | Remote fault indication sent to link partner (LP)                                                                          | 00      |
| 13:12 | Link partner (LP) remote fault       | RO     | Remote fault bits sent by LP during autonegotiation                                                                        | 00      |
| 11:10 | Reserved                             | RO     | Reserved                                                                                                                   | —       |
| 9     | Allow 1000BASE-X link-up             | R/W    | Sticky bit.<br>1: Allow 1000BASE-X fiber media link-up capability<br>0: Suppress 1000BASE-X fiber media link-up capability | 1       |
| 8     | Allow 100BASE-FX link-up             | R/W    | Sticky bit.<br>1: Allow 100BASE-FX fiber media link-up capability<br>0: Suppress 100BASE-FX fiber media link-up capability | 1       |
| 7     | Reserved                             | RO     | Reserved                                                                                                                   | —       |
| 6     | Far end fault detected in 100BASE-FX | RO     | Self-clearing bit.<br>1: Far end fault in 100BASE-FX detected                                                              | 0       |
| 5:0   | Reserved                             | RO     | Reserved                                                                                                                   | —       |

## 2.3.2 CU MEDIA CRC GOOD COUNTER

Register 18E1 makes it possible to read the contents of the CRC good counter for packets that are received on the Cu media interface; the number of CRC routines that have executed successfully. The following table shows the expected readouts.

**TABLE 2-34: CU MEDIA CRC GOOD COUNTER, ADDRESS 18E1 (0X12)**

| Bit  | Name                               | Access | Description                                                                                                                                                                                        | Default |
|------|------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | Packet since last read             | RO     | Self-clearing bit.<br>1: Packet received since last read.                                                                                                                                          | 0       |
| 14   | Reserved                           | RO     | Reserved.                                                                                                                                                                                          | —       |
| 13:0 | Cu Media CRC good counter contents | RO     | Self-clearing bit. Counter containing the number of packets with valid CRCs modulo 10,000; this counter does not saturate and will roll over to zero on the next good packet received after 9,999. | 0x000   |

## 2.3.3 EXTENDED MODE CONTROL

Register 19E1 controls the extended LED and other chip modes. The following table shows the settings available.

**TABLE 2-35: EXTENDED MODE CONTROL, ADDRESS 19E1 (0X13)**

| Bit  | Name                     | Access | Description                                                                                                                                         | Default |
|------|--------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | LED3 Extended Mode       | R/W    | Sticky bit.<br>1: See <a href="#">Section 1.13.2, Extended LED Modes</a>                                                                            | 0       |
| 14   | LED2 Extended Mode       | R/W    | Sticky bit.<br>1: See <a href="#">Section 1.13.2, Extended LED Modes</a>                                                                            | 0       |
| 13   | LED1 Extended Mode       | R/W    | Sticky bit.<br>1: See <a href="#">Section 1.13.2, Extended LED Modes</a>                                                                            | 0       |
| 12   | LED0 Extended Mode       | R/W    | Sticky bit.<br>1: See <a href="#">Section 1.13.2, Extended LED Modes</a>                                                                            | 0       |
| 11   | LED Reset Blink Suppress | R/W    | Sticky bit.<br>1: Blink LEDs after COMA_MODE is de-asserted<br>0: Suppress LED blink after COMA_MODE is de-asserted                                 | 0       |
| 10:5 | Reserved                 | RO     | Reserved                                                                                                                                            | 0       |
| 4    | Fast link failure        | R/W    | Sticky bit.<br>Enable fast link failure pin. This must be done from PHY0 only.<br>1: Enabled<br>0: Disabled (GPIO9 pin becomes general purpose I/O) | 0       |

**TABLE 2-35: EXTENDED MODE CONTROL, ADDRESS 19E1 (0X13) (CONTINUED)**

| Bit | Name                                  | Access | Description                                                                                                                          | Default |
|-----|---------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------|---------|
| 3:2 | Force MDI crossover                   | R/W    | Sticky bits.<br>00: Normal HP Auto-MDIX operation<br>01: Reserved<br>10: Copper media forced to MDI<br>11: Copper media forced MDI-X | 00      |
| 1   | Reserved                              | RO     | Reserved                                                                                                                             | —       |
| 0   | GPIO[1:0]/SIGDET[1:0]<br>pin polarity | R/W    | Sticky bit.<br>1: Active low<br>0: Active high                                                                                       | 0       |

### 2.3.4 ACTIPHY CONTROL

Register 20E1 controls the device ActiPHY sleep timer, its wake-up timer, and its link speed downshifting feature. The following table shows the settings available.

**TABLE 2-36: EXTENDED PHY CONTROL 3, ADDRESS 20E1 (0X14)**

| Bit   | Name                             | Access | Description                                                                                                                                                                                                                                                                       | Default |
|-------|----------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15    | Disable carrier extension        | R/W    | 1: Disable carrier extension in 1000BASE-T copper links                                                                                                                                                                                                                           | 1       |
| 14:13 | ActiPHY sleep timer              | R/W    | Sticky bit.<br>00: 1 second<br>01: 2 seconds<br>10: 3 seconds<br>11: 4 seconds                                                                                                                                                                                                    | 01      |
| 12:11 | ActiPHY wake-up timer            | R/W    | Sticky bit.<br>00: 160 ms<br>01: 400 ms<br>10: 800 ms<br>11: 2 seconds                                                                                                                                                                                                            | 00      |
| 10    | Reserved                         | RO     | Reserved                                                                                                                                                                                                                                                                          | —       |
| 9     | PHY address reversal             | R/W    | Sticky bit.<br>Reverse PHY address<br>Enabling causes physical PHY 0 to have address of 3, PHY 1 address of 2, PHY 2 address of 1, and PHY 3 address of 0.<br>Changing this bit to 1 should initially be done from PHY 0 and changing to 0 from PHY3<br>1: Enabled<br>0: Disabled | 0       |
| 8     | Reserved                         | RO     | Valid only on PHY0                                                                                                                                                                                                                                                                | —       |
| 7:6   | Media mode status                | RO     | 00: No media selected<br>01: Copper media selected<br>10: SerDes media selected<br>11: Reserved                                                                                                                                                                                   | 00      |
| 5     | Enable 10BASE-T no preamble mode | R/W    | Sticky bit.<br>1: 10BASE-T will assert RX_DV indication when data is presented to the receiver even without a preamble preceding it                                                                                                                                               | 0       |

**TABLE 2-36: EXTENDED PHY CONTROL 3, ADDRESS 20E1 (0X14) (CONTINUED)**

| Bit | Name                                    | Access | Description                                                                                                                                                                                                                                                                                  | Default |
|-----|-----------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 4   | Enable link speed autodownshift feature | R/W    | Sticky bit.<br>1: Enable auto link speed downshift from 1000BASE-T                                                                                                                                                                                                                           | 0       |
| 3:2 | Link speed auto downshift control       | R/W    | Sticky bits.<br>00: Downshift after 2 failed 1000BASE-T autonegotiation attempts<br>01: Downshift after 3 failed 1000BASE-T autonegotiation attempts<br>10: Downshift after 4 failed 1000BASE-T autonegotiation attempts<br>11: Downshift after 5 failed 1000BASE-T autonegotiation attempts | 01      |
| 1   | Link speed auto downshift status        | RO     | 0: No downshift<br>1: Downshift is required or has occurred                                                                                                                                                                                                                                  | 0       |
| 0   | Reserved                                | RO     | Reserved                                                                                                                                                                                                                                                                                     | —       |

## 2.3.5 POE AND MISCELLANEOUS FUNCTIONALITY

The register at address 23E1 controls various aspects of inline powering and the CRC error counter in the VSC8552.

**TABLE 2-37: EXTENDED PHY CONTROL 4, ADDRESS 23E1 (0X17)**

| Bit   | Name                                   | Access | Description                                                                                                                                                               | Default |
|-------|----------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:11 | PHY address                            | RO     | PHY address; latched on reset                                                                                                                                             | —       |
| 10    | Inline powered device detection        | R/W    | Sticky bit.<br>1: Enabled                                                                                                                                                 | 0       |
| 9:8   | Inline powered device detection status | RO     | Only valid when bit 10 is set.<br>00: Searching for devices<br>01: Device found; requires inline power<br>10: Device found; does not require inline power<br>11: Reserved | 00      |
| 7:0   | Cu Media CRC error counter             | RO     | Self-clearing bit                                                                                                                                                         | —       |

RC error counter for packets received on the Cu media interface. The value saturates at 0xFF and subsequently clears when read and restarts count.0x00

### 2.3.6 VERIPHY CONTROL 1

Register 24E1 in the extended register space provides control over the device VeriPHY diagnostics features. There are three separate VeriPHY control registers. The following table shows the settings available and describes the expected readouts.

**TABLE 2-38: VERIPHY CONTROL REGISTER 1, ADDRESS 24E1 (0X18)**

| Bit  | Name                   | Access | Description                                                                                                                                                      | Default |
|------|------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | VeriPHY trigger        | R/W    | Self-clearing bit.<br>1: Triggers the VeriPHY algorithm and clears when VeriPHY has completed. Settings in registers 24E–26E become valid after this bit clears. | 0       |
| 14   | VeriPHY valid          | RO     | 1: VeriPHY results in registers 24E–26E are valid.                                                                                                               | 0       |
| 13:8 | Pair A (1, 2) distance | RO     | Loop length or distance to anomaly for pair A (1, 2).                                                                                                            | 0x00    |
| 7:6  | Reserved               | RO     | Reserved.                                                                                                                                                        | —       |
| 5:0  | Pair B (3, 6) distance | RO     | Loop length or distance to anomaly for pair B (3, 6).                                                                                                            | 0x00    |

**Note:** The resolution of the 6-bit length field is 3 meters.

### 2.3.7 VERIPHY CONTROL 2

The register at address 25E1 consists of the second of the three device registers that provide control over VeriPHY diagnostics features. The following table shows the expected readouts.

**TABLE 2-39: VERIPHY CONTROL REGISTER 2, ADDRESS 25E1 (0X19)**

| Bit   | Name                   | Access | Description                                          | Default |
|-------|------------------------|--------|------------------------------------------------------|---------|
| 15:14 | Reserved               | RO     | Reserved                                             | —       |
| 13:8  | Pair C (4, 5) distance | RO     | Loop length or distance to anomaly for pair C (4, 5) | 0x00    |
| 7:6   | Reserved               | RO     | Reserved                                             | —       |
| 5:0   | Pair D (7, 8) distance | RO     | Loop length or distance to anomaly for pair D (7, 8) | 0x00    |

**Note:** The resolution of the 6-bit length field is 3 meters.

### 2.3.8 VERIPHY CONTROL 3

The register at address 26E1 consists of the third of the three device registers that provide control over VeriPHY diagnostics features. Specifically, this register provides information about the termination status (fault condition) for all two link partner pairs. The following table shows the expected readouts.

**TABLE 2-40: VERIPHY CONTROL REGISTER 3, ADDRESS 26E1 (0X1A)**

| Bit   | Name                             | Access | Description                         | Default |
|-------|----------------------------------|--------|-------------------------------------|---------|
| 15:12 | Pair A (1, 2) termination status | RO     | Termination fault for pair A (1, 2) | 0x00    |
| 11:8  | Pair B (3, 6) termination status | RO     | Termination fault for pair B (3, 4) | 0x00    |
| 7:4   | Pair C (4, 5) termination status | RO     | Termination fault for pair C (4, 5) | 0x00    |
| 3:0   | Pair D (7, 8) termination status | RO     | Termination fault for pair D (7, 8) | 0x00    |

The following table shows the meanings for the various fault codes.

**TABLE 2-41: VERIPHY CONTROL REGISTER 3 FAULT CODES**

| Code | Denotes                                  |
|------|------------------------------------------|
| 0000 | Correctly terminated pair                |
| 0001 | Open pair                                |
| 0010 | Shorted pair                             |
| 0100 | Abnormal termination                     |
| 1000 | Cross-pair short to pair A               |
| 1001 | Cross-pair short to pair B               |
| 1010 | Cross-pair short to pair C               |
| 1011 | Cross-pair short to pair D               |
| 1100 | Abnormal cross-pair coupling with pair A |
| 1101 | Abnormal cross-pair coupling with pair B |
| 1110 | Abnormal cross-pair coupling with pair C |
| 1111 | Abnormal cross-pair coupling with pair D |

## 2.3.9 ETHERNET PACKET GENERATOR CONTROL 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two separate EPG control registers. The following table shows the settings available in the first register.

**TABLE 2-42: EPG CONTROL REGISTER 1, ADDRESS 29E1 (0X1D)**

| Bit   | Name                                      | Access | Description                                                                              | Default |
|-------|-------------------------------------------|--------|------------------------------------------------------------------------------------------|---------|
| 15    | EPG enable                                | R/W    | 1: Enable EPG                                                                            | 0       |
| 14    | EPG run or stop                           | R/W    | 1: Run EPG                                                                               | 0       |
| 13    | Transmission duration                     | R/W    | 1: Continuous (sends in 10,000-packet increments)<br>0: Send 30,000,000 packets and stop | 0       |
| 12:11 | Packet length                             | R/W    | 00: 125 bytes<br>01: 64 bytes<br>10: 1518 bytes<br>11: 10,000 bytes (jumbo packet)       | 0       |
| 10    | Interpacket gap                           | R/W    | 1: 8,192 ns<br>0: 96 ns                                                                  | 0       |
| 9:6   | Destination address                       | R/W    | Lowest nibble of the 6-byte destination address                                          | 0001    |
| 5:2   | Source address                            | R/W    | Lowest nibble of the 6-byte destination address                                          | 0000    |
| 1     | Payload type                              | R/W    | 1: Randomly generated payload pattern<br>0: Fixed based on payload pattern               | 0       |
| 0     | Bad frame check sequence (FCS) generation | R/W    | 1: Generate packets with bad FCS<br>0: Generate packets with good FCS                    | 0       |

The following information applies to the EPG control number 1:

- Do not run the EPG when the VSC8552 is connected to a live network.

- bit 29E1.13 (continuous EPG mode control): When enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.
- The 6-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- The 6-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

### 2.3.10 ETHERNET PACKET GENERATOR CONTROL 2

Register 30E1 consists of the second set of bits that provide access to and control over the various aspects of the EPG testing feature. The following table shows the settings available.

**TABLE 2-43: EPG CONTROL REGISTER 2, ADDRESS 30E1 (0X1E)**

| Bit  | Name               | Access | Description                                                          | Default |
|------|--------------------|--------|----------------------------------------------------------------------|---------|
| 15:0 | EPG packet payload | R/W    | Data pattern repeated in the payload of packets generated by the EPG | 0x00    |

**Note:** If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E1 is set to 1), that bit (29E1.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

## 2.4 Extended Page 2 Registers

To access the extended page 2 registers (16E2–30E2), enable extended register access by writing 0x0002 to register 31. For more information, see [Table 2-31](#).

When extended page 2 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E2–30E2 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 2 space. These registers are accessible only when the device register 31 is set to 0x0002.

**TABLE 2-44: EXTENDED REGISTERS PAGE 2 SPACE**

| Address   | Name                    |
|-----------|-------------------------|
| 16E2      | Cu PMD Transmit Control |
| 17E2      | EEE Control             |
| 18E2      | RGMII Settings          |
| 19E2-29E2 | Reserved                |
| 30E2      | Ring Resiliency Control |

### 2.4.1 CU PMD TRANSMIT CONTROL

The register at address 16E2 consists of the bits that provide control over the amplitude settings for the transmit side Cu PMD interface. These bits provide the ability to make small adjustments in the signal amplitude to compensate for minor variations in the magnetics from different vendors. Extreme caution must be exercised when changing these settings from the default values as they have a direct impact on the signal quality. Changing these settings also affects the linearity and harmonic distortion of the transmitted signals. For help with changing these values, contact your Microchip representative.



**TABLE 2-45: CU PMD TRANSMIT CONTROL, ADDRESS 16E2 (0X10)**

| Bit   | Name                                          | Access | Description                                                                                                                                                                                                                                                                       | Default |
|-------|-----------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:12 | 1000BASE-T signal amplitude trim <sup>1</sup> | R/W    | Sticky bits.<br>1000BASE-T signal amplitude<br>1111: -1.7%<br>1110: -2.6%<br>1101: -3.5%<br>1100: -4.4%<br>1011: -5.3%<br>1010: -7%<br>1001: -8.8%<br>1000: -10.6%<br>0111: 5.5%<br>0110: 4.6%<br>0101: 3.7%<br>0100: 2.8%<br>0011: 1.9%<br>0010: 1%<br>0001: 0.1%<br>0000: -0.8% | 0000    |

**TABLE 2-45: CU PMD TRANSMIT CONTROL, ADDRESS 16E2 (0X10) (CONTINUED)**

| Bit  | Name                                          | Access | Description                                                                                                                                                                                                                                                                                                      | Default |
|------|-----------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 11:8 | 100BASE-TX signal amplitude trim <sup>2</sup> | R/W    | Sticky bits.<br>100BASE-TX signal amplitude<br>1111: -1.7%<br>1110: -2.6%<br>1101: -3.5%<br>1100: -4.4%<br>1011: -5.3%<br>1010: -7%<br>1001: -8.8%<br>1000: -10.6%<br>0111 5.5%<br>0110: 4.6%<br>0101: 3.7%<br>0100: 2.8%<br>0011: 1.9%<br>0010: 1%<br>0001: 0.1%<br>0000: -0.8%                                 | 0010    |
| 7:4  | 10BASE-T signal amplitude trim <sup>3</sup>   | R/W    | Sticky bits.<br>10BASE-T signal amplitude<br>1111: -7%<br>1110: -7.9%<br>1101: -8.8%<br>1100: -9.7%<br>1011: -10.6%<br>1010: -11.5%<br>1001: -12.4%<br>1000: -13.3%<br>0111: 0%<br>0110: -0.7%<br>0101: -1.6%<br>0100: -2.5%<br>0011: -3.4%<br>0010: -4.3%<br>0001: -5.2%<br>0000: -6.1%                         | 1011    |
| 3:0  | 10BASE-Te signal amplitude trim               | R/W    | Sticky bits.<br>10BASE-Te signal amplitude<br>1111: -30.45%<br>1110: -31.1%<br>1101: -31.75%<br>1100: -32.4%<br>1011: -33.05%<br>1010: -33.7%<br>1001: -34.35%<br>1000: -35%<br>0111: -25.25%<br>0110: -25.9%<br>0101: -26.55%<br>0100: -27.2%<br>0011: -27.85%<br>0010: -28.5%<br>0001: -29.15%<br>0000: -29.8% | 1110    |

1. Changes to 1000BASE-T amplitude may result in unpredictable side effects.
2. Adjust 100BASE-TX to specific magnetics.
3. Amplitude is limited by  $V_{CC}$  (2.5V).

#### 2.4.2 EEE CONTROL

The register at address 17E2 consists of the bits that provide additional control over the chip behavior in energy efficient Ethernet (IEEE 802.3az-2010) mode.

**TABLE 2-46: EEE CONTROL, ADDRESS 17E2 (0X11)**

| Bit            | Name                                    | Access | Description                                                                                                                                                                                                                                                  | Default |
|----------------|-----------------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15             | Enable 10BASE-Te                        | R/W    | Sticky bit.<br>Enable energy efficient (IEEE 802.3az-2010) 10BASE-Te operating mode.                                                                                                                                                                         | 0       |
| 14             | Enable LED in fiber unidirectional mode | R/W    | Sticky bit.<br>1: Enable LED functions in fiber unidirectional mode.                                                                                                                                                                                         | 0       |
| 13:10          | Invert LED polarity                     | R/W    | Sticky bits.<br>Invert polarity of LED[3:0]_[1:0] signals. Default is to drive an active low signal on the LED pins. This also applies to enhanced serial LED mode. For more information, see <a href="#">Section TABLE 1-10; Enhanced Serial LED Mode</a> . | 0000    |
| 9:6            | Reserved                                | RO     | Reserved.                                                                                                                                                                                                                                                    | —       |
| 5              | Enable 1000BASE-T force mode            | R/W    | Sticky bit.<br>1: Enable 1000BASE-T force mode to allow PHY to link-up in 1000BASE-T mode without forcing master/slave when register 0, bits 6 and 13 are set to 2'b10.                                                                                      | 0       |
| 4 <sup>1</sup> | Force transmit LPI                      | R/W    | Sticky bit.<br>1: Enable the EPG to transmit LPI on the MDI, ignore data from the MAC interface.<br>0: Transmit idles being received from the MAC.                                                                                                           | 0       |
| 3              | Inhibit 100BASE-TX transmit EEE LPI     | R/W    | Sticky bit.<br>1: Disable transmission of EEE LPI on transmit path MDI in 100BASE-TX mode when receiving LPI from MAC.                                                                                                                                       | 0       |
| 2              | Inhibit 100BASE-TX receive EEE LPI      | R/W    | Sticky bit.<br>1: Disable transmission of EEE LPI on receive path MAC interface in 100BASE-TX mode when receiving LPI from the MDI.                                                                                                                          | 0       |
| 1              | Inhibit 1000BASE-T transmit EEE LPI     | R/W    | Sticky bit.<br>1: Disable transmission of EEE LPI on transmit path MDI in 1000BASE-T mode when receiving LPI from MAC.                                                                                                                                       | 0       |
| 0              | Inhibit 1000BASE-T receive EEE LPI      | R/W    | Sticky bit.<br>1: Disable transmission of EEE LPI on receive path MAC interface in 1000BASE-T mode when receiving LPI from the MDI.                                                                                                                          | 0       |

1. 17E2 bits 4:0 are for debugging purposes only, not for operational use.

## 2.4.3 RGMII SETTINGS

The following table shows the register settings for the RGMII setting controls at address 18E2.

**TABLE 2-47: RGMII SETTINGS, ADDRESS 18E2**

| Bit | Name          | Access | Description                                                                                                                                                          | Default |
|-----|---------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 6:4 | rgmii_skew_tx | R/W    | 000: 0.2 ns delay<br>001: 0.8 ns delay<br>010: 1.1 ns delay<br>011: 1.7 ns delay<br>100: 2.0 ns delay<br>101: 2.3 ns delay<br>110: 2.6 ns delay<br>111: 3.4 ns delay | 000     |
| 3:1 | rgmii_skew_rx | R/W    | 000: 0.2 ns delay<br>001: 0.8 ns delay<br>010: 1.1 ns delay<br>011: 1.7 ns delay<br>100: 2.0 ns delay<br>101: 2.3 ns delay<br>110: 2.6 ns delay<br>111: 3.4 ns delay | 000     |
| 0   | rgmii_bit_rev | RO     |                                                                                                                                                                      | 0       |

## 2.4.4 RING RESILIENCY CONTROL

The following table shows the register settings for the ring resiliency controls at address 30E2.

**TABLE 2-48: RING RESILIENCY, ADDRESS 30E2**

| Bit  | Name                                              | Access | Description                                                                                                                                                                           | Default |
|------|---------------------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | Ring resiliency startup enable (master TR enable) | R/W    | Sticky                                                                                                                                                                                | 0       |
| 14   | Advertise ring resiliency                         | R/W    | Sticky                                                                                                                                                                                | 0       |
| 13   | LP ring resiliency advertisement                  | RO     | —                                                                                                                                                                                     | 0       |
| 12   | Force ring resiliency enable (override autoneg)   | R/W    | Sticky                                                                                                                                                                                | 0       |
| 11:6 | Reserved                                          | RO     | Reserved                                                                                                                                                                              | 000000  |
| 5:4  | Ring resiliency status                            | RO     | Ring resiliency status (from r1000 DSP SM)<br>00: Timing slave <sup>1</sup><br>10: Timing slave becoming master<br>11: Timing master <sup>1</sup><br>01: Timing master becoming slave | 11      |
| 3:1  | Reserved                                          | RO     | Reserved                                                                                                                                                                              | 000     |
| 0    | Start switchover (only when not in progress)      | RWSC   | —                                                                                                                                                                                     | 0       |

1. Reflects autoneg master/slave at initial link-up

## 2.5 Extended Page 3 Registers

To access the extended page 3 registers (16E3–30E3), enable extended register access by writing 0x0003 to register 31. For more information, see [Table 2-31](#).

When extended page 3 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E3–30E3 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 3 space. These registers are accessible only when the device register 31 is set to 0x0003.

**TABLE 2-49: EXTENDED REGISTERS PAGE 3 SPACE**

| Address | Name                                        |
|---------|---------------------------------------------|
| 16E3    | MAC SerDes PCS Control                      |
| 17E3    | MAC SerDes PCS Status                       |
| 18E3    | MAC SerDes Clause 37 Advertised Ability     |
| 19E3    | MAC SerDes Clause 37 Link Partner Ability   |
| 20E3    | MAC SerDes Status                           |
| 21E3    | Media SerDes Transmit Good Packet Counter   |
| 22E3    | Media SerDes Transmit CRC Error Counter     |
| 23E3    | Media SerDes PCS Control                    |
| 24E3    | Media SerDes PCS Status                     |
| 25E3    | Media SerDes Clause 37 Advertised Ability   |
| 26E3    | Media SerDes Clause 37 Link Partner Ability |
| 27E3    | Media SerDes status                         |
| 28E3    | Fiber Media CRC Good Counter                |
| 29E3    | Fiber Media CRC Error Counter               |
| 30E3    | Reserved                                    |

### 2.5.1 MAC SERDES PCS CONTROL

The register at address 16E3 consists of the bits that provide access to and control over MAC SerDes PCS block. The following table shows the settings available.

**TABLE 2-50: MAC SERDES PCS CONTROL, ADDRESS 16E3 (0X10)**

| Bit | Name                                  | Access | Description                                                              | Default |
|-----|---------------------------------------|--------|--------------------------------------------------------------------------|---------|
| 15  | MAC interface disable                 | R/W    | Sticky bit.<br>1: 1000BASE-X MAC interface disable when media link down. | 0       |
| 14  | MAC interface restart                 | R/W    | Sticky bit.<br>1: 1000BASE-X MAC interface restart on media link change. | 0       |
| 13  | MAC interface PD enable               | R/W    | Sticky bit.<br>1: MAC interface autonegotiation parallel detect enable.  | 0       |
| 12  | MAC interface autonegotiation restart | R/W    | Self-clearing bit.<br>1: Restart MAC interface autonegotiation.          | 0       |

**TABLE 2-50: MAC SERDES PCS CONTROL, ADDRESS 16E3 (0X10) (CONTINUED)**

| Bit  | Name                              | Access | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Default |
|------|-----------------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 11   | Force advertised ability          | R/W    | 1: Force 16-bit advertised ability from register 18E3.                                                                                                                                                                                                                                                                                                                                                                                                                   | 0       |
| 10:8 | SGMII preamble control            | R/W    | 000: No effect on the start of packet.<br>001: If both the first two nibbles of the 10/100 packet are not 0x5, a byte of 0x55 must be prefixed to the output, otherwise there will be no effect on the start of packet.<br>010: If both the first two nibbles of the 10/100 packet are not 0x5, a byte of 0x55 must be prefixed to the output. An additional byte of 0x55 must be prefixed to the output if the next two nibbles are also not 0x5.<br>011–111: Reserved. | 001     |
| 7    | MAC SerDes autonegotiation enable | R/W    | Sticky bit.<br>1: MAC SerDes ANEG enable.                                                                                                                                                                                                                                                                                                                                                                                                                                | 0       |
| 6    | SerDes polarity at input of MAC   | R/W    | 1: Invert polarity of signal received at input of MAC.                                                                                                                                                                                                                                                                                                                                                                                                                   | 0       |
| 5    | SerDes polarity at output of MAC  | R/W    | 1: Invert polarity of signal at output of MAC.                                                                                                                                                                                                                                                                                                                                                                                                                           | —       |
| 4    | Fast link status enable           | R/W    | 1: Use fast link fail indication as link status indication to MAC SerDes.<br>0: Use normal link status indication to MAC SerDes.                                                                                                                                                                                                                                                                                                                                         | 0       |
| 3    | Reserved                          | R/W    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0       |
| 2:0  | Reserved                          | RO     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                | —       |

## 2.5.2 MAC SERDES PCS STATUS

The register at address 17E3 consists of the bits that provide status from the MAC SerDes PCS block. The following table shows the settings available.

**TABLE 2-51: MAC SERDES PCS STATUS, ADDRESS 17E3 (0X11)**

| Bit   | Name                                     | Access | Description                                                                             |
|-------|------------------------------------------|--------|-----------------------------------------------------------------------------------------|
| 15:13 | Reserved                                 | RO     | Reserved                                                                                |
| 12    | SGMII alignment error                    | RO     | 1: RGMII/SGMII alignment error occurred                                                 |
| 11    | MAC interface LP autonegotiation restart | RO     | 1: MAC interface link partner autonegotiation restart request occurred                  |
| 10    | Reserved                                 | RO     | Reserved                                                                                |
| 9:8   | MAC remote fault                         | RO     | 01, 10, and 11: Remote fault detected from MAC<br>00: No remote fault detected from MAC |
| 7     | Asymmetric pause advertisement           | RO     | 1: Asymmetric pause advertised by MAC                                                   |
| 6     | Symmetric pause advertisement            | RO     | 1: Symmetric pause advertised by MAC                                                    |
| 5     | Full duplex advertisement                | RO     | 1: Full duplex advertised by MAC                                                        |
| 4     | Half duplex advertisement                | RO     | 1: Half duplex advertised by MAC                                                        |
| 3     | MAC interface LP autonegotiation capable | RO     | 1: MAC interface link partner autonegotiation capable                                   |

**TABLE 2-51: MAC SERDES PCS STATUS, ADDRESS 17E3 (0X11) (CONTINUED)**

| Bit | Name                                   | Access | Description                                                    |
|-----|----------------------------------------|--------|----------------------------------------------------------------|
| 2   | MAC interface link status              | RO     | 1: MAC interface link status connected                         |
| 1   | MAC interface autonegotiation complete | RO     | 1: MAC interface autonegotiation complete                      |
| 0   | MAC comma detect                       | RO     | 1: Comma currently detected<br>0: comma currently not detected |

### 2.5.3 MAC SERDES CLAUSE 37 ADVERTISED ABILITY

The register at address 18E3 consists of the bits that provide access to and control over MAC SerDes Clause 37 advertised ability. The following table shows the settings available.

**TABLE 2-52: MAC SERDES CL37 ADVERTISED ABILITY, ADDRESS 18E3 (0X12)**

| Bit  | Name                          | Access | Description                                                                                   | Default |
|------|-------------------------------|--------|-----------------------------------------------------------------------------------------------|---------|
| 15:0 | MAC SerDes advertised ability | R/W    | Current configuration code word being advertised (this register is read/write if 16E3.11 = 1) | 0x01E0  |

### 2.5.4 MAC SERDES CLAUSE 37 LINK PARTNER ABILITY

The register at address 19E3 consists of the bits that provide status of the MAC SerDes link partner's Clause 37 advertised ability. The following table shows the settings available.

**TABLE 2-53: MAC SERDES CL37 LP ABILITY, ADDRESS 19E3 (0X13)**

| Bit  | Name                  | Access | Description                                             |
|------|-----------------------|--------|---------------------------------------------------------|
| 15:0 | MAC SerDes LP ability | RO     | Last configuration code word received from link partner |

### 2.5.5 MAC SERDES STATUS

The register at address 20E3 consists of the bits that provide access to MAC SerDes status. The following table shows the settings available.

**TABLE 2-54: MAC SERDES STATUS, ADDRESS 20E3 (0X14)**

| Bit  | Name               | Access | Description                                                                            |
|------|--------------------|--------|----------------------------------------------------------------------------------------|
| 15   | Reserved           | RO     | Reserved                                                                               |
| 14   | MAC comma detect   | RO     | Super-sticky bit. Cleared upon SW reset.<br>1: Comma detected<br>0: Comma not detected |
| 13   | QSGMII sync status | RO     | —                                                                                      |
| 12:0 | Reserved           | RO     | Reserved                                                                               |

## 2.5.6 MEDIA SERDES TRANSMIT GOOD PACKET COUNTER

The register at address 21E3 consists of the bits that provide status of the media SerDes transmit good packet counter. The following table shows the settings available.

**TABLE 2-55: MEDIA SERDES TX GOOD PACKET COUNTER, ADDRESS 21E3 (0X15)**

| Bit  | Name                          | Access | Description                             |
|------|-------------------------------|--------|-----------------------------------------|
| 15   | Tx good packet counter active | RO     | 1: Transmit good packet counter active  |
| 14   | Reserved                      | RO     | Reserved                                |
| 13:0 | Tx good packet count          | RO     | Transmit good packet count modulo 10000 |

## 2.5.7 MEDIA SERDES TRANSMIT CRC ERROR COUNTER

The register at address 22E3 consists of the bits that provide status of the media SerDes transmit packet count that had a CRC error. The following table shows the settings available.

**TABLE 2-56: MEDIA SERDES TX CRC ERROR COUNTER, ADDRESS 22E3 (0X16)**

| Bit  | Name                | Access | Description                                  |
|------|---------------------|--------|----------------------------------------------|
| 15:8 | Reserved            | RO     | Reserved                                     |
| 7:0  | Tx CRC packet count | RO     | Transmit CRC packet count (saturates at 255) |

## 2.5.8 MEDIA SERDES PCS CONTROL

The register at address 23E3 consists of the bits that provide access to and control over Media SerDes PCS control. The following table shows the settings available.

**TABLE 2-57: MEDIA SERDES PCS CONTROL, ADDRESS 23E3 (0X17)**

| Bit   | Name                                               | Access | Description                                                                                        | Default |
|-------|----------------------------------------------------|--------|----------------------------------------------------------------------------------------------------|---------|
| 15:14 | Reserved                                           | RO     | Reserved                                                                                           | —       |
| 13    | Media interface autonegotiation parallel-detection | R/W    | Sticky bit.<br>1: SerDes media autonegotiation parallel detect enabled                             | 0       |
| 12    | Reserved                                           | RO     | Reserved                                                                                           | —       |
| 11    | Force advertised ability                           | R/W    | 1: Force 16-bit advertised ability from register 25E3.15:0                                         | 0       |
| 10:7  | Reserved                                           | RO     | Reserved                                                                                           | —       |
| 6     | Polarity reversal input                            | —      | Media SerDes polarity reversal input<br>0: No polarity reversal (default)<br>1: Polarity reversed  | 0       |
| 5     | Polarity reversal output                           | —      | Media SerDes polarity reversal output<br>0: No polarity reversal (default)<br>1: Polarity reversed | 0       |
| 4:0   | Reserved                                           | RO     | Reserved                                                                                           | —       |

### 2.5.9 MEDIA SERDES PCS STATUS

The register at address 24E3 consists of the bits that provide status of the Media SerDes PCS block. The following table shows the settings available.

**TABLE 2-58: MEDIA SERDES PCS STATUS, ADDRESS 24E3 (0X18)**

| Bit   | Name                                                 | Access | Description                                                              |
|-------|------------------------------------------------------|--------|--------------------------------------------------------------------------|
| 15:14 | Reserved                                             | RO     | Reserved                                                                 |
| 13    | SerDes protocol transfer                             | RO     | 100 Mb or 100BASE-FX link status                                         |
| 12    | SerDes protocol transfer                             | RO     | 10 Mb link status                                                        |
| 11    | Media interface link partner autonegotiation restart | RO     | 1: Media interface link partner autonegotiation restart request occurred |
| 10    | Reserved                                             | RO     | Reserved                                                                 |
| 9:8   | Remote fault detected                                | RO     | 01, 10, 11: Remote fault detected from link partner                      |
| 7     | Link partner asymmetric pause                        | RO     | 1: Asymmetric pause advertised by link partner                           |
| 6     | Link partner symmetric pause                         | RO     | 1: Symmetric pause advertised by link partner                            |
| 5     | Link partner full duplex advertisement               | RO     | 1: Full duplex advertised by link partner                                |
| 4     | Link partner half duplex advertisement               | RO     | 1: Half duplex advertised by link partner                                |
| 3     | Link partner autonegotiation capable                 | RO     | 1: Media interface link partner autonegotiation capable                  |
| 2     | Media interface link status                          | RO     | 1: Media interface link status                                           |
| 1     | Media interface autonegotiation complete             | RO     | 1: Media interface autonegotiation complete                              |
| 0     | Reserved                                             |        | Reserved                                                                 |

### 2.5.10 MEDIA SERDES CLAUSE 37 ADVERTISED ABILITY

The register at address 25E3 consists of the bits that provide access to and control over Media SerDes Clause 37 advertised ability. The following table shows the settings available.

**TABLE 2-59: MEDIA SERDES CL37 ADVERTISED ABILITY, ADDRESS 25E3 (0X19)**

| Bit  | Name                            | Access | Description                                                                                     | Default |
|------|---------------------------------|--------|-------------------------------------------------------------------------------------------------|---------|
| 15:0 | Media SerDes advertised ability | R/W    | Current configuration code word being advertised. This register is read/write when 23E3.11 = 1. | 0x0000  |

### 2.5.11 MEDIA SERDES CLAUSE 37 LINK PARTNER ABILITY

The register at address 26E3 consists of the bits that provide status of the media SerDes link partner's Clause 37 advertised ability. The following table shows the settings available.

**TABLE 2-60: MAC SERDES CL37 LP ABILITY, ADDRESS 26E3 (0X1A)**

| Bit  | Name                    | Access | Description                                             |
|------|-------------------------|--------|---------------------------------------------------------|
| 15:0 | Media SerDes LP ability | RO     | Last configuration code word received from link partner |

## 2.5.12 MEDIA SERDES STATUS

The register at address 27E3 consists of the bits that provide access to Media SerDes status. The following table shows the settings available.

**TABLE 2-61: MEDIA SERDES STATUS, ADDRESS 27E3 (0X1B)**

| Bit  | Name                    | Access | Description                                                     |
|------|-------------------------|--------|-----------------------------------------------------------------|
| 15   | K28.5 comma realignment | RO     | Self-clearing bit.<br>1: K28.5 comma re-alignment has occurred  |
| 14   | Signal detect           | RO     | Self-clearing bit. Sticky bit.<br>1: SerDes media signal detect |
| 13:0 | Reserved                | RO     | Reserved                                                        |

## 2.5.13 FIBER MEDIA CRC GOOD COUNTER

Register 28E3 makes it possible to read the contents of the CRC good counter for packets that are received on the Fiber media interface; the number of CRC routines that have executed successfully. The following table shows the expected readouts.

**TABLE 2-62: FIBER MEDIA CRC GOOD COUNTER, ADDRESS 28E3 (0X1C)**

| Bit  | Name                                  | Access | Description                                                                                                                     | Default |
|------|---------------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | Packet since last read                | RO     | Self-clearing bit.<br>1: Packet received since last read.                                                                       | 0       |
| 14   | Reserved                              | RO     | Reserved.                                                                                                                       | —       |
| 13:0 | Fiber media CRC good counter contents | RO     | Self-clearing bit. Counter containing the number of packets with valid CRCs. This counter does not saturate and will roll over. | 0x000   |

## 2.5.14 FIBER MEDIA CRC ERROR COUNTER

Register 29E3 makes it possible to read the contents of the CRC error counter for packets that are received on the Fiber media interface. The following table shows the expected readouts.

**TABLE 2-63: FIBER MEDIA CRC ERROR COUNTER, ADDRESS 29E3 (0X1D)**

| Bit  | Name                          | Access | Description                                                                                                                                                               | Default |
|------|-------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:8 | Reserved                      | RO     | Reserved.                                                                                                                                                                 | —       |
| 7:0  | Fiber Media CRC error counter | RO     | Self-clearing bit. CRC error counter for packets received on the Fiber media interface. The value saturates at 0xFF and subsequently clears when read and restarts count. | 0x00    |

## 2.6 General Purpose Registers

Accessing the general purpose register space is similar to accessing the extended page registers. Set register 31 to 0x0010. This sets all 32 registers to the general purpose register space.

To restore main register page access, write 0x0000 to register 31.

The following table lists the addresses and register names in the general purpose register page space. These registers are accessible only when the device register 31 is set to 0x0010. All general purpose register bits are super-sticky.

**TABLE 2-64: GENERAL PURPOSE REGISTERS PAGE SPACE**

| Address | Name                                 |
|---------|--------------------------------------|
| 0G–12G  | Reserved                             |
| 13G     | LED/SIGDET/GPIO Control              |
| 14G     | GPIO Control 2                       |
| 15G     | GPIO Input                           |
| 16G     | GPIO Output                          |
| 17G     | GPIO Output Enable                   |
| 18G     | Micro Command                        |
| 19G     | MAC Mode and Fast Link Configuration |
| 20G     | Two-Wire Serial MUX Control 1        |
| 21G     | Two-Wire Serial MUX Control 2        |
| 22G     | Two-Wire Serial MUX Data Read/Write  |
| 23G     | Recovered Clock 0 Control            |
| 24G     | Recovered Clock 1 Control            |
| 25G     | Enhanced LED Control                 |
| 26G     | Reserved                             |
| 27G     | Reserved                             |
| 28G     | Reserved                             |
| 29G     | Global Interrupt Status              |
| 30G     | Extended Revision ID                 |

### 2.6.1 RESERVED GENERAL PURPOSE ADDRESS SPACE

The bits in registers 0G to 12G of the general purpose register space are reserved.

### 2.6.2 SIGDET/GPIO CONTROL

The SIGDET control bits configure the GPIO[1:0]/SIGDET[1:0] pins to function either as signal detect pins for each fiber media port, or as GPIOs. The following table shows the values that can be written.

**TABLE 2-65: SIGDET/GPIO CONTROL, ADDRESS 13G (0X0D)**

| Bit   | Name            | Access | Description                                                                                                 | Default |
|-------|-----------------|--------|-------------------------------------------------------------------------------------------------------------|---------|
| 15:12 | Reserved        | RO     | Reserved                                                                                                    | 00      |
| 11:10 | GPIO5/I2C_SCL_1 | R/W    | 00: SCL for PHY1<br>01: Reserved<br>10: Reserved<br>11: Controlled by MII registers 15G to 17G <sup>1</sup> | 00      |
| 9:8   | GPIO4/I2C_SCL_0 | R/W    | 00: SCL for PHY0<br>01: Reserved<br>10: Reserved<br>11: Controlled by MII registers 15G to 17G <sup>2</sup> | 00      |

**TABLE 2-65: SIGDET/GPIO CONTROL, ADDRESS 13G (0X0D) (CONTINUED)**

| Bit | Name                  | Access | Description                                                                                        | Default |
|-----|-----------------------|--------|----------------------------------------------------------------------------------------------------|---------|
| 7:4 | Reserved              | RO     | Reserved                                                                                           | 00      |
| 3:2 | GPIO1/SIGDET1 control | R/W    | 00: SIGDET operation<br>01: Reserved<br>10: Reserved<br>11: Controlled by MII registers 15G to 17G | 00      |
| 1:0 | GPIO0/SIGDET0 control | R/W    | 00: SIGDET operation<br>01: Reserved<br>10: Reserved<br>11: Controlled by MII registers 15G to 17G | 00      |

1. Register 20G bit 1 must be clear in order for this setting to take effect.
2. Register 20G bit 0 must be clear in order for this setting to take effect.

## 2.6.3 GPIO CONTROL 2

The GPIO control 2 register configures the functionality of the COMA\_MODE input pins, and provides control for possible GPIO pin options.

**TABLE 2-66: GPIO CONTROL 2, ADDRESS 14G (0X0E)**

| Bit   | Name                                     | Access | Description                                                                                                                                                                                                                                                 | Default |
|-------|------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:14 | GPIO12 and GPIO13                        | R/W    | GPIO12 and GPIO13 control.<br>00: Reserved<br>01: Reserved.<br>10: Reserved.<br>11: GPIO12/GPIO13 operation. Controlled by MII registers 15G to 17G.                                                                                                        | —       |
| 13    | COMA_MODE output enable (active low)     | R/W    | 1: COMA_MODE pin is an input.<br>0: COMA_MODE pin is an output.                                                                                                                                                                                             | 1       |
| 12    | COMA_MODE output data                    | R/W    | Value to output on the COMA_MODE pin when it is configured as an output.                                                                                                                                                                                    | 0       |
| 11    | COMA_MODE input data                     | RO     | Data read from the COMA_MODE pin.                                                                                                                                                                                                                           | —       |
| 10    | Tri-state enable for two-wire serial bus | R/W    | 1: Tri-states two-wire serial bus output signals instead of driving them high. This allows those signals to be pulled above VDD25 using an external pull-up resistor.<br>0: Drive two-wire serial bus output signals to high and low values as appropriate. | 1       |
| 9     | Tri-state enable for LEDs                | R/W    | 1: Tri-state LED output signals instead of driving them high. This allows the signals to be pulled above V <sub>DDIO</sub> using an external pull-up resistor.<br>0: Drive LED bus output signals to high and low values.                                   | 1       |
| 8     | Reserved                                 | RO     | Reserved                                                                                                                                                                                                                                                    | 0       |
| 7:6   | GPIO11/1588_PPS_0                        | R/W    | GPIO11/1588_PPS_0 control.<br>00:<br>01: Reserved<br>10: Reserved<br>11: Controlled by MII registers 15G to 17G                                                                                                                                             | —       |

**TABLE 2-66: GPIO CONTROL 2, ADDRESS 14G (0X0E) (CONTINUED)**

| Bit | Name                | Access | Description                                                                                                                               | Default |
|-----|---------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 5:4 | GPIO10              | R/W    | GPIO10 control.<br>00: Reserved<br>01: Reserved<br>10: Reserved<br>11: Controlled by MII registers 15G to 17G                             | —       |
| 3:2 | GPIO9/FASTLINK_FAIL | R/W    | GPIO9/FASTLINK_FAIL control.<br>00: FASTLINK_FAIL operation<br>01: Reserved<br>10: Reserved<br>11: Controlled by MII registers 15G to 17G | —       |
| 1:0 | GPIO8/I2C_SDA       | R/W    | GPIO8/I2C_SDA control.<br>00: I2C_SDA operation<br>01: Reserved<br>10: Reserved<br>11: Controlled by MII registers 15G to 17G             | —       |

#### 2.6.4 GPIO INPUT

The input register contains information about the input to the device GPIO pins. Read from this register to access the data on the device GPIO pins. The following table shows the readout you can expect.

**TABLE 2-67: GPIO INPUT, ADDRESS 15G (0X0F)**

| Bit   | Name                | Access | Description               | Default |
|-------|---------------------|--------|---------------------------|---------|
| 15:14 | Reserved            | RO     | Reserved                  | 00      |
| 13    | GPIO13              | RO     | GPIO13 input              | 1       |
| 12    | GPIO12              | RO     | GPIO12 input              | 1       |
| 11    | GPIO11              | RO     | GPIO11 input              | 0       |
| 10    | GPIO10              | RO     | GPIO10 input              | 0       |
| 9     | GPIO9/FASTLINK_FAIL | RO     | GPIO9/FASTLINK_FAIL input | 1       |
| 8     | GPIO8/I2C_SDA       | RO     | GPIO8/I2C_SDA input       | 1       |
| 7:6   | Reserved            | RO     | Reserved                  | 0       |
| 5     | GPIO5/I2C_SCL_1     | RO     | GPIO5/I2C_SCL_1 input     | 1       |
| 4     | GPIO4/I2C_SCL_0     | RO     | GPIO4/I2C_SCL_0 input     | 1       |
| 3:2   | Reserved            | RO     | Reserved                  | —       |
| 1     | GPIO1/SIGDET1       | RO     | GPIO1/SIGDET1 input       | 1       |
| 0     | GPIO0/SIGDET0       | RO     | GPIO0/SIGDET0 input       | 0       |

## 2.6.5 GPIO OUTPUT

The output register allows you to access and control the output from the device GPIO pins. The following table shows the values you can write.

**TABLE 2-68: GPIO OUTPUT, ADDRESS 16G (0X10)**

| Bit   | Name                | Access | Description                | Default |
|-------|---------------------|--------|----------------------------|---------|
| 15:14 | Reserved            | RO     | Reserved                   | —       |
| 13    | GPIO13              | R/W    | GPIO13 output              | 0       |
| 12    | GPIO12              | R/W    | GPIO12 output              | 0       |
| 11    | GPIO11              | R/W    | GPIO11 output              | 0       |
| 10    | GPIO10              | R/W    | GPIO10 output              | 0       |
| 9     | GPIO9/FASTLINK_FAIL | R/W    | GPIO9/FASTLINK_FAIL output | 0       |
| 8     | GPIO8/I2C_SDA       | R/W    | GPIO8/I2C_SDA output       | 0       |
| 7:6   | Reserved            | RO     | Reserved                   | 0       |
| 5     | GPIO5/I2C_SCL_1     | R/W    | GPIO5/I2C_SCL_1 output     | 0       |
| 4     | GPIO4/I2C_SCL_0     | R/W    | GPIO4/I2C_SCL_0 output     | 0       |
| 3:2   | Reserved            | RO     | Reserved                   | —       |
| 1     | GPIO1/SIGDET1       | R/W    | GPIO1/SIGDET1 output       | 0       |
| 0     | GPIO0/SIGDET0       | R/W    | GPIO0/SIGDET0 output       | 0       |

## 2.6.6 GPIO PIN CONFIGURATION

Register 17G in the GPIO register space controls whether a particular GPIO pin functions as an input or an output. The following table shows the settings available.

**TABLE 2-69: GPIO INPUT/OUTPUT CONFIGURATION, ADDRESS 17G (0X11)**

| Bit   | Name                | Access | Description                       | Default |
|-------|---------------------|--------|-----------------------------------|---------|
| 15:14 | Reserved            | RO     | Reserved                          | —       |
| 13    | GPIO13              | R/W    | GPIO13 output enable              | 0       |
| 12    | GPIO12              | R/W    | GPIO12 output enable              | 0       |
| 11    | GPIO11              | R/W    | GPIO11 output enable              | 0       |
| 10    | GPIO10              | R/W    | GPIO10 output enable              | 0       |
| 9     | GPIO9/FASTLINK_FAIL | R/W    | GPIO9/FASTLINK_FAIL output enable | 0       |
| 8     | GPIO8/I2C_SDA       | R/W    | GPIO8/I2C_SDA output enable       | 0       |
| 7:6   | Reserved            | RO     | Reserved                          | 0       |
| 5     | GPIO5/I2C_SCL_1     | R/W    | GPIO5/I2C_SCL_1 output enable     | 0       |
| 4     | GPIO4/I2C_SCL_0     | R/W    | GPIO4/I2C_SCL_0 output enable     | 0       |
| 3:2   | Reserved            | RO     | Reserved                          | —       |
| 1     | GPIO1/SIGDET1       | R/W    | GPIO1/SIGDET1 output enable       | 0       |
| 0     | GPIO0/SIGDET0       | R/W    | GPIO0/SIGDET0 output              | 0       |

### 2.6.7 MICROPROCESSOR COMMAND

Register 18G is a command register. Bit 15 tells the internal processor to execute the command. When bit 15 is cleared the command has completed. Software needs to wait until bit 15 = 0 before proceeding with the next PHY register access. Bit 14 = 1 typically indicates an error condition where the squelch patch was not loaded. Use the following steps to execute the command:

1. Write desired command
2. Check bit 15 (move existing text)
3. Check bit 14 (if set, then error)

Commands may take up to 25 ms to complete before bit 15 changes to 0.

**Note:** All MAC interfaces must be the same — all QSGMII, RGMII, or SGMII.

**TABLE 2-70: MICROPROCESSOR COMMAND REGISTER, ADDRESS 18G**

| Command                                 | Setting             |
|-----------------------------------------|---------------------|
| Enable 2 ports MAC SGMII                | 0x80F0              |
| Enable 2 ports MAC 1/2 QSGMII           | 0x80E0              |
| QSGMII transmitter control <sup>1</sup> | —                   |
| Enable 2 ports Media 1000BASE-X         | 0x8FC1 <sup>2</sup> |
| Enable 2 ports Media 100BASE-FX         | 0x8FD1 <sup>2</sup> |

1. Contact your Microchip representative for an initialization script that greatly simplifies the programming of QSGMII transmit controls.
2. The “F” in the command has a bit representing each of the four PHYs. To exclude a PHY from the configuration, set its bit to 0. For example, the configuration of PHY 3 and PHY 2 to 1000BASE-X would be 1100 or a “C” and the command would be 0x8CC1.

### 2.6.8 MAC CONFIGURATION AND FAST LINK

Register 19G in the GPIO register space controls the MAC interface mode and the selection of the source PHY for the fast link failure indication. The following table shows the settings available for the GPIO9/FASTLINK-FAIL pin.

**TABLE 2-71: MAC CONFIGURATION AND FAST LINK REGISTER, ADDRESS 19G (0X13)**

| Bit   | Name                           | Access | Description                                                                                                                         | Default |
|-------|--------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:14 | MAC configuration              | R/W    | Select MAC interface mode<br>00: SGMII<br>01: QSGMII<br>10: RGMII<br>11: Reserved                                                   | 00      |
| 13:4  | Reserved                       | RO     | Reserved                                                                                                                            | —       |
| 3:0   | Fast link failure port setting | R/W    | Select fast link failure PHY source<br>0000: Port0<br>0001: Port1<br>0010: Reserved<br>0011: Reserved<br>1100–1111: Output disabled | 0xF     |

## 2.6.9 TWO-WIRE SERIAL MUX CONTROL 1

The following table shows the settings available to control the integrated two-wire serial MUX.

**TABLE 2-72: TWO-WIRE SERIAL MUX CONTROL 1, ADDRESS 20G (0X14)**

| Bit  | Name                                | Access | Description                                                                                                                                                                 | Default |
|------|-------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Two-wire serial device address      | R/W    | Top 7 bits of the 8-bit address sent out on the two wire serial stream. The bottom bit is the read/write signal, which is controlled by register 21G, bit 8. SFPs use 0xA0. | 0xA0    |
| 8:6  | Reserved                            | RO     | Reserved.                                                                                                                                                                   | —       |
| 5:4  | Two-wire serial SCL clock frequency | R/W    | 00: 50 kHz<br>01: 100 kHz<br>10: 400 kHz<br>11: 2 MHz                                                                                                                       | 01      |
| 3    | Two-wire serial MUX port 3 enable   | R/W    | 1: Enabled.<br>0: Two-wire serial disabled. Becomes GPIO pin.                                                                                                               | 0       |
| 2    | Two-wire serial MUX port 2 enable   | R/W    | 1: Enabled.<br>0: Two-wire serial disabled. Becomes GPIO pin.                                                                                                               | 0       |
| 1    | Two-wire serial MUX port 1 enable   | R/W    | 1: Enabled.<br>0: Two-wire serial disabled. Becomes GPIO pin.                                                                                                               | 0       |
| 0    | Two-wire serial MUX port 0 enable   | R/W    | 1: Enabled.<br>0: Two-wire serial disabled. Two-wire serial MUX port 0 becomes GPIO pin if serial LED function is enabled, regardless of the settings of this bit.          | 0       |

## 2.6.10 TWO-WIRE SERIAL MUX CONTROL 2

Register 21G is used to control the two-wire serial MUX for status and control of two-wire serial slave devices.

**TABLE 2-73: TWO-WIRE SERIAL MUX INTERFACE STATUS AND CONTROL, ADDRESS 21G (0X15)**

| Bit   | Name                              | Access | Description                                                                                                                | Default |
|-------|-----------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------|---------|
| 15    | Two-wire serial MUX ready         | RO     | 1: Two-wire serial MUX is ready for read or write                                                                          | 1       |
| 14:12 | Reserved                          | RO     | Reserved                                                                                                                   | —       |
| 11:10 | PHY port Address                  | R/W    | Specific VSC8552 PHY port being addressed.                                                                                 | 00      |
| 9     | Enable two-wire serial MUX access | R/W    | Self-clearing bit.<br>1: Execute read or write through the two-wire serial MUX based on the settings of register bit 21G.8 | 0       |
| 8     | Two-wire serial MUX read or write | R/W    | 1: Read from two-wire serial MUX<br>0: Write to two-wire serial MUX                                                        | 1       |
| 7:0   | Two-wire serial MUX address       | R/W    | Sets the address of the two-wire serial MUX used to direct read or write operations.                                       | 0x00    |

## 2.6.11 TWO-WIRE SERIAL MUX DATA READ/WRITE

Register 22G in the extended register space enables access to the two-wire serial MUX.

**TABLE 2-74: TWO-WIRE SERIAL MUX DATA READ/WRITE, ADDRESS 22G (0X16)**

| Bit  | Name                           | Access | Description                                                                                        | Default |
|------|--------------------------------|--------|----------------------------------------------------------------------------------------------------|---------|
| 15:8 | Two-wire serial MUX read data  | RO     | Eight-bit data read from two-wire serial MUX; requires setting both register 21G.9 and 21G.8 to 1. | —       |
| 7:0  | Two-wire serial MUX write data | R/W    | Eight-bit data to be written to two-wire serial MUX.                                               | 0x00    |

## 2.6.12 RECOVERED CLOCK 1 CONTROL

Register 23G in the extended register space controls the functionality of the recovered clock 1 output signal.

**TABLE 2-75: RECOVERED CLOCK 1 CONTROL, ADDRESS 23G (0X17)**

| Bit   | Name                   | Access | Description                                                                                                                                 | Default |
|-------|------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15    | Enable RCVRDCLK1       | R/W    | 1: Enable recovered clock 1 output<br>0: Disable recovered clock 1 output                                                                   | 0       |
| 14:11 | Clock source select    | R/W    | Select bits for source PHY for recovered clock:<br>0000: PHY0<br>0001: PHY1<br>0100–1111: Reserved                                          | 0000    |
| 10:8  | Clock frequency select | R/W    | Select output clock frequency:<br>000: 25 MHz output clock<br>001: 125 MHz output clock<br>010: 31.25 MHz output clock<br>011–111: Reserved | 000     |
| 7:6   | Reserved               | RO     | Reserved.                                                                                                                                   | —       |

**TABLE 2-75: RECOVERED CLOCK 1 CONTROL, ADDRESS 23G (0X17) (CONTINUED)**

| Bit | Name                              | Access | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Default |
|-----|-----------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 5:4 | Clock squelch level               | R/W    | <p>Select clock squelch level</p> <p>00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave).</p> <p>01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE.</p> <p>10: Squelch only when the link is not up.</p> <p>11: Disable clock squelch.</p> <p><b>Note:</b> A clock from the SerDes or Cu PHY will be output on the recovered clock output in this mode when the link is down.</p> <p>When the CLK_SQUELCH_IN pin is set high, it squelches the recovered clocks regardless of bit settings.</p> | —       |
| 3   | Reserved                          | RO     | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | —       |
| 2:0 | Clock selection for specified PHY | R/W    | <p>000: Serial media recovered clock</p> <p>001: Copper PHY recovered clock</p> <p>010: Copper PHY transmitter TCLK</p> <p>011–111: Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 000     |

## 2.6.13 RECOVERED CLOCK 2 CONTROL

Register 24G in the extended register space controls the functionality of the recovered clock 2 output signal.

**TABLE 2-76: RECOVERED CLOCK 2 CONTROL, ADDRESS 24G (0X18)**

| Bit   | Name                   | Access | Description                                                                                                                                                        | Default |
|-------|------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15    | Enable RCVRDCLK2       | R/W    | Enable recovered clock 2 output                                                                                                                                    | 0       |
| 14:11 | Clock source select    | R/W    | <p>Select bits for source PHY for recovered clock:</p> <p>0000: PHY0</p> <p>0001: PHY1</p> <p>0100–1111: Reserved</p>                                              | 0000    |
| 10:8  | Clock frequency select | R/W    | <p>Select output clock frequency:</p> <p>000: 25 MHz output clock</p> <p>001: 125 MHz output clock</p> <p>010: 31.25 MHz output clock</p> <p>011–111: Reserved</p> | 000     |
| 7:6   | Reserved               | RO     | Reserved                                                                                                                                                           | —       |

**TABLE 2-76: RECOVERED CLOCK 2 CONTROL, ADDRESS 24G (0X18) (CONTINUED)**

| Bit | Name                              | Access | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Default |
|-----|-----------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 5:4 | Clock squelch level               | R/W    | <p>Select clock squelch level:</p> <p>00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave).</p> <p>01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE</p> <p>10: Squelch only when the link is not up</p> <p>11: Disable clock squelch.</p> <p><b>Note:</b> A clock from the SerDes or Cu PHY will be output on the recovered clock output in this mode when the link is down.</p> <p><b>Note:</b> A clock from the SerDes or Cu PHY will be output on the recovered clock output in this mode when the link is down.</p> <p>When the CLK_SQUELCH_IN pin is set high, it squelches the recovered clocks regardless of bit settings.</p> | —       |
| 3   | Reserved                          | RO     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | —       |
| 2:0 | Clock selection for specified PHY | R/W    | <p>000: Serial media recovered clock</p> <p>001: Copper PHY recovered clock</p> <p>010–111: Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 000     |

#### 2.6.14 ENHANCED LED CONTROL

The following table contains the bits to control advanced functionality of the parallel and serial LED signals.

**TABLE 2-77: ENHANCED LED CONTROL, ADDRESS 25G (0X19)**

| Bit  | Name                                     | Access | Description                                                                                                                                                                                                                                                                      | Default |
|------|------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:8 | LED pulsing duty cycle control           | R/W    | <p>Programmable control for LED pulsing duty cycle when bit 30.12 is set to 1. Valid settings are between 0 and 198. A setting of 0 corresponds to a 0.5% duty cycle and 198 corresponds to a 99.5% duty cycle. Intermediate values change the duty cycle in 0.5% increments</p> | 00      |
| 7    | Port 1 enhanced serial LED output enable | R/W    | <p>Enable the enhanced serial LED output functionality for port 1 LED pins.</p> <p>1: Enhanced serial LED outputs</p> <p>0: Normal function</p>                                                                                                                                  | 0       |
| 6    | Port 0 enhanced serial LED output enable | R/W    | <p>Enable the enhanced serial LED output functionality for port 0 LED pins.</p> <p>1: Enhanced serial LED outputs</p> <p>0: Normal function</p>                                                                                                                                  | 0       |

**TABLE 2-77: ENHANCED LED CONTROL, ADDRESS 25G (0X19) (CONTINUED)**

| Bit | Name                            | Access | Description                                                                                                                                                                                                                                                                                             | Default |
|-----|---------------------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 5:3 | Serial LED frame rate selection | R/W    | Select frame rate of serial LED stream<br>000: 2500 Hz frame rate<br>001: 1000 Hz frame rate<br>010: 500 Hz frame rate<br>011: 250 Hz frame rate<br>100: 200 Hz frame rate<br>101: 125 Hz frame rate<br>110: 40 Hz frame rate<br>111: Output basic serial LED stream<br>See <a href="#">Table 1-9</a> . | —       |
| 2:1 | Serial LED select               | R/W    | Select which LEDs from each PHY to enable on the serial stream<br>00: Enable all four LEDs of each PHY<br>01: Enable LEDs 2, 1 and 0 of each PHY<br>10: Enable LEDs 1 and 0 of each PHY<br>11: Enable LED 0 of each PHY                                                                                 | 00      |
| 0   | LED port swapping               | R/W    | See <a href="#">Section 1.13.5, LED Port Swapping</a> .                                                                                                                                                                                                                                                 | —       |

## 2.6.15 GLOBAL INTERRUPT STATUS

The following table contains the interrupt status from the various sources to indicate which one caused that last interrupt on the pin.

**TABLE 2-78: GLOBAL INTERRUPT STATUS, ADDRESS 29G (0X1D)**

| Bit  | Name                               | Access | Default | Description                                                                                             |
|------|------------------------------------|--------|---------|---------------------------------------------------------------------------------------------------------|
| 15:2 | Reserved                           | RO     | 0x07FF  | Reserved                                                                                                |
| 1    | PHY1 interrupt source <sup>1</sup> | RO     | 1       | PHY1 interrupt source indication<br>0: PHY1 caused the interrupt<br>1: PHY1 did not cause the interrupt |
| 0    | PHY0 interrupt source <sup>1</sup> | RO     | 1       | PHY0 interrupt source indication<br>0: PHY0 caused the interrupt<br>1: PHY0 did not cause the interrupt |

1. This bit is set to 1 when the corresponding PHY's Interrupt Status register 26 (0x1A) is read.

## 2.6.16 EXTENDED REVISION ID

The following table lists the extended revision ID information.

**TABLE 2-79: EXTENDED REVISION ID, ADDRESS 30G (0X1E)**

| Bit  | Name       | Access | Default | Description |
|------|------------|--------|---------|-------------|
| 15:1 | Reserved   | RO     | 0x0000  | Reserved    |
| 0    | Ext Rev ID | RO     | 0x1     | Revision E  |

## 2.7 Clause 45 Registers to Support Energy Efficient Ethernet and 802.3bf

This section describes the Clause 45 registers that are required to support energy efficient Ethernet. Access to these registers is through the IEEE standard registers 13 and 14 (MMD access control and MMD data or address registers) as described in section 4.2.11 and 4.2.12.

The following table lists the addresses and register names in the Clause 45 register page space. When the link is down, 0 is the value returned for the x.180x addresses.

**TABLE 2-80: CLAUSE 45 REGISTERS PAGE SPACE**

| Address | Name                                                                           |
|---------|--------------------------------------------------------------------------------|
| 1.1801  | Tx maximum delay through PHY                                                   |
| 1.1803  | Tx minimum delay through PHY                                                   |
| 1.1805  | Rx maximum delay through PHY                                                   |
| 1.1807  | Rx minimum delay through PHY                                                   |
| 3.1     | PCS status 1                                                                   |
| 3.20    | EEE capability                                                                 |
| 3.22    | EEE wake error counter                                                         |
| 4.1801  | Tx maximum delay through xMII (RGMI, SGMII, QSGMII, including FIFO variations) |
| 4.1803  | Tx minimum delay through xMII (RGMI, SGMII, QSGMII, including FIFO variations) |
| 4.1805  | Rx maximum delay through xMII (RGMI, SGMII, QSGMII, including FIFO variations) |
| 4.1807  | Rx minimum delay through xMII (RGMI, SGMII, QSGMII, including FIFO variations) |
| 7.60    | EEE advertisement                                                              |
| 7.61    | EEE link partner advertisement                                                 |

#### 2.7.1 PCS STATUS 1

The bits in the PCS Status 1 register provide a status of the EEE operation from the PCS for the link that is currently active.

**TABLE 2-81: PCS STATUS 1, ADDRESS 3.1**

| Bit   | Name                    | Access | Description                                                                   |
|-------|-------------------------|--------|-------------------------------------------------------------------------------|
| 15:12 | Reserved                | RO     | Reserved                                                                      |
| 11    | Tx LPI received         | RO/LH  | 1: Tx PCS has received LPI<br>0: LPI not received                             |
| 10    | Rx LPI received         | RO/LH  | 1: Rx PCS has received LPI<br>0: LPI not received                             |
| 9     | Tx LPI indication       | RO     | 1: Tx PCS is currently receiving LPI<br>0: PCS is not currently receiving LPI |
| 8     | Rx LPI indication       | RO     | 1: Rx PCS is currently receiving LPI<br>0: PCS is not currently receiving LPI |
| 7:3   | Reserved                | RO     | Reserved                                                                      |
| 2     | PCS receive link status | RO     | 1: PCS receive link up<br>0: PCS receive link down                            |
| 1:0   | Reserved                | RO     | Reserved                                                                      |

## 2.7.2 EEE CAPABILITY

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The following table shows the bit assignments for the EEE capability register.

**TABLE 2-82: EEE CAPABILITY, ADDRESS 3.20**

| Bit  | Name              | Access | Description                                                                  |
|------|-------------------|--------|------------------------------------------------------------------------------|
| 15:3 | Reserved          | RO     | Reserved                                                                     |
| 2    | 1000BASE-T<br>EEE | RO     | 1: EEE is supported for 1000BASE-T<br>0: EEE is not supported for 1000BASE-T |
| 1    | 100BASE-TX<br>EEE | RO     | 1: EEE is supported for 100BASE-TX<br>0: EEE is not supported for 100BASE-TX |
| 0    | Reserved          | RO     | Reserved                                                                     |

## 2.7.3 EEE WAKE ERROR COUNTER

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and can occur during a refresh or a wakeup as defined by the PHY. This 16-bit counter is reset to all zeros when the EEE wake error counter is read or when the PHY undergoes hardware or software reset.

**TABLE 2-83: EEE WAKE ERROR COUNTER, ADDRESS 3.22**

| Bit  | Name               | Access | Description                         |
|------|--------------------|--------|-------------------------------------|
| 15:0 | Wake error counter | RO     | Count of wake time faults for a PHY |

## 2.7.4 EEE ADVERTISEMENT

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code. The following table shows the bit assignments for the EEE advertisement register.

**TABLE 2-84: EEE ADVERTISEMENT, ADDRESS 7.60**

| Bit  | Name              | Access | Description                                                                                                       | Default |
|------|-------------------|--------|-------------------------------------------------------------------------------------------------------------------|---------|
| 15:3 | Reserved          | RO     | Reserved                                                                                                          | —       |
| 2    | 1000BASE-T<br>EEE | R/W    | 1: Advertise that the 1000BASE-T has EEE capability<br>0: Do not advertise that the 1000BASE-T has EEE capability | 0       |
| 1    | 100BASE-TX<br>EEE | R/W    | 1: Advertise that the 100BASE-TX has EEE capability<br>0: Do not advertise that the 100BASE-TX has EEE capability | 0       |
| 0    | Reserved          | RO     | Reserved                                                                                                          | —       |

### 2.7.5 EEE LINK PARTNER ADVERTISEMENT

All the bits in the EEE LP Advertisement register are read only. A write to the EEE LP advertisement register has no effect. When the AN process has been completed, this register will reflect the contents of the link partner's EEE advertisement register. The following table shows the bit assignments for the EEE advertisement register.

**TABLE 2-85: EEE ADVERTISEMENT, ADDRESS 7.61**

| Bit  | Name              | Access | Description                                                                                                                      |
|------|-------------------|--------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:3 | Reserved          | RO     | Reserved                                                                                                                         |
| 2    | 1000BASE-T<br>EEE | RO     | 1: Link partner is advertising EEE capability for 1000BASE-T<br>0: Link partner is not advertising EEE capability for 1000BASE-T |
| 1    | 100BASE-TX<br>EEE | RO     | 1: Link partner is advertising EEE capability for 100BASE-TX<br>0: Link partner is not advertising EEE capability for 100BASE-TX |
| 0    | Reserved          | RO     | Reserved                                                                                                                         |

The following table shows the bit assignments for the 802.3bf registers. When the link is down, 0 is the value returned. cl45reg1\_1801 would be device address of 1 and register address of 1801.

**TABLE 2-86: 802.3BF REGISTERS**

| Register | Name                    | Function                                                                        |
|----------|-------------------------|---------------------------------------------------------------------------------|
| 1.1801   | cl45reg1_1801_val[15:0] | Tx maximum delay through PHY (PMA/PMD/PCS)                                      |
| 1.1803   | cl45reg1_1803_val[15:0] | Tx minimum delay through PHY (PMA/PMD/PCS)                                      |
| 1.1805   | cl45reg1_1805_val[15:0] | Rx maximum delay through PHY (PMA/PMD/PCS)                                      |
| 1.1807   | cl45reg1_1807_val[15:0] | Rx minimum delay through PHY (PMA/PMD/PCS)                                      |
| 4.1801   | cl45reg4_1801_val[15:0] | Tx maximum delay through xMII (RGMII, SGMII, QSGMII, including FIFO variations) |
| 4.1803   | cl45reg4_1803_val[15:0] | Tx minimum delay through xMII (RGMII, SGMII, QSGMII, including FIFO variations) |
| 4.1805   | cl45reg4_1805_val[15:0] | Rx maximum delay through xMII (RGMII, SGMII, QSGMII, including FIFO variations) |
| 4.1807   | cl45reg4_1807_val[15:0] | Rx minimum delay through xMII (RGMII, SGMII, QSGMII, including FIFO variations) |

## 3.0 ELECTRICAL SPECIFICATIONS

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8552 device.

### 3.1 DC Characteristics

This section contains the DC specifications for the VSC8552 device.

#### 3.1.1 VDD25

The following table shows the DC specifications for the pins referenced to VDD25. The specifications listed in the following table are valid only when  $V_{DD1} = 1.0V$ ,  $V_{DD1A} = 1.0V$ , or  $V_{DD25A} = 2.5V$ .

**TABLE 3-1: VDD25 DC CHARACTERISTICS**

| Parameter                          | Symbol      | Minimum | Maximum | Unit    | Condition                  |
|------------------------------------|-------------|---------|---------|---------|----------------------------|
| Output high voltage                | $V_{OH}$    | 2.0     |         | V       | $I_{OH} = -1.0\text{ mA}$  |
| Output low voltage                 | $V_{OL}$    |         | 0.4     | V       | $I_{OL} = 1.0\text{ mA}$   |
| Input high voltage                 | $V_{IH}$    | 1.85    | 3.3     | V       | —                          |
| Input low voltage                  | $V_{IL}$    | -0.3    | 0.7     | V       | —                          |
| Input leakage current              | $I_{ILEAK}$ | -32     | 32      | $\mu A$ | Internal resistor included |
| Output leakage current             | $I_{OLEAK}$ | -32     | 32      | $\mu A$ | Internal resistor included |
| Output low current drive strength  | $I_{OL}$    | —       | 6       | mA      | —                          |
| Output high current drive strength | $I_{OH}$    | -6      | —       | mA      | —                          |

#### 3.1.2 LED AND GPIO

The following table shows the DC specifications for the LED and GPIO pins.

**TABLE 3-2: LED AND GPIO CHARACTERISTICS**

| Pin  | Symbol   | Minimum | Maximum | Unit |
|------|----------|---------|---------|------|
| LED  | $I_{OH}$ | —       | 24      | mA   |
| LED  | $I_{OL}$ | -24     | —       | mA   |
| GPIO | $I_{OH}$ | —       | 12      | mA   |
| GPIO | $I_{OL}$ | -12     | —       | mA   |

#### 3.1.3 INTERNAL PULL-UP OR PULL-DOWN RESISTORS

Internal pull-up or pull-down resistors are specified in the following table. For more information about signals with internal pull-up or pull-down resistors, see [Section 4.3, Pins by Function](#).

All internal pull-up resistors are connected to their respective I/O supply.

**TABLE 3-3: INTERNAL PULL-UP OR PULL-DOWN RESISTORS**

| Parameter                             | Symbol         | Minimum | Typical | Maximum | Unit      |
|---------------------------------------|----------------|---------|---------|---------|-----------|
| Internal pull-up resistor, GPIO       | $R_{PU\_GPIO}$ | 33      | 53      | 90      | $k\Omega$ |
| Internal pull-up resistor, all others | $R_{PU}$       | 96      | 120     | 144     | $k\Omega$ |
| Internal pull-down resistor           | $R_{PD}$       | 96      | 120     | 144     | $k\Omega$ |

### 3.1.4 REFERENCE CLOCK

The following table shows the DC specifications for a differential reference clock input signal

**TABLE 3-4: REFERENCE CLOCK DC CHARACTERISTICS**

| Parameter                               | Symbol           | Minimum          | Typical | Maximum           | Unit     |
|-----------------------------------------|------------------|------------------|---------|-------------------|----------|
| Input voltage range                     | $V_{IP}, V_{IN}$ | -25              | —       | 1260              | mV       |
| Input differential peak-to-peak voltage | $ V_{ID} $       | 150 <sup>1</sup> | —       | 1200              | mV       |
| Input common-mode voltage               | $V_{ICM}$        | 0                | —       | 1200 <sup>2</sup> | mV       |
| Differential input impedance            | $R_I$            | —                | 100     | —                 | $\Omega$ |

1. To meet jitter specifications, the minimum  $|V_{ID}|$  must be 400 mV. When using a single-ended clock input, the REFCLK\_P low voltage must be less than  $V_{DDA} - 200$  mV, and the high voltage level must be greater than  $V_{DDA} + 200$  mV
2. The maximum common-mode voltage is provided without a differential signal. The common-mode voltage is only limited by the maximum and minimum input voltage range and by the differential amplitude of the input signal.

### 3.1.5 SERDES INTERFACE (SGMII)

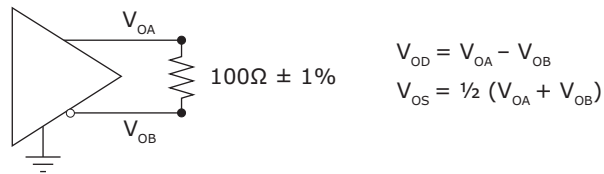
The SerDes output drivers are designed to operate in SGMII/LVDS mode. The SGMII/LVDS mode meets or exceeds the DC requirements of Serial-GMII Specification Revision 1.9 (ENG-46158), unless otherwise noted. The following table lists the DC specifications for the SGMII driver. The values are valid for all configurations, unless stated otherwise.

**TABLE 3-5: SERDES DRIVER DC SPECIFICATIONS**

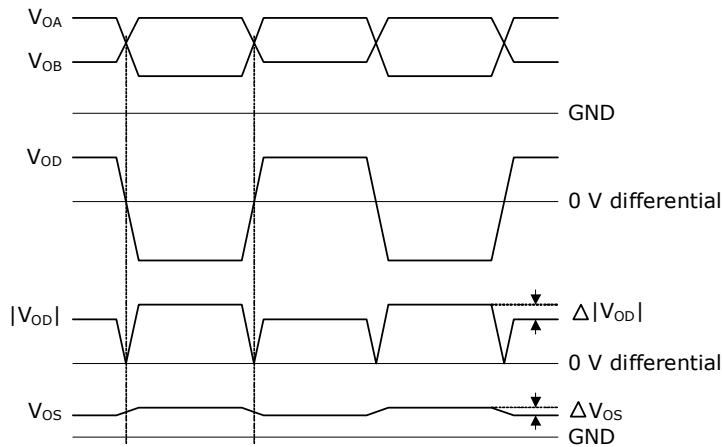
| Parameter                                                | Symbol                       | Minimum | Maximum | Unit     | Condition                                        |
|----------------------------------------------------------|------------------------------|---------|---------|----------|--------------------------------------------------|
| Output high voltage, $V_{OA}$ or $V_{OB}$                | $V_{OH}$                     | —       | 1050    | mV       | $R_L = 100\Omega \pm 1\%$                        |
| Output low voltage, $V_{OA}$ or $V_{OB}$                 | $V_{OL}$                     | 0       | —       | mV       | $R_L = 100\Omega \pm 1\%$                        |
| Output differential peak voltage                         | $ V_{OD} $                   | 350     | 450     | mV       | $V_{DD\_VS} = 1.0V$<br>$R_L = 100\Omega \pm 1\%$ |
| Output differential peak voltage, fiber media 1000BASE-X | $ V_{OD} $                   | 350     | 450     | mV       | $V_{DD\_VS} = 1.0V$<br>$R_L = 100\Omega \pm 1\%$ |
| Output offset voltage <sup>1</sup>                       | $V_{OS}$                     | 420     | 580     | mV       | $V_{DD\_VS} = 1.0V$<br>$R_L = 100\Omega \pm 1\%$ |
| DC output impedance, single-ended, SGMII mode            | $R_O$                        | 40      | 140     | $\Omega$ | $V_C = 1.0V$<br>See <a href="#">Figure 3-3</a>   |
| $R_O$ mismatch between A and B, SGMII mode <sup>2</sup>  | $\Delta R_O$                 | —       | 10      | %        | $V_C = 1.0V$<br>See <a href="#">Figure 3-3</a>   |
| Change in $ V_{OD} $ between 0 and 1, SGMII mode         | $\Delta  V_{OD} $            | —       | 25      | mV       | $R_L = 100\Omega \pm 1\%$                        |
| Change in $V_{OS}$ between 0 and 1, SGMII mode           | $\Delta V_{OS}$              | —       | 25      | mV       | $R_L = 100\Omega \pm 1\%$                        |
| Output current, driver shorted to GND, SGMII mode        | $ I_{OSA} $ ,<br>$ I_{OSB} $ | —       | 40      | mA       | —                                                |
| Output current, drivers shorted together, SGMII mode     | $ I_{OSAB} $                 | —       | 12      | mA       | —                                                |

1. Requires AC-coupling for SGMII compliance.
2. Matching of reflection coefficients. For more information about test methods, see IEEE Std 1596.3-1996.

**FIGURE 3-1: SGMII DC TRANSMIT TEST CIRCUIT**



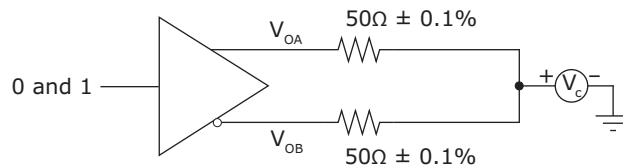
**FIGURE 3-2: SGMII DC DEFINITIONS**



$$\Delta|V_{OD}| = |V_{OAH} - V_{OBL}| - |V_{OBH} - V_{OAL}|$$

$$\Delta V_{OS} = \left| \frac{1}{2}(V_{OAH} + V_{OBL}) - \frac{1}{2}(V_{OAL} + V_{OBH}) \right|$$

**FIGURE 3-3: SGMII DC DRIVER OUTPUT IMPEDANCE TEST CIRCUIT**



The following table lists the DC specifications for the SGMII receivers.

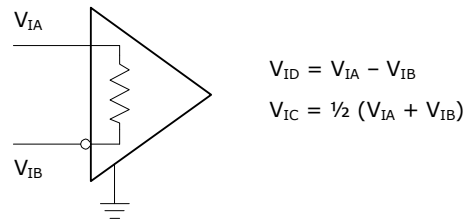
**TABLE 3-6: SERDES RECEIVER DC SPECIFICATIONS**

| Parameter                                 | Symbol     | Minimum | Maximum                  | Unit | Condition                       |
|-------------------------------------------|------------|---------|--------------------------|------|---------------------------------|
| Input voltage range, $V_{IA}$ or $V_{IB}$ | $V_I$      | -25     | 1250                     | mV   | —                               |
| Input differential peak-to-peak voltage   | $ V_{ID} $ | 100     | 1000                     | mV   | —                               |
| Input common-mode voltage <sup>1</sup>    | $V_{ICM}$  | 0       | $V_{DD\_A}$ <sup>2</sup> | mV   | Without any differential signal |
| Receiver differential input impedance     | $R_I$      | 80      | 120                      | Ω    | —                               |
| Input differential hysteresis, SGMII mode | $V_{HYST}$ | 25      | —                        | mV   | —                               |

1. SGMII compliancy requires external AC-coupling. When interfacing with specific Microchip devices, DC-coupling is possible. For more information, contact your local Microchip sales representative.

- The common-mode voltage is only limited by the maximum and minimum input voltage range and the input signal's differential amplitude.

**FIGURE 3-4: SGMII DC INPUT DEFINITIONS**



### 3.1.6 ENHANCED SERDES INTERFACE (QSGMII)

All DC specifications for the enhanced SerDes interface are compliant with QSGMII Specification Revision 1.3 and meet or exceed the requirements in the standard. They are also compliant with OIF-CEI-02.0 requirements where applicable.

The enhanced SerDes interface supports the following operating modes: SGMII, QSGMII, and SFP. The values in the following table apply to the modes specified in the condition column.

The following table shows the DC specifications for the enhanced SerDes driver.

**TABLE 3-7: ENHANCED SERDES DRIVER DC SPECIFICATIONS**

| Parameter                                                         | Symbol                       | Minimum | Maximum | Unit     | Condition                                                         |
|-------------------------------------------------------------------|------------------------------|---------|---------|----------|-------------------------------------------------------------------|
| Output differential peak voltage, SFP and QSGMII modes            | $ V_{ODp} $                  | 250     | 400     | mV       | $V_{DD\_VS} = 1.0V$<br>$R_L = 100\Omega \pm 1\%$<br>maximum drive |
| Output differential peak voltage, SGMII mode <sup>1</sup>         | $ V_{ODp} $                  | 150     | 400     | mV       | $V_{DD\_VS} = 1.0V$<br>$R_L = 100\Omega \pm 1\%$                  |
| DC output impedance, single-ended, SGMII mode                     | $R_O$                        | 40      | 140     | $\Omega$ | $V_C = 1.0V$<br>See <a href="#">Figure 3-3</a>                    |
| $R_O$ mismatch between A and B, SGMII mode <sup>2</sup>           | $\Delta R_O$                 | —       | 10      | %        | $V_C = 1.0V$<br>See <a href="#">Figure 3-3</a>                    |
| Change in $ V_{OD} $ between 0 and 1, SGMII mode                  | $\Delta  V_{OD} $            | —       | 25      | mV       | $R_L = 100\Omega \pm 1\%$                                         |
| Change in $V_{OS}$ between 0 and 1, SGMII mode                    | $\Delta V_{OS}$              | —       | 25      | mV       | $R_L = 100\Omega \pm 1\%$                                         |
| Output current, drivers shorted to ground, SGMII and QSGMII modes | $ I_{OSA} $ ,<br>$ I_{OSB} $ | —       | 40      | mA       | —                                                                 |
| Output current, drivers shorted together, SGMII and QSGMII modes  | $ I_{OSAB} $                 | —       | 12      | mA       | —                                                                 |

- Voltage is adjustable in 64 steps.
- Matching of reflection coefficients. For more information about test methods, see IEEE Std 1596.3-1996.

# VSC8552

The following table lists the DC specifications for the enhanced SerDes receiver.

**TABLE 3-8: ENHANCED SERDES RECEIVER DC SPECIFICATIONS**

| Parameter                                              | Symbol     | Minimum | Typical | Maximum | Unit     |
|--------------------------------------------------------|------------|---------|---------|---------|----------|
| Input voltage range, $V_{IA}$ or $V_{IB}$ <sup>1</sup> | $V_I$      | -0.25   | —       | 1.2     | V        |
| Input differential peak-to-peak voltage                | $ V_{ID} $ | 100     | —       | 1600    | mV       |
| Input common-mode voltage                              | $V_{ICM}$  | 0       | —       | 1200    | mV       |
| Receiver differential input impedance                  | $R_I$      | 80      | 100     | 120     | $\Omega$ |

1. QSGMII DC input sensitivity is less than 400 mV.

## 3.1.7 CURRENT CONSUMPTION

The following tables show the current consumption values for each mode. Add significant margin above the values for sizing power supplies.

**TABLE 3-9: CURRENT CONSUMPTION**

| Mode       | Typical    |           |              |             | Maximum    |           |              |             | Unit | Condition          |
|------------|------------|-----------|--------------|-------------|------------|-----------|--------------|-------------|------|--------------------|
|            | 1V Digital | 1V Analog | 2.5V Digital | 2.5V Analog | 1V Digital | 1V Analog | 2.5V Digital | 2.5V Analog |      |                    |
| Reset      | 52         | 55        | 9            | 1           | 460        | 110       | 13           | 5           | mA   | —                  |
| Power down | 110        | 170       | 10           | 20          | 525        | 220       | 15           | 25          | mA   | —                  |
| 1000BASE-T | 250        | 180       | 15           | 250         | 755        | 245       | 15           | 265         | mA   | 2-port SGMII       |
| 100BASE-TX | 155        | 175       | 15           | 170         | 645        | 235       | 15           | 190         | mA   | 2-port SGMII       |
| 10BASE-T   | 130        | 170       | 15           | 145         | 615        | 230       | 15           | 150         | mA   | 2-port SGMII       |
| 10BASE-Te  | 130        | 170       | 15           | 135         | 615        | 230       | 15           | 140         | mA   | 2-port SGMII       |
| 1000BASE-X | 145        | 205       | 15           | 35          | 685        | 265       | 15           | 40          | mA   | 2-port SGMII       |
| 100BASE-FX | 135        | 200       | 15           | 35          | 645        | 260       | 15           | 40          | mA   | 2-port SGMII       |
| 1000BASE-T | 235        | 100       | 55           | 250         | 740        | 160       | 65           | 265         | mA   | 2-port RGMII       |
| 100BASE-TX | 140        | 95        | 20           | 170         | 630        | 150       | 20           | 190         | mA   | 2-port RGMII       |
| 10BASE-T   | 115        | 90        | 15           | 145         | 600        | 145       | 15           | 150         | mA   | 2-port RGMII       |
| 10BASE-Te  | 115        | 90        | 15           | 135         | 600        | 145       | 15           | 140         | mA   | 2-port RGMII       |
| 1000BASE-X | 130        | 120       | 55           | 35          | 670        | 180       | 65           | 40          | mA   | 2-port RGMII       |
| 100BASE-FX | 120        | 115       | 20           | 35          | 630        | 175       | 20           | 40          | mA   | 2-port RGMII       |
| 1000BASE-T | 250        | 145       | 10           | 250         | 755        | 210       | 15           | 265         | mA   | 2-port half QSGMII |
| 100BASE-TX | 155        | 140       | 10           | 170         | 645        | 200       | 15           | 190         | mA   | 2-port half QSGMII |
| 10BASE-T   | 130        | 135       | 10           | 145         | 615        | 195       | 15           | 150         | mA   | 2-port half QSGMII |
| 10BASE-Te  | 130        | 135       | 10           | 135         | 615        | 195       | 15           | 140         | mA   | 2-port half QSGMII |
| 1000BASE-X | 145        | 170       | 10           | 35          | 685        | 230       | 15           | 40          | mA   | 2-port half QSGMII |
| 100BASE-FX | 135        | 165       | 10           | 35          | 645        | 225       | 15           | 40          | mA   | 2-port half QSGMII |

## 3.1.8 THERMAL DIODE

The VSC8552 device includes an on-die diode and internal circuitry for monitoring die temperature (junction temperature). The operation and accuracy of the diode is not guaranteed and should only be used as a reference. Care should be taken to find compatible grounded cathode temperature monitoring device.

A thermal sensor, located on the board or in a stand-alone measurement kit, can monitor and display the die temperature of the switch for thermal management or instrumentation purposes.

Temperature measurement using a thermal diode is very sensitive to noise.

The following table provides the diode parameter and interface specifications. Note that the ThermDC pin is connected to VSS internally in the device.

**TABLE 3-10: THERMAL DIODE PARAMETERS**

| Parameter             | Symbol | Typical | Maximum | Unit |
|-----------------------|--------|---------|---------|------|
| Forward bias current  | IFW    | —       | 1       | mA   |
| Diode ideality factor | n      | 1.008   | —       | —    |

**Note:** Microchip does not support or recommend operation of the thermal diode under reverse bias.

The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

$$I_{FW} = I_S \times \left( e^{V_d \times \frac{q}{nkT}} - 1 \right)$$

where,  $I_S$  = saturation current,  $q$  = electronic charge,  $V_d$  = voltage across the diode,  $k$  = Boltzmann Constant, and  $T$  = absolute temperature (Kelvin).

## 3.2 AC Characteristics

This section provides the AC specifications for the VSC8552 device.

### 3.2.1 REFERENCE CLOCK

The following table shows the AC specifications for a 125 MHz differential reference clock source. Performance is guaranteed for 125 MHz differential clocks only; however, 125 MHz single-ended clocks are also supported for QSGMII interfaces.

25 MHz clock implementations are available but are limited to SGMII interfaces. For more information, contact your Microchip representative.

**TABLE 3-11: REFERENCE CLOCK AC CHARACTERISTICS FOR QSGMII 125 MHZ DIFFERENTIAL CLOCK**

| Parameter                                                                              | Symbol     | Minimum | Typical | Maximum | Unit | Condition                                                   |
|----------------------------------------------------------------------------------------|------------|---------|---------|---------|------|-------------------------------------------------------------|
| Reference clock frequency, REFCLK_SEL2 = 1                                             | $f$        |         | 125.00  |         | MHz  | ±100 ppm                                                    |
| Duty cycle                                                                             | DC         | 40      | 50      | 60      | %    | —                                                           |
| Rise time and fall time                                                                | $t_r, t_f$ | —       | —       | 1.5     | ns   | 20% to 80% threshold                                        |
| RefClk input RMS jitter requirement, bandwidth between 12 kHz and 500 kHz <sup>1</sup> | —          | —       | —       | 20      | ps   | To meet jitter generation of 1G output data per IEEE 802.3z |
| RefClk input RMS jitter requirement, bandwidth between 500 kHz and 15 MHz <sup>1</sup> | —          | —       | —       | 4       | ps   | To meet jitter generation of 1G output data per IEEE 802.3z |
| RefClk input RMS jitter requirement, bandwidth between 15 MHz and 40 MHz <sup>1</sup>  | —          | —       | —       | 20      | ps   | To meet jitter generation of 1G output data per IEEE 802.3z |

**TABLE 3-11: REFERENCE CLOCK AC CHARACTERISTICS FOR QSGMII 125 MHz DIFFERENTIAL CLOCK (CONTINUED)**

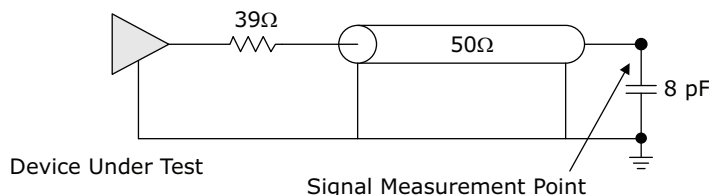
| Parameter                                                                             | Symbol | Minimum                             | Typical | Maximum                             | Unit | Condition                                                   |
|---------------------------------------------------------------------------------------|--------|-------------------------------------|---------|-------------------------------------|------|-------------------------------------------------------------|
| RefClk input RMS jitter requirement, bandwidth between 40 MHz and 80 MHz <sup>1</sup> | —      | —                                   | —       | 100                                 | ps   | To meet jitter generation of 1G output data per IEEE 802.3z |
| Jitter gain from RefClk to SerDes output, bandwidth between 0 MHz and 0.1 MHz         | —      | —                                   | —       | 0.3                                 | dB   | —                                                           |
| Jitter gain from RefClk to SerDes output, bandwidth between 0.1 MHz and 7 MHz         | —      | —                                   | 1       | 3                                   | dB   | —                                                           |
| Jitter gain from RefClk to SerDes output, bandwidth above 7 MHz                       | —      | $1-20 \times \log(f/7 \text{ MHz})$ | —       | $3-20 \times \log(f/7 \text{ MHz})$ | dB   | —                                                           |

1. Maximum RMS jitter allowed at the RefClk input for the given bandwidth.

## 3.2.2 RECOVERED CLOCK

This section provides the AC characteristics for the recovered clock output signals. The following illustration shows the test circuit for the recovered clock output signals.

**FIGURE 3-5: TEST CIRCUIT FOR RECOVERED CLOCK OUTPUT SIGNALS**



The following table shows the AC specifications for the RCVRDCLK1 and RCVRDCLK2 outputs.

**TABLE 3-12: RECOVERED CLOCK AC CHARACTERISTICS**

| Parameter                  | Symbol     | Minimum | Typical | Maximum | Unit | Condition |
|----------------------------|------------|---------|---------|---------|------|-----------|
| Recovered clock frequency  | $f$        | —       | 125.00  | —       | MHz  | —         |
| Recovered clock frequency  | $f$        | —       | 31.25   | —       | MHz  | —         |
| Recovered clock frequency  | $f$        | —       | 25.00   | —       | MHz  | —         |
| Recovered clock cycle time | $t_{RCYC}$ | —       | 8.0     | —       | ns   | —         |
| Recovered clock cycle time | $t_{RCYC}$ | —       | 32.0    | —       | ns   | —         |
| Recovered clock cycle time | $t_{RCYC}$ | —       | 40.0    | —       | ns   | —         |

**TABLE 3-12: RECOVERED CLOCK AC CHARACTERISTICS (CONTINUED)**

| Parameter                                                           | Symbol                    | Minimum | Typical | Maximum | Unit | Condition   |
|---------------------------------------------------------------------|---------------------------|---------|---------|---------|------|-------------|
| Frequency stability                                                 | $f_{\text{STABILITY}}$    | —       |         | 50      | ppm  | —           |
| Duty cycle, master mode                                             | DC                        | 40      | 50      | 60      | %    | —           |
| Clock rise time and fall time                                       | $t_R, t_F$                | —       | 600     | —       | ps   | 20% to 80%  |
| Peak-to-peak jitter, copper media interface (1000BASE-T slave mode) | $JPP_{\text{CLK\_Cu}}$    | —       | —       | 400     | ps   | 10K samples |
| Peak-to-peak jitter, fiber media interface, 100BASE-FX              | $JPP_{\text{CLK\_FIF}_X}$ | —       | —       | 1.2     | ns   | 10K samples |
| Peak-to-peak jitter, fiber media interface, 1000BASE-X              | $JPP_{\text{CLK\_FIX}}$   | —       | —       | 250     | ps   | 10K samples |

### 3.2.3 SERDES OUTPUTS

The values listed in the following table are valid for all configurations, unless otherwise noted.

**TABLE 3-13: SERDES OUTPUTS AC SPECIFICATIONS**

| Parameter                                             | Symbol            | Minimum                                  | Maximum  | Unit | Condition                                       |
|-------------------------------------------------------|-------------------|------------------------------------------|----------|------|-------------------------------------------------|
| $V_{OD}$ ringing compared to $V_S$ , RGMII/SGMII mode | $V_{\text{RING}}$ | —                                        | $\pm 10$ | %    | $RL = 100\Omega \pm 1\%$                        |
| $V_{OD}$ rise time and fall time, RGMII/SGMII mode    | $t_R, t_F$        | 100                                      | 200      | ps   | 20% to 80% of $V_S$<br>$RL = 100\Omega \pm 1\%$ |
| Differential peak-to-peak output voltage              | $V_{OD}$          | —                                        | 30       | mV   | Tx disabled                                     |
| Differential output return loss, 50 MHz to 625 MHz    | $R_{LO\_DIFF}$    | $\geq 10$                                | —        | dB   | $RL = 100\Omega \pm 1\%$                        |
| Differential output return loss, 625 MHz to 1250 MHz  | $R_{LO\_DIFF}$    | $10 - 10 \times \log(f/625 \text{ MHz})$ | —        | dB   | $RL = 100\Omega \pm 1\%$                        |
| Common-mode return loss, 50 MHz to 625 MHz            | $RL_{OCM}$        | 6                                        | —        | dB   | —                                               |
| Interpair skew, RGMII/SGMII mode                      | $t_{\text{SKEW}}$ | —                                        | 20       | ps   | —                                               |

### 3.2.4 SERDES DRIVER JITTER

The following table lists the jitter characteristics for the SerDes output driver.

**TABLE 3-14: SERDES DRIVER JITTER CHARACTERISTICS**

| Parameter            | Symbol | Maximum | Unit | Condition                             |
|----------------------|--------|---------|------|---------------------------------------|
| Total jitter         | $TJ_O$ | 192     | ps   | Measured according to IEEE 802.3.38.5 |
| Deterministic jitter | $DJ_O$ | 80      | ps   | Measured according to IEEE 802.3.38.5 |

## 3.2.5 SERDES INPUTS

The following table lists the AC specifications for the SerDes inputs.

**TABLE 3-15: SERDES INPUT AC SPECIFICATIONS**

| Parameter                                           | Maximum                                  | Unit | Condition                |
|-----------------------------------------------------|------------------------------------------|------|--------------------------|
| Differential input return loss, 50 MHz to 625 MHz   | $\geq 10$                                | dB   | RL = $100\Omega \pm 1\%$ |
| Differential input return loss, 625 MHz to 1250 MHz | $10 - 10 \times \log(f/625 \text{ MHz})$ | dB   | RL = $100\Omega \pm 1\%$ |

## 3.2.6 SERDES RECEIVER JITTER TOLERANCE

The following table lists jitter tolerances for the SerDes receiver.

**TABLE 3-16: SERDES RECEIVER JITTER TOLERANCE**

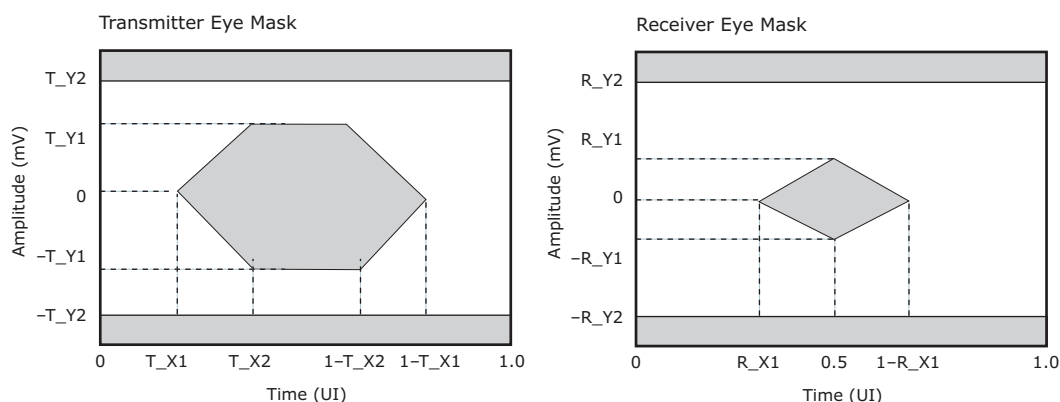
| Parameter                                                      | Symbol           | Minimum | Unit | Condition                                 |
|----------------------------------------------------------------|------------------|---------|------|-------------------------------------------|
| Total jitter tolerance, greater than 637 kHz, SFP mode         | TJT <sub>I</sub> | 600     | ps   | Measured according to IEEE 802.3 38.6.8   |
| Deterministic jitter tolerance, greater than 637 kHz, SFP mode | DJT <sub>I</sub> | 370     | ps   | Measured according to IEEE 802.3 38.6.8   |
| Cycle distortion jitter tolerance, 100BASE-FX mode             | JT <sub>CD</sub> | 1.4     | ns   | Measured according to ISO/IEC 9314-3:1990 |
| Data-dependent jitter tolerance, 100BASE-FX mode               | DDJ              | 2.2     | ns   | Measured according to ISO/IEC 9314-3:1990 |
| Random peak-to-peak jitter tolerance, 100BASE-FX mode          | RJT              | 2.27    | ns   | Measured according to ISO/IEC 9314-3:1990 |

## 3.2.7 ENHANCED SERDES INTERFACE

All AC specifications for the enhanced SerDes interface are compliant with QSGMII Specification Revision 1.3 and meet or exceed the requirements in the standard. They are also compliant with the OIF-CEI-02.0 requirements where applicable.

The enhanced SerDes interface supports the following modes of operation: SGMII, QSGMII, and SFP. The values in the tables in the following sections apply to the QSGMII modes listed in the condition column and are based on the test circuit shown in Figure 3-1. The transmit and receive eye specifications relate to the eye diagrams shown in the following illustration, with the compliance load as defined in the test circuit.

**FIGURE 3-6: QSGMII TRANSIENT PARAMETERS**



## 3.2.7.1 Enhanced SerDes Outputs

The following table provides the AC specifications for the enhanced SerDes outputs in SGMII mode.

**TABLE 3-17: ENHANCED SERDES OUTPUTS AC SPECIFICATIONS, SGMII MODE**

| Parameter                                            | Symbol           | Minimum                                  | Maximum  | Unit | Condition                                       |
|------------------------------------------------------|------------------|------------------------------------------|----------|------|-------------------------------------------------|
| Unit interval, 1.25G mode                            | UI               | —                                        | —        | —    | 800 ps                                          |
| $V_{OD}$ ringing compared to $V_S$                   | $V_{RING}$       | —                                        | $\pm 10$ | %    | $R_L = 100\Omega \pm 1\%$                       |
| $V_{OD}$ rise time and fall time                     | $t_R, t_F$       | 100                                      | 200      | ps   | 20% to 80% of $V_S$<br>$R_L = 10\Omega \pm 1\%$ |
| Differential peak-to-peak output voltage             | $V_{OD}$         | —                                        | 30       | mV   | Tx disabled                                     |
| Differential output return loss, 50 MHz to 625 MHz   | $RL_{O\_DIF\_F}$ | $\geq 10$                                | —        | dB   | $R_L = 100\Omega \pm 1\%$                       |
| Differential output return loss, 625 MHz to 1250 MHz | $RL_{O\_DIF\_F}$ | $10 - 10 \times \log(f/625 \text{ MHz})$ | —        | dB   | $R_L = 100\Omega \pm 1\%$                       |
| Common-mode return loss, 50 MHz to 625 MHz           | $RL_{OCM}$       | 6                                        | —        | dB   | —                                               |
| Intrapair skew                                       | $t_{SKEW}$       | —                                        | 20       | ps   | —                                               |

The following table provides the AC specifications for the enhanced SerDes outputs in QSGMII mode.

**TABLE 3-18: ENHANCED SERDES OUTPUTS AC SPECIFICATIONS, QSGMII MODE**

| Parameter                                           | Symbol           | Minimum                                       | Maximum | Unit | Condition                                        |
|-----------------------------------------------------|------------------|-----------------------------------------------|---------|------|--------------------------------------------------|
| Unit interval, 5G                                   | UI               | —                                             | —       | —    | 200 ps                                           |
| $V_{OD}$ rise time and fall time                    | $t_R, t_F$       | 30                                            | 96      | ps   | 20% to 80% of $V_S$<br>$R_L = 100\Omega \pm 1\%$ |
| Differential peak-to-peak output voltage            | $V_{OD}$         | —                                             | 30      | mV   | Tx disabled                                      |
| Differential output return loss, 100 MHz to 2.5 GHz | $RL_{O\_DIF\_F}$ | 8                                             | —       | dB   | $R_L = 100\Omega \pm 1\%$                        |
| Differential output return loss, 2.5 GHz to 5 GHz   | $RL_{O\_DIF\_F}$ | $8 \text{ dB} - 16.6 \log(f/2.5 \text{ GHz})$ | —       | dB   | $R_L = 100\Omega \pm 1\%$                        |
| Eye mask X1                                         | $T_{X1}$         | —                                             | 0.15    | UI   | —                                                |
| Eye mask X2                                         | $T_{X2}$         | —                                             | 0.4     | UI   | —                                                |
| Eye mask Y1                                         | $T_{Y1}$         | 200                                           | —       | mV   | —                                                |
| Eye mask Y2                                         | $T_{Y2}$         | —                                             | 450     | mV   | —                                                |

## 3.2.7.2 Enhanced SerDes Driver Jitter Characteristics

The following table lists the jitter characteristics for the enhanced SerDes driver in QSGMII mode. For information about jitter characteristics for the enhanced SerDes driver in SGMII mode, see [Table 3-14](#).

**TABLE 3-19: ENHANCED SERDES DRIVER JITTER CHARACTERISTICS, QSGMII MODE**

| Parameter                   | Symbol          | Maximum | Unit | Condition                              |
|-----------------------------|-----------------|---------|------|----------------------------------------|
| Total output jitter         | TJ <sub>O</sub> | 60      | ps   | Measured according to IEEE 802.3.38.5. |
| Deterministic output jitter | DJ <sub>O</sub> | 10      | ps   | Measured according to IEEE 802.3.38.5. |

## 3.2.7.3 Enhanced SerDes Inputs

The following table lists the AC specifications for the enhanced SerDes inputs in SGMII mode.

**TABLE 3-20: ENHANCED SERDES INPUT AC SPECIFICATIONS, SGMII MODE**

| Parameter                                         | Symbol               | Minimum | Unit | Condition                 |
|---------------------------------------------------|----------------------|---------|------|---------------------------|
| Unit interval, 1.25G                              | UI                   | —       | ps   | 800 ps                    |
| Differential input return loss, 50 MHz to 625 MHz | RL <sub>I_DIFF</sub> | 10      | dB   | R <sub>L</sub> = 100Ω ±1% |
| Common-mode input return loss, 50 MHz to 625 MHz  | RL <sub>ICM</sub>    | 6       | dB   | —                         |

The following table lists the AC specifications for the enhanced SerDes inputs in QSGMII mode.

**TABLE 3-21: ENHANCED SERDES INPUTS AC SPECIFICATIONS, QSGMII MODE**

| Parameter                                          | Symbol               | Minimum                     | Maximum | Unit | Condition                 |
|----------------------------------------------------|----------------------|-----------------------------|---------|------|---------------------------|
| Unit interval, 5G                                  | UI                   | —                           | —       | —    | 200 ps                    |
| Differential input return loss, 100 MHz to 2.5 GHz | RL <sub>I_DIFF</sub> | 8                           | —       | dB   | R <sub>L</sub> = 100Ω ±1% |
| Differential input return loss, 2.5 GHz to 5 GHz   | RL <sub>I_DIFF</sub> | 8 dB – 16.6 log (f/2.5 GHz) | —       | dB   | R <sub>L</sub> = 100Ω ±1% |
| Common-mode input return loss, 100 MHz to 2.5 GHz  | RL <sub>ICM</sub>    | 6                           | —       | dB   | —                         |
| Eye mask X1                                        | R_X1                 | —                           | 0.3     | UI   | —                         |
| Eye mask Y1                                        | R_Y1                 | —                           | 50      | mV   | —                         |
| Eye mask Y2                                        | R_Y2                 | —                           | 450     | mV   | —                         |

### 3.2.7.4 Enhanced SerDes Receiver Jitter Tolerance

The following table lists the jitter tolerance for the enhanced SerDes receiver in QSGMII mode. For information about jitter tolerance for the enhanced SerDes receiver in SGMII mode, see [Table 3-16](#).

**TABLE 3-22: ENHANCED SERDES RECEIVER JITTER TOLERANCE, QSGMII MODE**

| Parameter                                    | Symbol            | Maximum | Unit | Condition                                                            |
|----------------------------------------------|-------------------|---------|------|----------------------------------------------------------------------|
| Bounded high-probability jitter <sup>1</sup> | BHPJ              | 90      | ps   | 92 ps peak-to-peak random jitter and 38 ps sinusoidal jitter (SJHF). |
| Sinusoidal jitter, maximum                   | SJ <sub>MAX</sub> | 1000    | ps   | —                                                                    |
| Sinusoidal jitter, high frequency            | SJ <sub>HF</sub>  | 10      | ps   | —                                                                    |
| Total jitter tolerance                       | TJT <sub>I</sub>  | 120     | ps   | 92 ps peak-to-peak random jitter and 38 ps sinusoidal jitter (SJHF). |

1. This is the sum of uncorrelated bounded high probability jitter (0.15 UI), and correlated bounded high probability jitter (0.30 UI). Uncorrelated bounded high probability jitter is distribution where the value of the jitter shows no correlation to any signal level being transmitted, formally defined as deterministic jitter (DJ). Correlated bounded high probability jitter is jitter distribution where the value of the jitter shows a strong correlation to the signal level being transmitted.

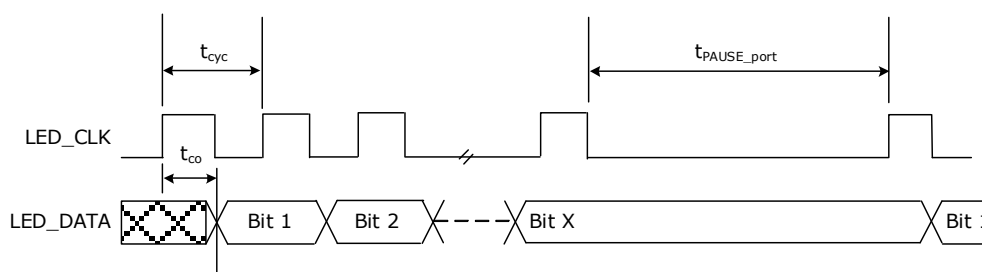
### 3.2.8 BASIC SERIAL LEDS

This section contains the AC specifications for the basic serial LEDs.

**TABLE 3-23: BASIC SERIAL LEDS AC CHARACTERISTICS**

| Parameter                        | Symbol                  | Typical   | Unit |
|----------------------------------|-------------------------|-----------|------|
| LED_CLK cycle time               | t <sub>CYC</sub>        | 1024      | ns   |
| Pause between LED port sequences | t <sub>PAUSE_port</sub> | 3072      | ns   |
| Pause between LED bit sequences  | t <sub>PAUSE_bit</sub>  | 25.541632 | ms   |
| LED_CLK to LED_DATA              | t <sub>CO</sub>         | 1         | ns   |

**FIGURE 3-7: BASIC SERIAL LED TIMING**



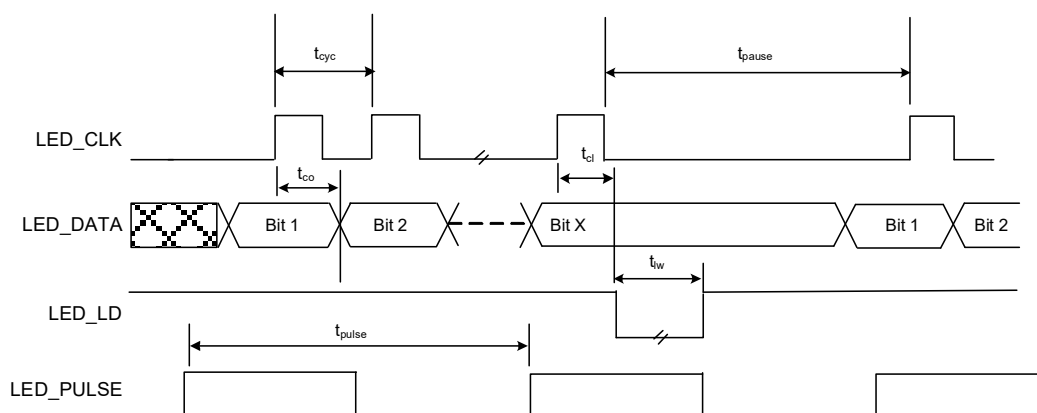
## 3.2.9 ENHANCED SERIAL LEDS

This section contains the AC specifications for the enhanced serial LEDs. The duty cycle of the LED\_PULSE signal is programmable and can be varied between 0.5% and 99.5%.

**TABLE 3-24: ENHANCED SERIAL LEDS AC CHARACTERISTICS**

| Parameter                            | Symbol      | Minimum | Typical | Maximum | Unit    |
|--------------------------------------|-------------|---------|---------|---------|---------|
| LED_CLK cycle time                   | $t_{CYC}$   | —       | 256     | —       | ns      |
| Pause between LED_DATA bit sequences | $t_{PAUSE}$ | 0.396   | —       | 24.996  | ms      |
| LED_CLK to LED_DATA                  | $t_{CO}$    | —       | 127     | —       | ns      |
| LED_CLK to LED_LD                    | $t_{CL}$    | —       | 256     | —       | ns      |
| LED_LD pulse width                   | $t_{LW}$    | —       | 128     | —       | ns      |
| LED_PULSE cycle time                 | $t_{PULSE}$ | 199     | —       | 201     | $\mu$ s |

**FIGURE 3-8: ENHANCED SERIAL LED TIMING**



## 3.2.10 JTAG INTERFACE

This section provides the AC specifications for the JTAG interface. The specifications meet or exceed the requirements of IEEE 1149.1-2001. The JTAG receive signal requirements are requested at the pin of the device. The JTAG\_TRST signal is asynchronous to the clock, and does not have a setup or hold time requirement.

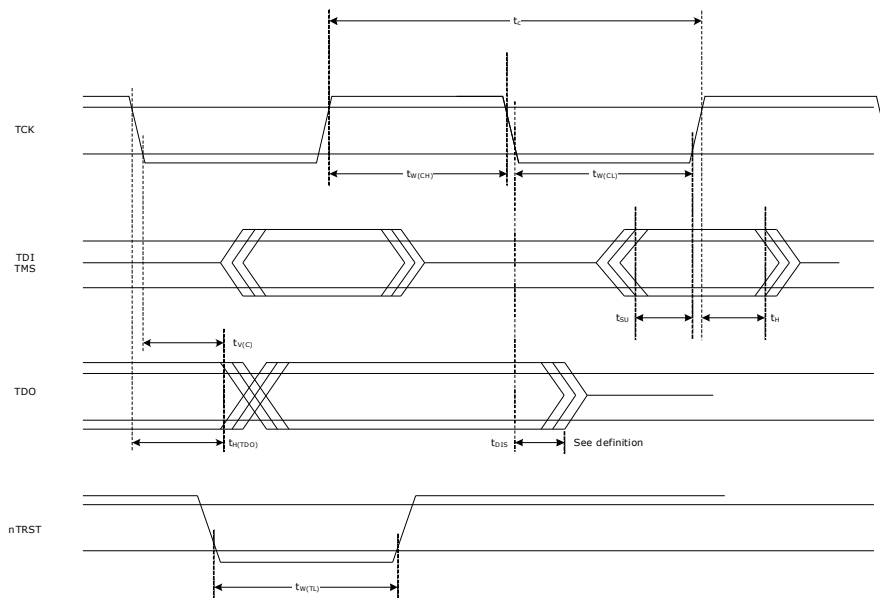
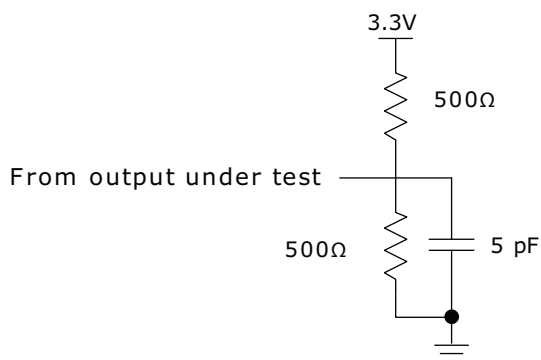
**TABLE 3-25: JTAG INTERFACE AC SPECIFICATIONS**

| Parameter                   | Symbol      | Minimum | Maximum | Unit | Condition     |
|-----------------------------|-------------|---------|---------|------|---------------|
| TCK frequency               | $f$         | —       | 10      | MHz  | —             |
| TCK cycle time              | $t_C$       | 100     | —       | ns   | —             |
| TCK high time               | $t_{W(CH)}$ | 40      | —       | ns   | —             |
| TCK low time                | $t_{W(CL)}$ | 40      | —       | ns   | —             |
| Setup time to TCK rising    | $t_{SU}$    | 10      | —       | ns   | —             |
| Hold time from TCK rising   | $t_H$       | 10      | —       | ns   | —             |
| TDO valid after TCK falling | $t_{V(C)}$  | —       | 28      | ns   | $C_L = 10$ pF |

**TABLE 3-25: JTAG INTERFACE AC SPECIFICATIONS (CONTINUED)**

| Parameter                      | Symbol       | Minimum | Maximum | Unit | Condition        |
|--------------------------------|--------------|---------|---------|------|------------------|
| TDO hold time from TCK falling | $t_{H(TDO)}$ | 0       | —       | ns   | $C_L = 0$ pF     |
| TDO disable time <sup>1</sup>  | $t_{DIS}$    | —       | 30      | ns   | See Figure 3-10. |
| TRST time low                  | $t_{W(TL)}$  | 30      | —       | ns   | —                |

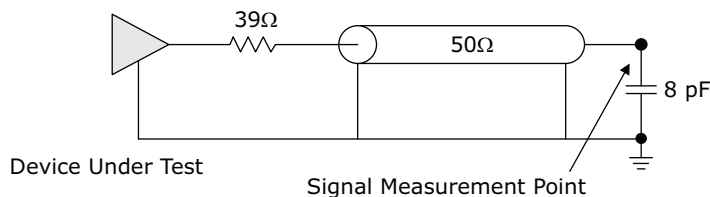
1. The pin begins to float when a 300 mV change from the actual  $V_{OH}/V_{OL}$  level occurs.

**FIGURE 3-9: JTAG INTERFACE TIMING DIAGRAM****FIGURE 3-10: TEST CIRCUIT FOR TDO DISABLE TIME**

### 3.2.11 RGMII, UNCOMPENSATED

The following illustration shows the test circuit for the RGMII output signals.

**FIGURE 3-11: TEST CIRCUIT FOR RGMII OUTPUT SIGNALS**

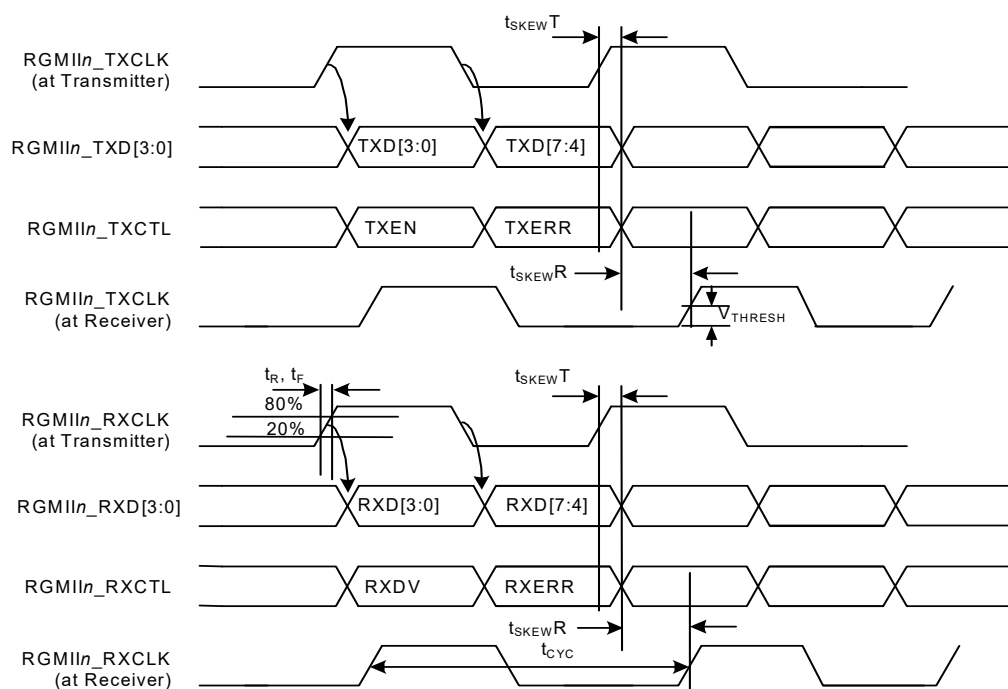


The following table lists the characteristics when using the device in RGMII uncompensated mode. For more information about the RGMII uncompensated timing, see [Figure 3-12](#).

**TABLE 3-26: AC CHARACTERISTICS FOR RGMII UNCOMPENSATED**

| Parameter                                               | Symbol           | Minimum | Typical          | Maximum | Unit | Condition                                                          |
|---------------------------------------------------------|------------------|---------|------------------|---------|------|--------------------------------------------------------------------|
| Clock frequency                                         | —                | —       | 125<br>25<br>2.5 | —       | MHz  | 1000BASE-T operation<br>100BASE-TX operation<br>10BASE-T operation |
| 1000BASE-T duty cycle                                   | $t_{DUTY1000}$   | 40      | 50               | 60      | %    | —                                                                  |
| 10/100BASE-T duty cycle                                 | $t_{DUTY10/100}$ | 35      | 38               | 65      | %    | 10BASE-T                                                           |
| 10/100BASE-T duty cycle                                 | $t_{DUTY10/100}$ | 40      | 50               | 60      | %    | 100BASE-TX                                                         |
| Data to clock output skew <sup>1</sup> (at transmitter) | $t_{SKEWT}$      | –500    | 0                | 500     | ps   | —                                                                  |
| Data to clock output skew <sup>1</sup> (at receiver)    | $t_{SKEWR}$      | 1.0     | 1.8              | 2.6     | ns   | —                                                                  |
| TX_CLK switching threshold                              | $V_{THRESH}$     | —       | 1.25             | —       | V    | $V_{DD25} = 2.5$                                                   |
| Clock/data output rise and fall times                   | $t_R$ and $t_F$  | —       | —                | 750     | ps   | 20% to 80%, 1000BASE-T                                             |
| Clock/data output rise and fall times                   | $t_R$ and $t_F$  | —       | —                | 1000    | ps   | 20% to 80%, 10BASE-T/<br>100BASE-TX                                |

- When operating in uncompensated mode, the PC board design requires a clock to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

**FIGURE 3-12: RGMII UNCOMPENSATED TIMING**

$n = 0$  or  $1$ , corresponding to PHY  $n$ .

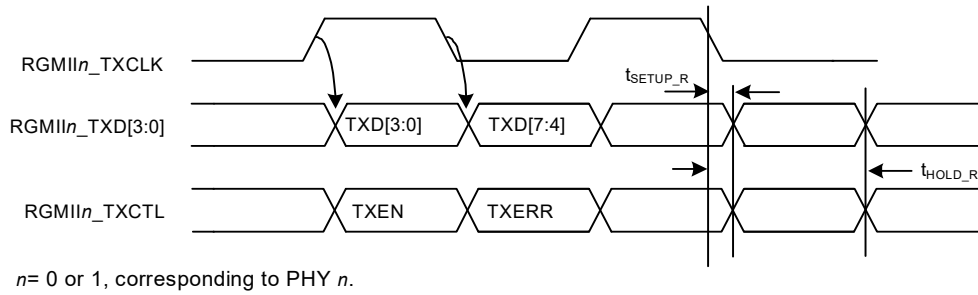
### 3.2.12 RGMII, COMPENSATED

The following table lists the characteristics when using the device in RGMII compensated mode.

**TABLE 3-27: PHY INPUT (RGMII<sub>n</sub>\_TXCLK DELAY WHEN REGISTER 18E2.[6:4]=011'B)**

| Parameter                                  | Symbol                | Minimum | Typical | Maximum | Unit |
|--------------------------------------------|-----------------------|---------|---------|---------|------|
| Data to clock setup (TX_CLK delay = 011'b) | $t_{\text{SETUP\_R}}$ | -1.0    | —       | —       | ns   |
| Clock to data hold (TX_CLK delay = 011'b)  | $t_{\text{HOLD\_R}}$  | 2.8     | —       | —       | ns   |

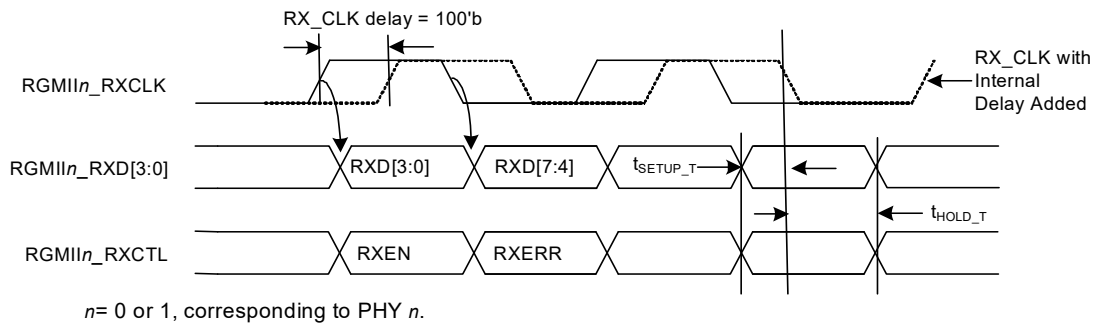
**FIGURE 3-13: COMPENSATED INPUT RGMII TIMING**



**TABLE 3-28: PHY OUTPUT (RGMII\_n\_RXCLK DELAY WHEN REGISTER 18E2.[3:1]=100'B)**

| Parameter                                  | Symbol               | Minimum | Typical | Maximum | Unit |
|--------------------------------------------|----------------------|---------|---------|---------|------|
| Data to clock setup (RX_CLK delay = 100'b) | $t_{\text{SETUP}_T}$ | 1.3     | 2.0     | —       | ns   |
| Clock to data hold (RX_CLK delay = 100'b)  | $t_{\text{HOLD}_T}$  | 1.4     | 2.0     | —       | ns   |

**FIGURE 3-14: COMPENSATED OUTPUT RGMII TIMING**



### 3.2.13 SERIAL MANAGEMENT INTERFACE

This section contains the AC specifications for the serial management interface (SMI).

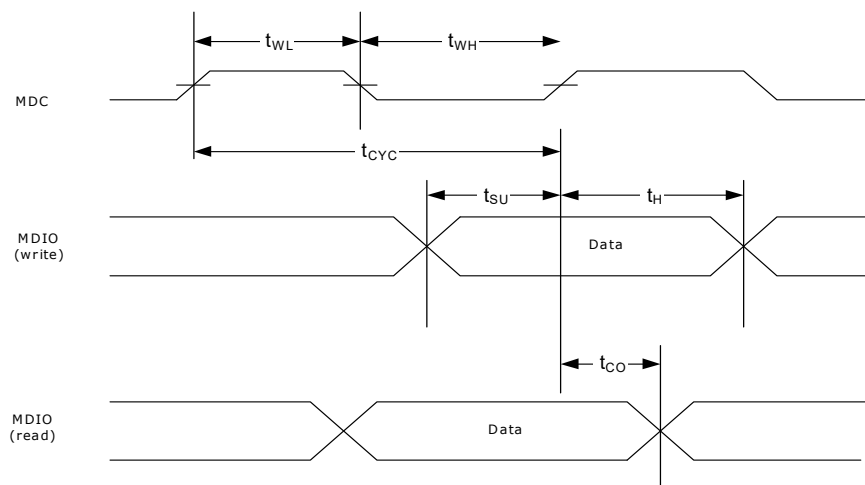
**TABLE 3-29: SERIAL MANAGEMENT INTERFACE AC CHARACTERISTICS**

| Parameter                  | Symbol           | Minimum | Typical | Maximum | Unit | Condition |
|----------------------------|------------------|---------|---------|---------|------|-----------|
| MDC frequency <sup>1</sup> | $f_{\text{CLK}}$ | —       | 2.5     | 12.5    | MHz  |           |
| MDC cycle time             | $t_{\text{CYC}}$ | 80      | 400     | —       | ns   | —         |
| MDC time high              | $t_{\text{WH}}$  | 20      | 50      | —       | ns   | —         |
| MDC time low               | $t_{\text{WL}}$  | 20      | 50      | —       | ns   | —         |
| Setup to MDC rising        | $t_{\text{SU}}$  | 10      | —       | —       | ns   | —         |
| Hold from MDC rising       | $t_{\text{H}}$   | 10      | —       | —       | ns   | —         |

**TABLE 3-29: SERIAL MANAGEMENT INTERFACE AC CHARACTERISTICS (CONTINUED)**

| Parameter         | Symbol   | Minimum | Typical | Maximum                            | Unit | Condition                                                                    |
|-------------------|----------|---------|---------|------------------------------------|------|------------------------------------------------------------------------------|
| MDC rise time     | $t_R$    | —       | —       | 100<br>$t_{CYC} \times 10\%^{(1)}$ | ns   | MDC = 0: 1 MHz<br>MDC = 1:<br>MHz – $f_{CLK}$ maximum                        |
| MDC fall time     | $t_F$    | —       | —       | 100<br>$t_{CYC} \times 10\%^{(1)}$ | —    | —                                                                            |
| MDC to MDIO valid | $t_{CO}$ | —       | 10      | 300                                | ns   | Time-dependant on the value of the external pull-up resistor on the MDIO pin |

1. For  $f_{CLK}$  above 1 MHz, the minimum rise time and fall time is in relation to the frequency of the MDC clock period. For example, if  $f_{CLK}$  is 2 MHz, the minimum clock rise time and fall time is 50 ns.

**FIGURE 3-15: SERIAL MANAGEMENT INTERFACE TIMING**

### 3.2.14 RESET TIMING

This section contains the AC specifications that apply to device reset functionality. The signal applied to the NRESET input must comply with the specifications listed in the following table.

**TABLE 3-30: RESET TIMING SPECIFICATIONS**

| Parameter                                                          | Symbol      | Minimum | Maximum | Unit |
|--------------------------------------------------------------------|-------------|---------|---------|------|
| NRESET assertion time after power supplies and clock stabilize     | $t_W$       | 2       | —       | ms   |
| Recovery time from reset inactive to device fully active           | $t_{REC}$   | —       | 105     | ms   |
| NRESET pulse width                                                 | $t_{W(RL)}$ | 100     | —       | ns   |
| Wait time between NRESET de-assert and access of the SMI interface | $t_{WAIT}$  | 105     | —       | ms   |

## 3.3 Operating Conditions

The following table shows the recommended operating conditions for the VSC8552 device.

**TABLE 3-31: RECOMMENDED OPERATING CONDITIONS**

| Parameter                                       | Symbol             | Minimum | Typical | Maximum | Unit |
|-------------------------------------------------|--------------------|---------|---------|---------|------|
| Power supply voltage for V <sub>DD1</sub>       | V <sub>DD1</sub>   | 0.95    | 1.00    | 1.05    | V    |
| Power supply voltage for V <sub>DD1A</sub>      | V <sub>DD1A</sub>  | 0.95    | 1.00    | 1.05    | V    |
| Power supply voltage for V <sub>DD25</sub>      | V <sub>DD25</sub>  | 2.38    | 2.50    | 2.62    | V    |
| Power supply voltage for V <sub>DD25A</sub>     | V <sub>DD25A</sub> | 2.38    | 2.50    | 2.62    | V    |
| VSC8552 operating temperature <sup>1</sup>      | T                  | 0       | —       | 125     | °C   |
| VSC8552-05 operating temperature <sup>(1)</sup> | T                  | −40     | —       | 125     | °C   |

1. Minimum specification is ambient temperature, and the maximum is junction temperature. For carrier class applications, the maximum operating temperature is 110 °C junction.

## 3.4 Stress Ratings

This section contains the stress ratings for the VSC8552 device.

**Warning** Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

**TABLE 3-32: STRESS RATINGS**

| Parameter                                             | Symbol               | Minimum               | Maximum | Unit |
|-------------------------------------------------------|----------------------|-----------------------|---------|------|
| Power supply voltage for core supply                  | V <sub>VDD1</sub>    | −0.3                  | 1.10    | V    |
| Power supply voltage for analog circuits              | V <sub>VDD1A</sub>   | −0.3                  | 1.10    | V    |
| Power supply voltage for analog circuits              | V <sub>VDD25A</sub>  | −0.3                  | 2.75    | V    |
| Power supply voltage for digital I/O                  | V <sub>VDD25</sub>   | −0.3                  | 2.75    | V    |
| Input voltage for GPIO and logic input pins           | —                    | —                     | 3.3     | V    |
| Storage temperature                                   | T <sub>S</sub>       | −55                   | 125     | °C   |
| Electrostatic discharge voltage, charged device model | V <sub>ESD_CDM</sub> | −250                  | 250     | V    |
| Electrostatic discharge voltage, human body model     | V <sub>ESD_HBM</sub> | See note <sup>1</sup> |         | V    |

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000V, but fails an ESD pulse of 4000V.

**Warning** This device can be damaged by electrostatic discharge (ESD) voltage. Microchip recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

## 4.0 PIN DESCRIPTIONS

The VSC8552 device has 256 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file so that you can copy it electronically. In Acrobat, double-click the attachment icon.

### 4.1 Pin Identifications

This section contains the pin descriptions for the VSC8552 device. The following table provides notations for definitions of the various pin types.

**TABLE 4-1: PIN TYPE SYMBOL DEFINITIONS**

| Symbol | Pin Type            | Description                                          |
|--------|---------------------|------------------------------------------------------|
| 3V     | —                   | 3.3V-tolerant pin.                                   |
| ABIAS  | Analog bias         | Analog bias pin.                                     |
| ADIFF  | Analog differential | Analog differential signal pair.                     |
| I      | Input               | Input without on-chip pull-up or pull-down resistor. |
| I/O    | Bidirectional       | Bidirectional input or output signal.                |
| NC     | No connect          | No connect pins must be left floating.               |
| O      | Output              | Output signal.                                       |
| OD     | Open drain          | Open drain output.                                   |
| OS     | Open source         | Open source output.                                  |
| PD     | Pull-down           | On-chip pull-down resistor to VSS.                   |
| PU     | Pull-up             | On-chip pull-up resistor to VDD_IO.                  |
| ST     | Schmitt-trigger     | Input has Schmitt-trigger circuitry.                 |

### 4.2 Pin Diagram

The following illustrations show the pin diagram for the VSC8552 device. For clarity, the device is shown in two halves, the top left and top right.

**FIGURE 4-1: PIN DIAGRAM, TOP LEFT**

|   | 1            | 2            | 3            | 4            | 5           | 6           | 7           | 8           |
|---|--------------|--------------|--------------|--------------|-------------|-------------|-------------|-------------|
| A | NC_1         | RESERVED_54  | RESERVED_56  | RESERVED_58  | RESERVED_60 | RESERVED_62 | RESERVED_64 | RESERVED_66 |
| B | VSS_1        | RESERVED_55  | RESERVED_57  | RESERVED_59  | RESERVED_61 | RESERVED_63 | RESERVED_65 | RESERVED_67 |
| C | REFCLK_N     | VDD25A_1     | THERMDA      | VDD25A_2     | VSS_3       | VDD25A_3    | VDD1A_1     | VDD1A_2     |
| D | REFCLK_P     | THERMDC_VSS  | REF_FILT_A   | REF_REXT_A   | VSS_6       | VSS_7       | VSS_8       | VSS_9       |
| E | REFCLK_SEL2  | TMS          | TRST         | VDD25A_6     | VDD1_1      | VSS_14      | VSS_15      | VSS_16      |
| F | TDO          | TDI          | TCK          | VSS_20       | VDD1_3      | VSS_21      | VSS_22      | VSS_23      |
| G | LED0_0       | LED1_0       | LED2_0       | LED3_0       | VDD1_5      | VSS_27      | VSS_28      | VSS_29      |
| H | LED0_1       | LED1_1       | LED2_1       | LED3_1       | VDD1_7      | VSS_33      | VSS_34      | VSS_35      |
| J | RGMII1_RXD0  | RGMII1_RXD1  | RGMII1_RXD2  | RGMII1_RXD3  | VDD1_9      | VSS_39      | VSS_40      | VSS_41      |
| K | RGMII1_TXCLK | RGMII1_TXCTL | RGMII1_RXCTL | RGMII1_RXCLK | VDD1_11     | VSS_45      | VSS_46      | VSS_47      |
| L | RGMII1_TXD0  | RESERVED_73  | COMA_MODE    | RESERVED_3   | VDD1_13     | VSS_51      | VSS_52      | VSS_53      |
| M | RGMII1_TXD1  | MDINT        | NRESET       | VDD25_2      | VDD1_15     | VSS_57      | VSS_58      | VSS_59      |
| N | RGMII1_TXD2  | MDIO         | RESERVED_71  | RESERVED_72  | VDD1_17     | VSS_63      | VSS_64      | VSS_65      |
| P | RGMII1_TXD3  | MDC          | VDD25_4      | RESERVED_4   | VDD25A_8    | VDD1A_5     | VDD1A_6     | VDD1A_7     |
| R | VSS_69       | RESERVED_22  | RESERVED_24  | RESERVED_26  | RESERVED_28 | RESERVED_30 | RESERVED_32 | RESERVED_34 |
| T | NC_3         | RESERVED_23  | RESERVED_25  | RESERVED_27  | RESERVED_29 | RESERVED_31 | RESERVED_33 | RESERVED_35 |

FIGURE 4-2: PIN DIAGRAM, TOP RIGHT

| 9           | 10         | 11       | 12       | 13              | 14                  | 15             | 16           |   |
|-------------|------------|----------|----------|-----------------|---------------------|----------------|--------------|---|
| RESERVED_68 | TXVPA_1    | TXVPB_1  | TXVPC_1  | TXVPD_1         | TXVPA_0             | TXVPB_0        | NC_2         | A |
| RESERVED_69 | TXVNA_1    | TXVNB_1  | TXVNC_1  | TXVND_1         | TXVNA_0             | TXVNB_0        | VSS_2        | B |
| VDD1A_3     | RESERVED_1 | VDD25A_4 | VSS_4    | VDD1A_4         | VDD25A_5            | TXVNC_0        | TXVPC_0      | C |
| VSS_10      | VSS_11     | VSS_12   | VSS_13   | RESERVED_2      | RGMII0_TXD3         | TXVND_0        | TXVPD_0      | D |
| VSS_17      | VSS_18     | VSS_19   | VDD1_2   | VDD25A_7        | RGMII0_TXD2         | CLK_SQUELCH_IN | RESERVED_70  | E |
| VSS_24      | VSS_25     | VSS_26   | VDD1_4   | RGMII0_TXD1     | PHYADD4             | RGMII0_TXD0    | RCVRDCLK1    | F |
| VSS_30      | VSS_31     | VSS_32   | VDD1_6   | PHYADD2         | PHYADD3             | RGMII0_TXCLK   | RCVRDCLK2    | G |
| VSS_36      | VSS_37     | VSS_38   | VDD1_8   | VDD25_1         | GPIO13              | RGMII0_TXCTL   | RGMII0_RXCLK | H |
| VSS_42      | VSS_43     | VSS_44   | VDD1_10  | RGMII0_RXCTL    | GPIO12              | RESERVED_18    | RESERVED_19  | J |
| VSS_48      | VSS_49     | VSS_50   | VDD1_12  | GPIO8/I2C_SDA   | GPIO9/FASTLINK-FAIL | GPIO10         | GPIO11       | K |
| VSS_54      | VSS_55     | VSS_56   | VDD1_14  | GPIO4/I2C_SCL_0 | GPIO5/I2C_SCL_1     | RGMII0_RXD0    | RGMII0_RXD1  | L |
| VSS_60      | VSS_61     | VSS_62   | VDD1_16  | VDD25_3         | GPIO1/SIGDET1       | RGMII0_RXD2    | RGMII0_RXD3  | M |
| VSS_66      | VSS_67     | VSS_68   | VDD1_18  | SerDes_Rext_1   | GPIO0/SIGDET0       | TDP_0          | TDN_0        | N |
| VDD1A_8     | VDD1A_9    | VDD1A_10 | VDD25A_9 | VDD25A_10       | SerDes_Rext_0       | RDP_0          | RDN_0        | P |
| RESERVED_36 | FIBROP_1   | FIBRIP_1 | RDP_1    | TDP_1           | FIBROP_0            | FIBRIP_0       | VSS_70       | R |
| RESERVED_37 | FIBRON_1   | FIBRIN_1 | RDN_1    | TDN_1           | FIBRON_0            | FIBRIN_0       | NC_4         | T |

### 4.3 Pins by Function

This section contains the functional pin descriptions for the VSC8552 device.

## 4.3.1 GPIO AND SIGDET

The following table lists the GPIO and SIGDET pins.

**TABLE 4-2: GPIO AND SIGDET PINS**

| Name            | Pin | Type        | Description                                                                                                                                                     |
|-----------------|-----|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO0/SIGDET0   | N14 | I/O, PU, 3V | General purpose input/output (GPIO). The multipurpose SIGDET pins, two-wire serial controller pins, and fast link fail pin can be configured to serve as GPIOs. |
| GPIO1/SIGDET1   | M14 |             |                                                                                                                                                                 |
| GPIO4/I2C_SCL_0 | L13 |             |                                                                                                                                                                 |
| GPIO5/I2C_SCL_1 | L14 |             |                                                                                                                                                                 |
| GPIO8/I2C_SDA   | K13 |             |                                                                                                                                                                 |
| GPIO10          | K15 |             |                                                                                                                                                                 |
| GPIO12          | J14 |             |                                                                                                                                                                 |
| GPIO13          | H14 |             |                                                                                                                                                                 |

## 4.3.2 JTAG

The following table lists the JTAG test pins.

**TABLE 4-3: JTAG PINS**

| Name | Pin | Type          | Description                                                                                                                          |
|------|-----|---------------|--------------------------------------------------------------------------------------------------------------------------------------|
| TCK  | F3  | I, PU, ST, 3V | JTAG test clock input.                                                                                                               |
| TDI  | F2  | I, PU, ST, 3V | JTAG test serial data input.                                                                                                         |
| TDO  | F1  | O             | JTAG test serial data output.                                                                                                        |
| TMS  | E2  | I, PU, ST, 3V | JTAG test mode select.                                                                                                               |
| TRST | E3  | I, PU, ST, 3V | JTAG reset.<br><b>Note:</b> When JTAG is not in use, this pin must be tied to ground with a pull-down resistor for normal operation. |

## 4.3.3 MISCELLANEOUS

The following table lists the miscellaneous pins.

**TABLE 4-4: MISCELLANEOUS PINS**

| Name                                                 | Pin                                    | Type      | Description                                                                                                                                                                                                                                                                                                                       |
|------------------------------------------------------|----------------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK_SQUELCH_IN                                       | E15                                    | I, PU, 3V | Input control to squelch recovered clock.                                                                                                                                                                                                                                                                                         |
| COMA_MODE                                            | L3                                     | I, PU, 3V | When this pin is asserted high, all PHYs are held in a powered down state. When de-asserted low, all PHYs are powered up and resume normal operation. This signal is also used to synchronize the operation of multiple chips on the same PCB to provide visual synchronization for LEDs driven by separate chips. <sup>(1)</sup> |
| LED0_[0:1]<br>LED1_[0:1]<br>LED2_[0:1]<br>LED3_[0:1] | G1, H1<br>G2, H2<br>G3, H3,<br>G4, H4, | O         | LED direct-drive outputs. All LEDs pins are active-low. A serial LED stream can also be implemented. See <a href="#">Section 2.2.26, LED Mode Select</a> .<br><b>Note:</b> LEDbit_port, where port = PHY port number and bit = the particular LED for the port.                                                                   |
| NC_1<br>NC_2<br>NC_3<br>NC_4                         | A1<br>A16<br>T1<br>T16                 | NC        | No connect.                                                                                                                                                                                                                                                                                                                       |

TABLE 4-4: MISCELLANEOUS PINS (CONTINUED)

| Name                          | Pin                                                                     | Type          | Description                                                                                                                                                                                                                                              |
|-------------------------------|-------------------------------------------------------------------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PHYADD2<br>PHYADD3<br>PHYADD4 | G13<br>G14<br>F14                                                       | I, PD,<br>3V  | Device SMI address bits 4:2.                                                                                                                                                                                                                             |
| RCVRDCLK1<br>RCVRDCLK2        | F16<br>G16                                                              | O             | Clock output can be enabled or disabled and also output a clock frequency of 125 MHz or 25 MHz based on the selected active recovered media programmed for this pin. This pin is not active when NRESET is asserted. When disabled, the pin is held low. |
| REF_FILT_A                    | D3                                                                      | ABIAS         | Reference filter connects to an external 1 $\mu$ F capacitor to analog ground.                                                                                                                                                                           |
| REF_REXT_A                    | D4                                                                      | ABIAS         | Reference external connects to an external 2 k $\Omega$ (1%) resistor to analog ground.                                                                                                                                                                  |
| REFCLK_N<br>REFCLK_P          | C1<br>D1                                                                | I,<br>ADIFF   | 125 MHz or 25 MHz reference clock input pair. Must be capacitively coupled and LVDS compatible.                                                                                                                                                          |
| REFCLK_SEL2                   | E1                                                                      | I, PU,<br>3 V | Selects the reference clock speed:<br>0: 25 MHz (VSS)<br>1: 125 MHz (2.5 V)<br>Use 125 MHz for typical applications.                                                                                                                                     |
| RESERVED_[1:4]                | C10, D13, L4,<br>P4                                                     | NC            | Leave these pins unconnected (floating).                                                                                                                                                                                                                 |
| RESERVED_[18:19]              | J15, J16                                                                | NC            | Leave these pins unconnected (floating).                                                                                                                                                                                                                 |
| RESERVED_[22:37]              | R2, T2, R3, T3,<br>R4, T4, R5, T5,<br>R6, T6, R7, T7,<br>R8, T8, R9, T9 | NC            | Leave these pins unconnected (floating).                                                                                                                                                                                                                 |
| RESERVED_[54:69]              | A2, B2, A3, B3,<br>A4, B4, A5, B5,<br>A6, B6, A7, B7,<br>A8, B8, A9, B9 | NC            | Leave these pins unconnected (floating).                                                                                                                                                                                                                 |
| RESERVED_[70:73]              | E16, N3, N4, L2                                                         | NC            | Leave these pins unconnected (floating).                                                                                                                                                                                                                 |
| THERMDA                       | C3                                                                      | A             | Thermal diode anode.                                                                                                                                                                                                                                     |
| THERMDC_VSS                   | D2                                                                      | A             | Thermal diode cathode connected to device ground. Temperature sensor must be chosen accordingly.                                                                                                                                                         |

1. For more information, see [Section 1.19.1, Initialization](#). For a typical bring-up example, see [Section 1.19, Configuration](#).

## 4.3.4 POWER SUPPLY

The following table lists the power supply pins and associated functional pins. All power supply pins must be connected to their respective voltage input, even if certain functions are not used for a specific application. No power supply sequencing is required. However, clock and power must be stable before releasing Reset.

**TABLE 4-5: POWER SUPPLY PINS**

| Name                    | Pin                                                                                                                                                                                                                                                                                                          | Type | Description                                                                                                                                                                    |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD1_[1:18]             | E5, E12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12, M5, M12, N5, N12                                                                                                                                                                                                                              | 1.0V | 1.0V internal digital logic.                                                                                                                                                   |
| VDD1A_[1:10]            | C7, C8, C9, C13, P6, P7, P8, P9, P10, P11                                                                                                                                                                                                                                                                    | 1.0V | 1.0V analog power requiring additional PCB power supply filtering. Associated with the QSGMII/SGMII MAC receiver output pins.                                                  |
| VDD25_[1:4]             | H13, M4, M13, P3                                                                                                                                                                                                                                                                                             | 2.5V | 2.5V general digital power supply. Associated with the LED, GPIO, JTAG, twisted pair interface, reference filter, reference external supply connect, and recovered clock pins. |
| VDD25A_[1:10]           | C2, C4, C6, C11, C14, E4, E13, P5, P12, P13                                                                                                                                                                                                                                                                  | 2.5V | 2.5V general analog power supply.                                                                                                                                              |
| VSS_[1:4]<br>VSS_[6:70] | B1, B16, C5, C12<br>D5, D6, D7, D8, D9, D10, D11, D12, E6, E7, E8, E9, E10, E11, F4, F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11, M6, M7, M8, M9, M10, M11, N6, N7, N8, N9, N10, N11, R1, R16 | 0V   | General device ground.                                                                                                                                                         |

### 4.3.4.1 RGMII Interface

The following table lists the RGMII interface pins.

**Note:** Unused RGMII port pins cannot be used as GPIOs.

**TABLE 4-6: RGMII INTERFACE PINS**

| Name                                                     | Pin                      | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------------------------------------------------------|--------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RGMII0_RXCLK                                             | H16                      | O    | Receive clock. Receive data is sourced from the PHY synchronously on the rising edge of RXCLK and is the recovered clock from the media.                                                                                                                                                                                                                                                                                                                                      |
| RGMII0_RXCTL                                             | J13                      | O    | Multiplexed receive data valid, receive error. This output is sampled by the MAC on opposite edges of RXCLK to indicate two receive conditions from the PHY:<br><br>1. On the rising edge of RXCLK, this output serves as RXDV and signals valid data is available on the RXD input data bus.<br><br>2. On the falling edge of RXCLK, this output signals a receive error from the PHY, based on a logical derivative of RXDV and RXER, as stated by the RGMII specification. |
| RGMII0_RXD0<br>RGMII0_RXD1<br>RGMII0_RXD2<br>RGMII0_RXD3 | L15<br>L16<br>M15<br>M16 | O    | Multiplexed receive data. Bits 3:0 are synchronously output on the rising edge of RXCLK and bits 7:4 on the falling edge of RXCLK.                                                                                                                                                                                                                                                                                                                                            |
| RGMII0_TXCLK                                             | G15                      | I    | Transmit clock. This clock is 2.5 MHz for 10 Mbps mode, 25 MHz for 100 Mbps mode, and 125 MHz for 1000 Mbps mode. If left unconnected, these pins require a pull-down resistor to ground.                                                                                                                                                                                                                                                                                     |
| RGMII0_TXCTL                                             | H15                      | I    | Multiplexed transmit enable, transmit error. This input is sampled by the PHY on opposite edges of TXCLK to indicate two transmit conditions of the MAC:<br><br>1. On the rising edge of TXCLK, this input serves as TXEN, indicating valid data is available on the TXD input data bus.<br><br>2. On the falling edge of TXCLK, this input signals a transmit error from the MAC, based on a logical derivative of TXEN and TXER, as stated by the RGMII specification.      |
| RGMII0_TXD0<br>RGMII0_TXD1<br>RGMII0_TXD2<br>RGMII0_TXD3 | F15<br>F13<br>E14<br>D14 | I    | Multiplexed transmit data. Bits 3:0 are synchronously output on the rising edge of TXCLK and bits 7:4 on the falling edge of TXCLK.                                                                                                                                                                                                                                                                                                                                           |
| RGMII1_RXCLK                                             | K4                       | O    | Receive clock. Receive data is sourced from the PHY synchronously on the rising edge of RXCLK and is the recovered clock from the media.                                                                                                                                                                                                                                                                                                                                      |
| RGMII1_RXCTL                                             | K3                       | O    | Multiplexed receive data valid, receive error. This output is sampled by the MAC on opposite edges of RXCLK to indicate two receive conditions from the PHY:<br><br>1. On the rising edge of RXCLK, this output serves as RXDV and signals valid data is available on the RXD input data bus.<br><br>2. On the falling edge of RXCLK, this output signals a receive error from the PHY, based on a logical derivative of RXDV and RXER, as stated by the RGMII specification. |

**TABLE 4-6: RGMII INTERFACE PINS (CONTINUED)**

| Name                                                     | Pin                  | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------------------------------------------------------|----------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RGMII1_RXD0<br>RGMII1_RXD1<br>RGMII1_RXD2<br>RGMII1_RXD3 | J1<br>J2<br>J3<br>J4 | O    | Multiplexed receive data. Bits 3:0 are synchronously output on the rising edge of RXCLK and bits 7:4 on the falling edge of RXCLK.                                                                                                                                                                                                                                                                                                                                       |
| RGMII1_TXCLK                                             | K1                   | I    | Transmit clock. This clock is 2.5 MHz for 10 Mbps mode, 25 MHz for 100 Mbps mode, and 125 MHz for 1000 Mbps mode. If left unconnected, these pins require a pull-down resistor to ground.                                                                                                                                                                                                                                                                                |
| RGMII1_TXCTL                                             | K2                   | I    | Multiplexed transmit enable, transmit error. This input is sampled by the PHY on opposite edges of TXCLK to indicate two transmit conditions of the MAC:<br><br>1. On the rising edge of TXCLK, this input serves as TXEN, indicating valid data is available on the TXD input data bus.<br><br>2. On the falling edge of TXCLK, this input signals a transmit error from the MAC, based on a logical derivative of TXEN and TXER, as stated by the RGMII specification. |
| RGMII1_TXD0<br>RGMII1_TXD1<br>RGMII1_TXD2<br>RGMII1_TXD3 | L1<br>M1<br>N1<br>P1 | I    | Multiplexed transmit data. Bits 3:0 are synchronously output on the rising edge of TXCLK and bits 7:4 on the falling edge of TXCLK.                                                                                                                                                                                                                                                                                                                                      |

## 4.3.5 SGMII/SERDES/QSGMII MAC INTERFACE

The following table lists the SerDes MAC interface pins.

**TABLE 4-7: SERDES MAC INTERFACE PINS**

| Name           | Pin        | Type     | Description                                                                              |
|----------------|------------|----------|------------------------------------------------------------------------------------------|
| RDN_0<br>RDP_0 | P16<br>P15 | O, ADIFF | PHY0 QSGMII/SGMII/SerDes MAC receiver output pair.                                       |
| RDN_1<br>RDP_1 | T12<br>R12 | O, ADIFF | SGMII/SerDes MAC receiver output pair.                                                   |
| SerDes_Rext_0  | P14        | ABIAS    | SerDes bias pins. Connect to a 620Ω 1% resistor between SerDes_Rext_0 and SerDes_Rext_1. |
| SerDes_Rext_1  | N13        | ABIAS    | SerDes bias pins. Connect to a 620Ω 1% resistor between SerDes_Rext_0 and SerDes_Rext_1. |
| TDN_0<br>TDP_0 | N16<br>N15 | I, ADIFF | PHY0 QSGMII/SGMII/SerDes MAC transmitter input pair.                                     |
| TDN_1<br>TDP_1 | T13<br>R13 | I, ADIFF | SGMII/SerDes MAC transmitter input pair.                                                 |

#### 4.3.6 SERDES MEDIA INTERFACE

The following table lists the SerDes media interface pins.

**TABLE 4-8: SERDES MEDIA INTERFACE PINS**

| Name                 | Pin        | Type     | Description                           |
|----------------------|------------|----------|---------------------------------------|
| FIBRIN_0<br>FIBRIN_1 | T15<br>T11 | I, ADIFF | SerDes media receiver input pair.     |
| FIBRIP_0<br>FIBRIP_1 | R15<br>R11 | I, ADIFF | SerDes media receiver input pair.     |
| FIBRON_0<br>FIBRON_1 | T14<br>T10 | O, ADIFF | SerDes media transmitter output pair. |
| FIBROP_0<br>FIBROP_1 | R14<br>R10 | O, ADIFF | SerDes media transmitter output pair. |

#### 4.3.7 SERIAL MANAGEMENT INTERFACE

The following table lists the serial management interface (SMI) pins. The SMI pins are referenced to VDD25 and can be set to a 2.5 V power supply.

**TABLE 4-9: SMI PINS**

| Name   | Pin | Type           | Description                                                                                                                                                                                                                                                                                                                                                     |
|--------|-----|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MDC    | P2  | I, PD, 3 V     | Management data clock. A 0 MHz to 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.                                                                                                                                                                                                                                           |
| MDINT  | M2  | I/O, OS, OD    | Management interrupt signal. Upon reset the device will configure these pins as active-low (open drain) or active-high (open source) based on the polarity of an external 10 kΩ resistor connection. These pins can be tied together in a wired-OR configuration with only a single pull-up or pull-down resistor.                                              |
| MDIO   | N2  | I/O, OD        | Management data input/output pin. Serial data is written or read from this pin bidirectionally between the PHY and Station Manager, synchronously on the positive edge of MDC. One external pull-up resistor is required at the Station Manager, and its value depends on the MDC clock frequency and the total sum of the capacitive loads from the MDIO pins. |
| NRESET | M3  | I, PD, ST, 3 V | Device reset. Active low input that powers down the device and sets all register bits to their default state.                                                                                                                                                                                                                                                   |

#### 4.3.8 TWISTED PAIR INTERFACE

The following table lists the twisted pair interface pins.

**TABLE 4-10: TWISTED PAIR INTERFACE PINS**

| Name               | Pin        | Type  | Description                     |
|--------------------|------------|-------|---------------------------------|
| TXVNA_0<br>TXVNA_1 | B14<br>B10 | ADIFF | TX/RX channel A negative signal |
| TXVNB_0<br>TXVNB_1 | B15<br>B11 | ADIFF | TX/RX channel B negative signal |
| TXVNC_0<br>TXVNC_1 | C15<br>B12 | ADIFF | TX/RX channel C negative signal |
| TXVND_0<br>TXVND_1 | D15<br>B13 | ADIFF | TX/RX channel D negative signal |
| TXVPA_0<br>TXVPA_1 | A14<br>A10 | ADIFF | TX/RX channel A positive signal |

**TABLE 4-10: TWISTED PAIR INTERFACE PINS (CONTINUED)**

| Name               | Pin        | Type  | Description                     |
|--------------------|------------|-------|---------------------------------|
| TXVPB_0<br>TXVPB_1 | A15<br>A11 | ADIFF | TX/RX channel B positive signal |
| TXVPC_0<br>TXVPC_1 | C16<br>A12 | ADIFF | TX/RX channel C positive signal |
| TXVPD_0<br>TXVPD_1 | D16<br>A13 | ADIFF | TX/RX channel D positive signal |

## 5.0 PACKAGE INFORMATION

VSC8552XKS-02 and VSC8552XKS-05 are packaged in a lead(Pb)-free, 256-pin, plastic ball grid array (BGA) with a 17 mm × 17 mm body size, 1 mm pin pitch, and 1.8 mm maximum height.

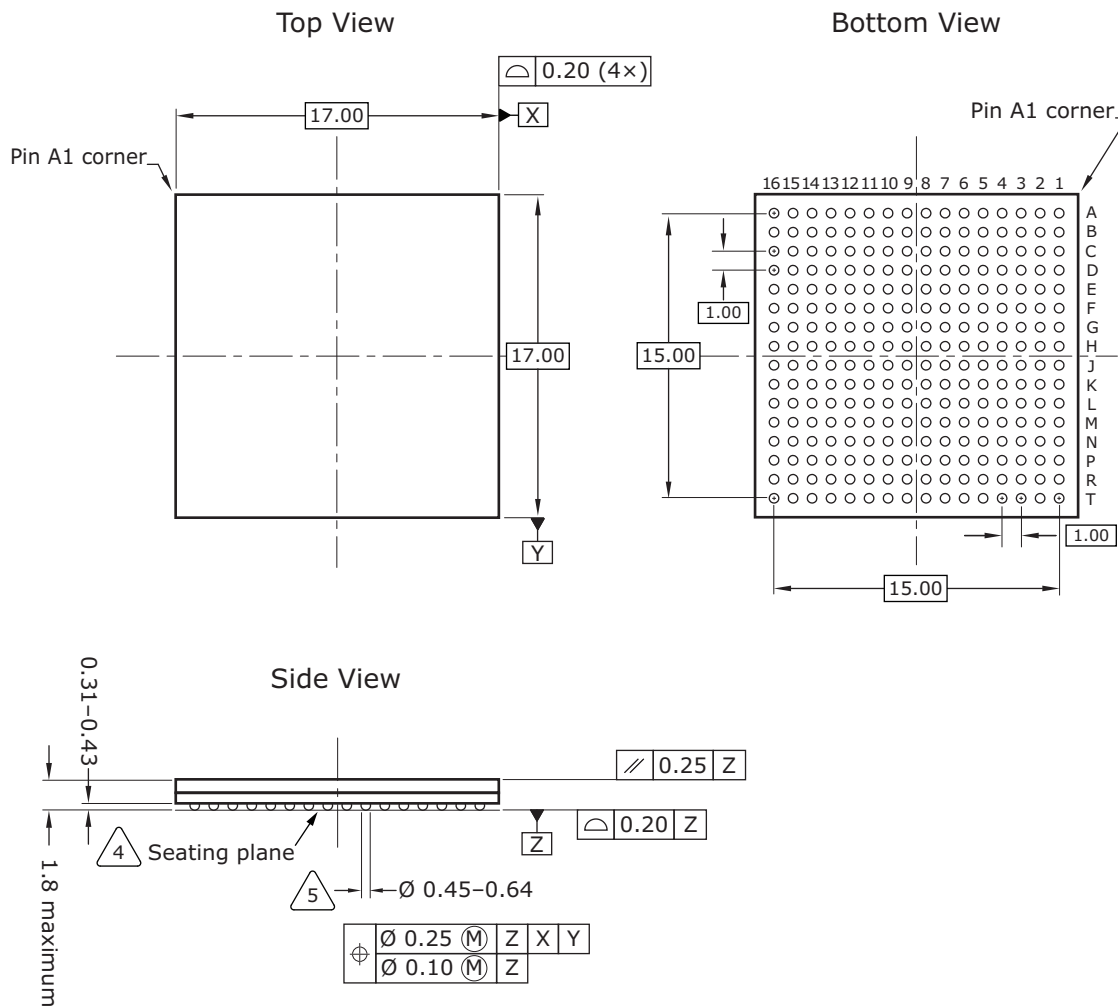
Lead(Pb)-free products from Microchip comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8552 device.

### 5.1 Package Drawing

The following illustration shows the package drawing for the VSC8552 device. The drawing contains the top view, bottom view, side view, dimensions, tolerances, and notes.

**FIGURE 5-1: PACKAGE DRAWING**



## Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Ball diameter is 0.50 mm.
3. Radial true position is represented by typical values.
4. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
5. Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.

## 5.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at [www.jedec.org](http://www.jedec.org). The thermal specifications are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

**TABLE 5-1: THERMAL RESISTANCES**

| Symbol                  | °C/W | Parameter                                                    |
|-------------------------|------|--------------------------------------------------------------|
| $\theta_{JCTop}$        | 5.9  | Die junction to package case top                             |
| $\theta_{JB}$           | 12.7 | Die junction to printed circuit board                        |
| $\theta_{JA}$           | 22   | Die junction to ambient                                      |
| $\theta_{JMA}$ at 1 m/s | 18.5 | Die junction to moving air measured at an air speed of 1 m/s |
| $\theta_{JMA}$ at 2 m/s | 16.3 | Die junction to moving air measured at an air speed of 2 m/s |

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using BGA packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

## 5.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

## 6.0 DESIGN CONSIDERATIONS

This section provides information about design considerations for the VSC8552 device.

### 6.1 Link Status LED Remains on while COMA\_MODE pin is Asserted High

When the COMA\_MODE is asserted high, the link status LED may not deactivate unless the media cable is disconnected from the device.

While using COMA\_MODE, link status should be verified using status registers rather than LED indicators.

### 6.2 LED Pulse Stretch Enable Turns OFF LED Pins

Enabling the pulse stretch function for LED0 or LED1 by setting register 30, bits 5:6 shuts off those LED pins.

Use the default blink function setting of LED0 and LED1 rather than pulse stretching. For more information, see [Section 2.2.27, LED Behavior](#).

### 6.3 AMS and 100BASE-FX

When the PHY operating mode (set in register 23) is AMS and the current active media is 100BASE-FX, register 0 bit 12 will be 0. This would normally indicate that auto-negotiation is disabled and the PHY is in forced mode. But in this mode, it has other meanings.

The workaround is to ensure that bit 12 is always written as 1 when doing writes or updates to register 0 in AMS mode.

### 6.4 10BASE-T Signal Amplitude

10BASE-T signal amplitude can be lower than the minimum specified in IEEE 802.3 paragraph 14.3.1.2.1 (2.2 V) at low supply voltages.

This issue is not estimated to present any system level impact. Performance is not impaired with cables up to 130 m with various link partners.

### 6.5 10BASE-T Link Recovery Failures

If the link disconnects when traffic is flowing while the device operates in a 10BASE-T mode, the PHY may not re-link.

There is a software workaround for this issue in which the device's internal microcontroller monitors link transitions in 10BASE-T mode and forces a soft power-down/power-up procedure to prevent a re-link failure.

A side effect of this software workaround is that the counts in registers 20 and 21 will be cleared (For more information, see [Section 2.2.18, Error Counter 2](#) and [Section 2.2.19, Error Counter 3](#)).

### 6.6 SNR Degradation and Link Drops

The link may drop after approximately 100 master/slave relationship swaps with the ring resiliency feature when using Category 5 (Cat5) cables that are longer than 75m.

The workaround is to use a combination of an initialization script and a procedure change. Contact Microchip for the workaround solution if the ring resiliency feature is being enabled.

### 6.7 Clause 45 Register 3.22

The clause 45, register 3.22 is cleared upon read only when the extended page access register (register 31) is set to 0.

This register cannot be read when the page access register is set to a value other than 0.

The workaround is to set extended page access register to 0 before accessing clause 45, register 3.22.

### 6.8 Clause 45 Register 3.1

Clause 45, register 3.1, Rx and Tx LPI received bits are cleared upon read only when the extended page access register (register 31) is set to 0.

This has a minor implication for software that needs to ensure that the extended page access register is set to 0 before reading clause 45, register 3.1.

The workaround is to set extended page access register to 0 before accessing clause 45, register 3.1.

## 6.9 Clause 45 Register Address Post-Increment

Clause 45 register address post-increment only works when reading registers and only when extended page access register (register 31) is set to 0.

The workaround is to access the registers individually.

## 6.10 Fast Link Failure Indication

The fast link failure indication for all the ports is enabled using port 0, register 19E.4.

The workaround is to set register 19E.4 = 1 in PHY 0 to enable Fast Link Fail indication.

## 6.11 Near-End Loopback with AMS Enabled

Near-end loopback does not work when AMS is enabled. Near-end loopback is controlled by setting bit 14 of register 0.

The workaround is to disable AMS when enabling loopback. This is a debug feature and does not have any real life implications.

## 6.12 Carrier Detect Assertion

Carrier detect assertion is set to false incorrectly when 9 out of 10 bits in the K28.1 word are in error.

No real life implication is expected, because the event that can trigger this error is extremely unlikely. If it does occur, the link may drop momentarily and come back up.

## 6.13 Link Status not Correct in Register 24E3.2 for 100BASE-FX Operation

The link status in register 24E3.2 only reflects the status of 1000BASE-X links. It does not reflect the status of 100BASE-FX links.

The workaround is to check register 28.4:3 for media operating mode (10 for fiber), 28.4:3 for speed status (100 for 100 Mbps), and then check 16.12 for current link status.

## 6.14 Register 28.14 does not Reflect Autonegotiation Disabled in 100BASE-FX Mode

Register 28.14 does not reflect autonegotiation status in 100BASE-FX mode. It works correctly in all copper and 1000BASE-X media modes.

The workaround is to use register 0.12 for autonegotiation status in 100BASE-FX mode when AMS is disabled. For more information about limitations when AMS is enabled, see [Section 6.3, AMS and 100BASE-FX](#).

## 6.15 Near-End Loopback Non-Functional in Protocol Transfer Mode

Near-end loopback does not work correctly when the device is configured in protocol transfer mode.

This is a debug feature and does not have any effect on the normal operation of the device.

## 6.16 Fiber-Media CRC Counters Non-Functional in Protocol Transfer Mode at 10 Mbps and 100 Mbps

Packets received on the media SerDes interface will not be counted correctly in registers 28E3 and 29E3 when the device is configured in protocol transfer mode and operating at 10 Mbps or 100 Mbps speeds.

These counters are used for debugging and there is no effect on the normal operation of the device.

## 6.17 Fiber-Media Recovered Clock does not Squelch Based on Link Status

To squelch the clock in fiber media mode, code sync status is used instead of link status. This causes the clock to not be squelched if the device is configured in 1000BASE-X mode with autonegotiation enabled when the transmit fiber is unplugged.

There is a software workaround for this issue where the device's internal microcontroller monitors link status and forces the clock off when no link is present.

## 6.18 1000BASE-X Parallel Detect Mode with Clause 37 Autonegotiation Enabled

When connected to a forced-mode link partner and attempting autonegotiation, the PHY in 1000BASEX parallel detect mode requires a minimum 250 ms IDLE stream in order to establish a link. If the PHY port is programmed with 1000BASE-X parallel detect-enabled (MAC-side register 16E3 bit 13, or media-side register 23E3 bit 13), then a forced-mode link partner sending traffic with an inter-packet gap less than 250 ms will not allow the local device's PCS to transition from a link-down to link-up state.

## 6.19 Anomalous PCS Error Indications in Energy Efficient Ethernet Mode

When a port is processing traffic with Energy Efficient Ethernet enabled on the link, certain PCS errors (such as false carriers, spurious start-of-stream detection, and idle errors) and EEE wake errors may occur. There is no effect on traffic bit error rate for cable lengths up to 75 meters, and minor packet loss may occur on links longer than 75 meters. Regardless of cable length, some error indications should not be used while EEE is enabled. These error indications include false carrier interrupts (Interrupt Status register 26 bit 3), receive error interrupts (Interrupt Status register 26 bit 0), and EEE wake error interrupts.

Contact Microchip for a script that needs to be applied during system initialization if EEE will be enabled.

## 6.20 Long Link-Up Times while in Forced 100BASE-TX Mode of Operation

While in forced 100BASE-TX operation and attempting to link up, the device may experience abnormally long link-up times.

This issue can only occur if the Unified API is not used with the device. In those circumstances, the workaround for this issue is to clear all speed advertisements in the autonegotiation advertisement registers (register 4, bits 9:5 and register 9, bits 9:8), then toggle the auto-negotiation enable bit of the mode control register (register 0, bit 12) for a port upon detecting its link is down. Any advertisements temporarily cleared can then be restored once register 0, bit 12 is cleared.

Contact Microchip for the latest code sequence included in the Unified API.

## 6.21 Station Managers Cannot use MDIO Address Offsets 0x2 and 0x3 with the PHY

In addition to responding to the two lowest MDIO addresses that can be resolved with device serial management interface address bits 4:2, the device will unexpectedly respond to offsets that have bit 1 set (for a detailed addressing diagram, see [Section 1.12.1, SMI Frames](#)). However, PHY2 and PHY3 are unusable targets on this device, so their corresponding MDIO addresses must not be used by the SMI station manager that controls this device. It is essential to avoid assigning addresses to other devices on the bus that would overlap the 0x2 and 0x3 offsets.

The workaround for this issue is to ensure the station manager connected to this device avoids using the two MDIO addresses immediately following the PHY1 target.

## 7.0 ORDERING INFORMATION

The VSC8552 device is offered with two operating temperature ranges. The range for VSC8552 is 0 °C ambient to 125 °C junction, and the range for VSC8552-05 is -40 °C ambient to 125 °C junction.

VSC8552XKS-02 and VSC8552XKS-05 are packaged in a lead(Pb)-free, 256-pin, plastic ball grid array (BGA) with a 17 mm × 17 mm body size, 1 mm pin pitch, and 1.8 mm maximum height.

Lead(Pb)-free products from Microchip comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8552 device.

**TABLE 7-1: ORDERING INFORMATION**

| Part Order Number | Description                                                                                                                                                                              |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VSC8552XKS-02     | Lead-free, 256-pin, plastic BGA with a 17 mm × 17 mm body size, 1 mm pin pitch, and 1.8 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction <sup>1</sup> .   |
| VSC8552XKS-05     | Lead-free, 256-pin, plastic BGA with a 17 mm × 17 mm body size, 1 mm pin pitch, and 1.8 mm maximum height. The operating temperature is -40 °C ambient to 125 °C junction <sup>1</sup> . |

1. For carrier class applications, the maximum operating temperature is 110 °C junction.

## APPENDIX A: REVISION HISTORY

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

### A.1 Revision A – 02/2023

Revision A is published in February 2023. The following is a summary of changes made in this revision.

- Migrated the datasheet from Microsemi format to the Microchip's template.

### A.2 Revision 4.2

Revision 4.2 was published in April 2019. The following is a summary of the changes in revision 4.2 of this document.

- The Block Diagram figure was updated. For more information, see [Figure 4](#).
- The IEEE 1588 Architecture figure was updated by removing reference to the pps functionality. For more information, see [Figure 8-23](#).
- The IEEE 1588 Device Synchronization section was updated by removing reference to the pps functionality. For more information, see [Section 8.11.17, IEEE 1588 Device Synchronization](#).
- The Timestamp Update section was updated by removing reference to the pps functionality. For more information, see [Section 8.11.18, Timestamp Update](#).
- The Timestamp Update section was updated by removing reference to the pps functionality. For more information, see [Section 8.11.18, Timestamp Update](#).
- The Local Time Counter section was updated by removing reference to the PPS0 functionality and the Local Time Counter Load/Save Timing figure. For more information, see [Section 8.11.23, Local Time Counter](#).
- The 1588\_PPS\_0/1 Mux Control section was deleted.
- The Register Bits for GPIO Control and Status table was updated by removing reference to the pps functionality. For more information, see [Table 1-11](#).
- The GPIO Control 2, Address 14G (0x0E) table was updated by removing reference to the pps functionality. For more information, see [Table 2-66](#).
- The GPIO Input, Address 15G (0x0F) table was updated by removing reference to the pps functionality. For more information, see [Table 2-67](#).
- The GPIO Output, Address 16G (0x10) table was updated by removing reference to the pps functionality. For more information, see [Table 2-68](#).
- The GPIO Input/Output Configuration, Address 17G (0x11) table was updated by removing reference to the pps functionality. For more information, see [Table 2-69](#).
- 
- The Registers in IP\_1588\_LTC table was updated by removing reference to the pps functionality. For more information, see .
- The Fields in LTC\_CTRL table was updated by removing reference to the pps functionality. For more information, see .
- The was removed.
- The IP\_1588:MISC\_CFG section was removed.
- The diagrams have been updated by removing references to the pps functionality. For more information, see [Figure 4-1](#) and [Figure 4-2](#).
- The 1588 Support Pins table was updated by removing references to the pps functionality. For more information, see [Table 4-2](#).
- The GPIO and 1588 Support Pins table was updated by removing references to the pps functionality. For more information, see [Table 4-3](#).
- The GPIO and SIGDET Pins table was updated by removing references to the pps functionality. For more information, see [Table 4-2](#).
- The 10BASE-T link recovery failures section was updated. For more information, see [Section 6.5, 10BASE-T Link Recovery Failures](#).

### A.3 Revision 4.1

Revision 4.1 was published in May 2018. The following is a summary of the changes in revision 4.1 of this document.

- Configuration procedure steps were clarified. For more information, see [Section 1.19, Configuration](#).
- The description of bit 10 was updated for register 0. For more information, see [Table 2-3](#).
- The description of bit 0 was updated for register 22. For more information, see [Section 2.2.20, Extended Control and Status](#).
- Design considerations were updated. For more information, see [Section 6.0, Design Considerations](#).

## A.4 Revision 4.0

Revision 4.0 was published in November 2017. The following is a summary of the changes in revision 4.0 of this document.

- A note was added about enhanced serial LED mode using the  $V_{DD}$  LED drive state.
- Details about LED pulsing were updated.
- Information on enabling the serial clock was added.
- Register bits were designated as “sticky” where appropriate.
- A footnote was added about the fast link failure interrupt mask.
- The default for the ring resiliency status bits 4:4 was updated from 00 to 11.
- The default value for the MAC SerDes clause 37 advertised ability register was updated from 0x0000 to 0x01E0.
- Footnotes regarding required register clears were added to the SIGDET/GPIO control register.
- All GPIO input register bits marked as read-only and defaults updated.
- Global interrupt status register defaults were added.
- Register 30G changed from reserved to extended revision ID register.
- Current consumption values were updated.
- Some parameter names and conditions for recovered clock AC characteristics were updated.
- Product SKUs in the package section were corrected to match the ordering information.
- Design considerations were removed and new ones added to correctly reflect device functionality.

## A.5 Revision 2.0

Revision 2.0 of this datasheet was published in September 2017. This was the first publication of the document.

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