REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19															
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Rajesh Pithadia	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Rajesh Pithadia	
	APPROVED BY Charles F. Saffle	MICROCIRCUIT, LINEAR, MICROPOWER, OVERVOLTAGE PROTECTION, OPERATIONAL AMPLIFIER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 15-06-01	
	REVISION LEVEL	SIZE A
		CAGE CODE **67268**
		5962-14206
		SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	R	14206	01	V	X	A
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
Drawing number						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADA4096-2	Radiation hardened, dual, 30 V, micropower, overvoltage protection, operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F10	10	Bottom brazed flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

Supply voltage (+V_{SY} to –V_{SY})	36 V
Input voltage (V_{IN}):	
Operating	-V_{SY} to +V_{SY}
Overvoltage condition 2/	-V_{SY} – 32 V to + V_{SY} + 32 V
Differential input voltage 3/	±V_{SY}
Input current	±5 mA
Output short circuit duration to GND	Indefinite
Storage temperature range	-65°C to +150°C
Maximum junction temperature (T_J)	+150°C
Lead temperature (soldering, 60 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	17°C/W 4/
Thermal resistance, junction-to-ambient (θ_{JA})	27°C/W 4/

1.4 Recommended operating conditions.

Supply voltage (±V_{SY})	±1.8 V to ±15.0 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.4.1 Operating performance characteristics. 5/

Input capacitance:	
Differential (C_{DM}) V_{SY} = ±15 V	2.5 pF
Common mode (C_{CM}) V_{SY} = ±15 V	7.0 pF
Settling time (t_S) to 0.1%, 10 V step, V_{SY} = ±15 V	23.4 µs
Closed loop impedance (Z_{OUT} f = 100 kHz, A_V = 1):	
V_{SY} = ±1.5 V	102 Ω
V_{SY} = ±5 V	71 Ω
V_{SY} = ±15 V	40 Ω
Unity gain crossover (V_{IN} = 5 mV_{P-P}, R_L = 10 kΩ, A_V = 1):	
V_{SY} = ±1.5 V	465 kHz
V_{SY} = ±5 V	550 kHz
V_{SY} = ±15 V	800 kHz
Phase margin:	
V_{SY} = ±1.5 V	51°
V_{SY} = ±5 V	52°
V_{SY} = ±15 V	60°
-3 dB closed loop bandwidth (V_{IN} = 5 mV_{P-P}, A_V = 1):	
V_{SY} = ±1.5 V	672 kHz
V_{SY} = ±5 V	783 kHz
V_{SY} = ±15 V	1029 kHz
Noise performance (V_{SY} = ±1.5 V, V_{SY} = ±5 V, V_{SY} = ±15 V):	
Voltage noise (e_{nP-P}, 0.1 Hz to 10 Hz)	0.7 V_{P-P}
Voltage noise density (e_n, f = 1 kHz)	27 nV/$\sqrt{Hz}$
Current noise density (in, f = 1 kHz)	0.2 pA/$\sqrt{Hz}$
Channel separation (V_{SY} = ±15 V)	100 dB

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Performance not guaranteed during overvoltage conditions.
3/ Limit the input current to ±5 mA.
4/ Measurement taken under absolute worst case condition and represents data taken with thermal camera for highest power density location. See MIL-STD-1835 for base line values of θ_{JC}.
5/ Unless otherwise specified, T_A = 25°C and V_{CM} = 0 V.

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) .... 100 krads(Si) 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

6/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ $V_{SY} = \pm 1.65$ V $V_{CM} = 0$ V $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input characteristics							
Offset voltage	V_{OS}		1	01	-300	300	µV
			2, 3		-500	500	
		M, D, P, L, R	1		-300	300	
Offset voltage matching	$V_{OSA} - V_{OSB}$		1	01	-300	300	µV
			2, 3		-500	500	
		M, D, P, L, R	1		-300	300	
Offset voltage drift	$\Delta V_{OS} / \Delta T$	4/ 5/	2, 3	01	-3	2	µV/°C
Input bias current	I_B	6/	1	01	-25	0	nA
			2		-30	5	
			3		-35	0	
		M, D, P, L, R	1		-25	0	
		$V_{CM} = +V_{SY}$ 6/	1		0	25	
			2		-10	35	
			3		0	45	
		M, D, P, L, R	1		0	25	
		$V_{CM} = -V_{SY}$ 6/	1		-45	-15	
			2		-50	5	
			3		-65	10	
		M, D, P, L, R	1		-45	-15	
Input offset current	I_{OS}		1, 2	01	-1.5	1.5	nA
			3		-3	3	
		M, D, P, L, R	1		-1.5	1.5	
Input voltage range	IVR		1, 2, 3	01	$-V_{SY}$	$+V_{SY}$	V
		M, D, P, L, R	1		$-V_{SY}$	$+V_{SY}$	
Common-mode rejection ratio	CMRR	$V_{CM} = -V_{SY}$ to $+V_{SY}$	1	01	61		dB
			2, 3		58		
		M, D, P, L, R	1		61		
Large signal voltage gain	A_{VO}	$R_L = 10$ kΩ, $V_O = -V_{SY} + 0.1$ V to $+V_{SY} - 0.1$ V	1	01	91		dB
			2, 3		84		
		M, D, P, L, R	1		91		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ V_{SY} = ±1.65 V V_{CM} = 0 V -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input characteristics – continued.								
Large signal voltage gain	A_{VO}	R_L = 2 kΩ, V_O = $-V_{SY}$ + 0.2 V to $+V_{SY}$ – 0.2 V		1	01	86		dB
				2, 3		77		
			M, D, P, L, R	1		86		
Output characterisitics								
Output voltage high	V_{OH}	R_L = 10 kΩ to GND		1	01	$+V_{SY}$ - 0.02		V
				2, 3		$+V_{SY}$ - 0.05		
			M, D, P, L, R	1		$+V_{SY}$ - 0.02		
		R_L = 2 kΩ to GND		1		$+V_{SY}$ - 0.05		
				2, 3		$+V_{SY}$ - 0.1		
			M, D, P, L, R	1		$+V_{SY}$ - 0.05		
Output voltage low	V_{OL}	R_L = 10 kΩ to GND		1	01		$-V_{SY}$ + 0.02	V
				2, 3			$-V_{SY}$ + 0.05	
			M, D, P, L, R	1			$-V_{SY}$ + 0.02	
		R_L = 2 kΩ to GND		1			$-V_{SY}$ + 0.04	
				2, 3			$-V_{SY}$ + 0.1	
			M, D, P, L, R	1			$-V_{SY}$ + 0.04	
Short circuit limit	I_{SC+}	Source		1, 2, 3	01	-11	-1	mA
			M, D, P, L, R	1		-11	-1	
	I_{SC-}	Sink		1, 2, 3		2	13	
			M, D, P, L, R	1		2	13	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/ V_{SY} = ±1.65 V V_{CM} = 0 V -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply							
Power supply rejection ratio	PSRR	V_{SY} = 3.3 V to 36 V	1	01	100		dB
			2, 3		90		
		M, D, P, L, R	1		100		
Total supply current (both amplifiers)	I_{SY}	V_O = 0 V	1	01		100	µA
			2			140	
			3			130	
		M, D, P, L, R	1			100	
Dynamic performance							
Slew rate	SR	R_L = 10 kΩ, C_L = 100 pF 4/ 7/ 8/	4	01	0.15		V/µs
			5		0.25		
			6		0.09		
Gain bandwidth product	GBP	V_{IN} = 5 mV_{P-P}, R_L = 10 kΩ, A_V = -100 4/ 7/	4, 5, 6	01	350		kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $V_{SY} = \pm 5$ V $V_{CM} = 0$ V $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input characteristics							
Offset voltage	V_{OS}		1	01	-300	300	µV
			2, 3		-500	500	
		M, D, P, L, R	1		-300	300	
Offset voltage matching	$V_{OSA} - V_{OSB}$		1	01	-300	300	µV
			2, 3		-500	500	
		M, D, P, L, R	1		-300	300	
Offset voltage drift	$\Delta V_{OS} / \Delta T$	4/ 5/	2, 3	01	-3	2	µV/°C
Input bias current	I_B	6/	1	01	-25	0	nA
			2		-25	10	
			3		-35	0	
		M, D, P, L, R	1		-25	0	
		$V_{CM} = +V_{SY} - 2.5$ V 6/	1		-20	5	
			2		-30	15	
			3		-35	10	
		M, D, P, L, R	1		-20	5	
		$V_{CM} = -V_{SY} + 2.5$ V 6/	1		-30	0	
			2		-35	10	
			3		-40	5	
		M, D, P, L, R	1		-25	0	
		$V_{CM} = +V_{SY}$ 6/	1		0	25	
			2		-10	35	
			3		0	45	
		M, D, P, L, R	1		10	35	
		$V_{CM} = -V_{SY}$ 6/	1		-45	-15	
			2		-50	5	
			3		-70	-15	
		M, D, P, L, R	1		-40	-15	

See footnotes at end of table

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $V_{SY} = \pm5$ V $V_{CM} = 0$ V $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input characteristics – continued.							
Input offset current	I_{OS}		1	01	-2	2	nA
			2, 3		-3	3	
		M, D, P, L, R	1		-2	2	
Input voltage range	IVR		1, 2, 3	01	$-V_{SY}$	$+V_{SY}$	V
		M, D, P, L, R	1		$-V_{SY}$	$+V_{SY}$	
Common-mode rejection ratio	CMRR	$V_{CM} = -V_{SY}$ to $+V_{SY}$	1	01	72		dB
			2, 3		68		
		M, D, P, L, R	1		72		
		$V_{CM} = -V_{SY} + 2$ V to $+V_{SY} - 2$ V	1	01	91		
			2, 3		85		
		M, D, P, L, R	1		91		
Large signal voltage gain	A_{VO}	$R_L = 10$ kΩ, $V_O = -V_{SY} + 0.2$ V to $+V_{SY} - 0.2$ V	1	01	102		dB
			2, 3		99		
		M, D, P, L, R	1		102		
		$R_L = 2$ kΩ, $V_O = -V_{SY} + 0.3$ V to $+V_{SY} - 0.3$ V	1	01	93		
		$R_L = 2$ kΩ, $V_O = -V_{SY} + 0.3$ V to $+V_{SY} - 0.3$ V	2		88		
		$R_L = 2$ kΩ, $V_O = -V_{SY} + 0.4$ V to $+V_{SY} - 0.4$ V	3		88		
		M, D, P, L, R	1		93		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ V_{SY} = ±5 V V_{CM} = 0 V -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output characteristics							
Output voltage high	V_{OH}	R_L = 10 kΩ to GND	1	01	$+V_{SY}$ - 0.04		V
			2, 3		$+V_{SY}$ - 0.05		
		M, D, P, L, R	1		$+V_{SY}$ - 0.04		
		R_L = 2 kΩ to GND	1		$+V_{SY}$ - 0.2		
			2, 3		$+V_{SY}$ - 0.3		
		M, D, P, L, R	1		$+V_{SY}$ - 0.2		
Output voltage low	V_{OL}	R_L = 10 kΩ to GND	1	01		$-V_{SY}$ + 0.03	V
			2, 3			$-V_{SY}$ + 0.05	
		M, D, P, L, R	1			$-V_{SY}$ + 0.03	
		R_L = 2 kΩ to GND	1			$-V_{SY}$ + 0.2	
			2, 3			$-V_{SY}$ + 0.25	
		M, D, P, L, R	1			$-V_{SY}$ + 0.2	
Short circuit limit	I_{SC+}	Source	1, 2	01	-18	-6	mA
			3		-14	-2	
		M, D, P, L, R	1		-18	-6	
	I_{SC-}	Sink	1, 2, 3		3	16	
		M, D, P, L, R	1		3	16	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ V_{SY} = ±5 V V_{CM} = 0 V -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power supply								
Total supply current (both amplifiers)	I_{SY}	V_O = 0 V		1	01		110	µA
				2, 3			150	
			M, D, P, L, R	1			110	
Dynamic performance								
Slew rate	SR	R_L = 10 kΩ, C_L = 100 pF 4/ 7/ 8/		4	01	0.2		V/µs
				5		0.3		
				6		0.12		
Gain bandwidth product	GBP	V_{IN} = 5 mV_{P-P}, R_L = 10 kΩ, A_V = -100 4/ 7/		4, 5, 6	01	450		kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ $V_{SY} = \pm15$ V $V_{CM} = 0$ V -55°C ≤ T_A ≤ +125°C unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input characteristics								
Offset voltage	V_{OS}			1	01	-300	300	µV
				2, 3		-500	500	
			M, D, P, L, R	1		-300	300	
Offset voltage matching	V_{OSA} - V_{OSB}			1	01	-300	300	µV
				2, 3		-500	500	
			M, D, P, L, R	1		-300	300	
Offset voltage drift	ΔV_{OS} / ΔT	4/ 5/		2, 3	01	-3	2	µV/°C
Input bias current	I_B	6/		1	01	-20	5	nA
				2, 3		-25	10	
			M, D, P, L, R	1		-20	5	
		$V_{CM} = +V_{SY} - 2.5$ V 6/		1		-10	15	
				2, 3		-20	25	
			M, D, P, L, R	1		-10	15	
		$V_{CM} = -V_{SY} + 2.5$ V 6/		1		-35	-5	
				2		-40	5	
				3		-50	-5	
			M, D, P, L, R	1		-35	-5	
		$V_{CM} = +V_{SY}$ 6/		1		10	35	
				2		-5	40	
				3		10	55	
			M, D, P, L, R	1		10	35	
		$V_{CM} = -V_{SY}$ 6/		1		-55	-25	
				2		-55	0	
				3		-80	-25	
			M, D, P, L, R	1		-55	-25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ V_{SY} = ±15 V V_{CM} = 0 V -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input characteristics – continued.							
Input offset current	I_{OS}		1, 2	01	-1.5	1.5	nA
			3		-3	3	
		M, D, P, L, R	1		-1.5	1.5	
Input voltage range	IVR		1, 2, 3	01	$-V_{SY}$	$+V_{SY}$	V
		M, D, P, L, R	1		$-V_{SY}$	$+V_{SY}$	
Common-mode rejection ratio	CMRR	$V_{CM} = -V_{SY}$ to $+V_{SY}$	1	01	81		dB
			2, 3		75		
		M, D, P, L, R	1		81		
		$V_{CM} = -V_{SY} + 2$ V to $+V_{SY} - 2$ V	1	01	95		
			2, 3		89		
		M, D, P, L, R	1		95		
Large signal voltage gain	A_{VO}	R_L = 10 kΩ, $V_O = -V_{SY} + 0.3$ V to $+V_{SY} - 0.3$ V	1	01	109		dB
			2, 3		105		
		M, D, P, L, R	1		109		
		R_L = 2 kΩ, $V_O = -V_{SY} + 4$ V to $+V_{SY} - 4$ V	1	01	99		
		R_L = 2 kΩ, $V_O = -V_{SY} + 4$ V to $+V_{SY} - 4$ V	2		90		
		R_L = 2 kΩ, $V_O = -V_{SY} + 5$ V to $+V_{SY} - 5$ V	3		90		
		M, D, P, L, R	1		99		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ V_{SY} = ±15 V V_{CM} = 0 V -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output characteristics							
Output voltage high	V_{OH}	R_L = 10 kΩ to GND	1	01	$+V_{SY}$ - 0.08		V
			2, 3		$+V_{SY}$ - 0.25		
		M, D, P, L, R	1		$+V_{SY}$ - 0.08		
		R_L = 2 kΩ to GND	1, 2		$+V_{SY}$ - 1		
			3		$+V_{SY}$ - 6		
		M, D, P, L, R	1		$+V_{SY}$ - 1		
Output voltage low	V_{OL}	R_L = 10 kΩ to GND	1	01		$-V_{SY}$ + 0.08	V
			2, 3			$-V_{SY}$ + 0.25	
		M, D, P, L, R	1			$-V_{SY}$ + 0.08	
		R_L = 2 kΩ to GND	1			$-V_{SY}$ + 0.75	
			2			$-V_{SY}$ + 1.5	
			3			$-V_{SY}$ + 3	
		M, D, P, L, R	1			$-V_{SY}$ + 0.75	
Short circuit limit	I_{SC+}	Source	1	01	-28	-17	mA
			2		-34	-20	
			3		-28	-6	
		M, D, P, L, R	1		-28	-17	
	I_{SC-}	Sink	1, 2, 3		8	18	
		M, D, P, L, R	1		8	18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ V_{SY} = ±15 V V_{CM} = 0 V -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Power supply							
Total supply current (both amplifiers)	I_{SY}	V_O = 0 V, V_{SY} = ±15 V and V_{SY} = ±16.5 V	1	01		150	µA
			2, 3			200	
		M, D, P, L, R	1			150	
Dynamic performance							
Slew rate	SR	R_L = 10 kΩ, C_L = 100 pF 4/ 7/ 8/	4	01	0.3		V/µs
			5		0.4		
			6		0.2		
Gain bandwidth product	GBP	V_{IN} = 5 mV_{P-P}, R_L = 10 kΩ, A_V = -100 4/ 7/	4, 5, 6	01	600		kHz

1/ Device type 01 supplied to this drawing has been characterized through all levels M, D, P, L, R of irradiation. However, device type 01 is only tested at the “R” level. Pre and post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurement for any RHA level, T_A = +25°C.

2/ Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

3/ V_{SY} = ±1.8 V recommended operating condition guaranteed by 100% production test at V_{SY} = ±1.65 V minimum recommended operating condition.

4/ Parameter is not tested post radiation.

5/ Calculated from 25°C to -55°C, 25°C to 125°C, and -55°C to 125°C

6/ Input bias current depends on $\pm V_S$, V_{CM}, and temperature. Refer to the input bias current versus V_{CM} and temperature graphs for various $\pm V_S$ in the manufactuer’s datasheet.

7/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

8/ Measured from 10% to 90% and 90% to 10% of rail to rail output swing.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
1	OUT A	Analog output	Operational amplifier output, Amplifier A
2	-IN A	Analog input	Operational amplifier negative input, Amplifier A
3	NC/GND	N/A	No connection or ground this terminal
4	+IN A	Analog input	Operational amplifier positive input, Amplifier A
5	$-V_S$	Power	Negative power supply
6	+IN B	Analog input	Operational amplifier positive input, Amplifier B
7	-IN B	Analog input	Operational amplifier negative input, Amplifier B
8	NC/GND	N/A	No connection or ground this terminal
9	OUT B	Analog output	Operational amplifier output, Amplifier B
10	$+V_S$	Power	Positive power supply

FIGURE 1. Terminal connections.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/ 2/	1,2,3,4,5,6 2/ 3/
Group A test requirements (see 4.4)	1,2,3,4,5,6 2/	1,2,3,4,5,6 2/
Group C end-point electrical parameters (see 4.4)	1,2,3,4,5,6 2/	1,2,3,4,5,6 2/ 3/
Group D end-point electrical parameters (see 4.4)	1,2,3,4,5,6 2/	1,2,3,4,5,6 2/
Group E end-point electrical parameters (see 4.4)	1	1

1/ PDA applies to subgroup 1 only. Deltas are not excluded from PDA
2/ Parameters marked with footnote 5/ in Table I are part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.
3/ Delta limits as specified in Table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test delta parameters. 1/

Parameter	Device types	Symbol	Limits		Units
			Min	Max	
Offset voltage	01	V_{OS}	-50	+50	µV
Input bias current, V_{CM} = 0 V	01	I_B	-1.6	+1.6	nA
Supply current	01	I_{SY}	-4	+4	µA

1/ 240 hour burn-in and group C end point electrical parameters. Deltas are performed at T_A = +25°C.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Application notes.

6.7.1 General Description. The device's dual operational amplifier features micropower operation and rail-to-rail input and output ranges. The extremely low power requirements and guaranteed operation from 3 V to 30 V make these amplifiers perfectly suited to monitor battery usage and to control battery charging. Their dynamic performance, including 27 $nV/\sqrt{Hz}$ voltage noise density, recommends them for low power applications. Capacitive loads to 200 pF are handled without oscillation. The device has overvoltage protection inputs and diodes that allow the voltage input to extend 32 V above and below the supply rails, making this device ideal for robust applications. The device features a unique input stage that allows the input voltage to exceed either supply safely without any phase reversal or latch-up. This is called input overvoltage protection, or OVP. See manufacturer's datasheet for application information.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-06-01

Approved sources of supply for SMD 5962-14206 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1420601VXA	24355	ADA4096-2AF/QMLR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 7910 Triad Center Drive Greensboro, NC 27409-9605