REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made changes to table I and editorial changes throughout. Changed PDA from 10 percent to 5 percent.	91-03-06	M. A. Frye
B	Changes in accordance with NOR 5962-R196-92.	92-11-02	M. A. Frye
C	Incorporate revision B NOR. Update drawing to current requirements. Editorial changes throughout. - drw	05-12-16	Raymond Monnin

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
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REV STATUS	REV	C	C	C	C	C	C	C	C						
OF SHEETS	SHEET	1	2	3	4	5	6	7	8						

PMIC N/A	PREPARED BY Gary Zahn	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY William E. Shoup	
	APPROVED BY N. A. Hauck	MICROCIRCUIT, LINEAR, 12-BIT D/A CONVERTER, RANGE PROGRAMMABLE, VOLTAGE OUTPUT, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 83-10-04	
	REVISION LEVEL C	SIZE: A; CAGE CODE: **14933**; **83003**
		SHEET 1 OF 8

DSCC FORM 2233
APR 97

5962-E151-06

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

83003	01	J	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	DAC87	D/A converter, 12-bit with voltage Ranges as follows: 0 V to +5 V unipolar 0 V to +10 V unipolar -2.5 V to +2.5 V bipolar -5 V to +5 V bipolar -10 V to +10 V bipolar

1.2.2 Case outline. The case outline is as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Positive supply voltage V_{CC} to digital return	+18 V dc
Negative supply voltage V_{EE} to digital return	-18 V dc
Digital input voltage to digital return	0 V dc to 7.0 V dc
Output short circuit duration (to ground only)	25 ms
Lead temperature (soldering, 60 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	48°C/W
Power dissipation (P_D) 1/	550 mW

1.4 Recommended operating conditions.

Positive supply voltage (V_{CC})	+16.5 V dc
Negative supply voltage (V_{EE})	-16.5 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution					12		Bits
Supply current from V_{CC}	I_{CC}	Input bits = 1111 1111 1111, V_{CC} = 15 V	1, 2, 3	01	1	10	mA
Supply current from V_{EE}	I_{EE}	Input bits = 0000 0000 0000, V_{CC} = -15 V	1, 2, 3	01	-20	-1	mA
Digital input low current	I_{IL}	V_{IN} = 0.8 V, V_{CC} = 15 V, (each input measured separately)	1, 2, 3	01	0	+100	µA
Digital input high current	I_{IH}	V_{IN} = 5.5 V, V_{CC} = 15 V	1, 2, 3	01	-1	+250	µA
Output short circuit current	I_{OS}	Input bits = 0000 0000 0000	1, 2, 3	01		40	mA
Reference voltage	V_{REF}	I_O = -2.5 mA, T_A = +25°C	1	01	6.23	6.37	V
Reference voltage drift	dV_{REF}/dT	2/	2, 3	01	-10	+10	PPM/°C
Unipolar offset voltage error	V_{OS}	Input bits = 1111 1111 1111, Unipolar, V_{FSR} = 10 V, T_A = +25°C	1	01	-0.1	+0.1	% FSR
Unipolar offset voltage drift	dV_{OS}/dT	2/	2, 3	01	-3	+3	PPM/°C
Gain error 3/	AE	Input bits = 0000 0000 0000, Input bits = 1111 1111 1111, Unipolar, V_{FSR} = 10 V, T_A = +25°C	1	01	-0.2	+0.2	% FSR
Gain error drift	dAE/dT	2/	2, 3	01	-20	+20	PPM/°C
Bipolar gain error 4/	BPAE	Input bits = 0000 0000 0000, Input bits = 1111 1111 1111, T_A = +25°C	1	01	-0.2	+0.2	% FSR
Bipolar offset error 4/	BPOE	Input bits = 1111 1111 1111, T_A = +25°C	1	01	-0.1	+0.1	% FSR
Bipolar offset error drift	dBPOE/dT	2/	2, 3	01	-10	+10	PPM/°C
Bipolar zero error 4/	BZE	Input bits = 0111 1111 1111, T_A = +25°C	1	01	-4	+4	LSB
Bipolar zero error drift	dBZE/dT	2/	2, 3	01	-10	+10	PPM/°C
Power supply sensitivity from V_{CC} at full scale	+PSRR	Input bits = 0000 0000 0000, $+13.5 V \le V_{CC} \le +16.5 V$, $+11.4 V \le V_{CC} \le +12.6V$, V_{EE} = -15 V, V_{EE} = -12 V	1, 2, 3	01	-0.002	+0.002	$\frac{\%\Delta FSR}{\%\Delta V_{CC}}$
Power supply sensitivity from V_{EE} at full scale	-PSRR	Input bits = 0000 0000 0000, $-13.5 V \le V_{CC} \le -16.5 V$, $-12.6 V \le V_{CC} \le -11.4 V$, V_{CC} = +15 V, V_{CC} = +12 V	1, 2, 3	01	-0.002	+0.002	$\frac{\%\Delta FSR}{\%\Delta V_{EE}}$

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Integral linearity error	LE	(Abbreviate codes test) 5/		1	01	-0.5	+0.5	LSB
				2, 3		-0.75	+0.75	
Differential linearity error	DLE	(Abbreviate codes test)		1	01	-0.75	+0.75	LSB
				2, 3		-1.0	+1.0	
Integral linearity error	LE	(All codes test)		7	01	-0.5	+0.5	LSB
				8		-0.75	+0.75	
Settling time 6/	t_{SLH}		20 V to ±1/2 LSB	9	01		5	µs
		T_A = +25°C	20 V to ±1 LSB				4	
		Input bits = 1111 1111 1111 to input bits = 0000 0000 0000						
		1 LSB to ±1/2 LSB, T_A = +25°C Input bits = 1111 1111 1111 to input bits = 1111 1111 1110					2	
Settling time 6/	t_{SHL}		20 V to ±1/2 LSB	9	01		5	µs
		T_A = +25°C	20 V to ±1 LSB				4	
		Input bits = 0000 0000 0000 to input bits = 1111 1111 1111						
		1 LSB to ±1/2 LSB, T_A = +25°C Input bits = 1111 1111 1110 to input bits = 1111 1111 1111					2	
Output noise voltage 6/	NO	All inputs = 1111 1111 1111, 10 Hz ≤ 8W ≤ 100 kHz, T_A = +25°C		9			160	µV rms

1/ Unless otherwise specified, V_{CC} = 15.0 V, V_{EE} = -15.0 V, logic "0" = 0.8 V, logic "1" = 2.0 V, V_{FSR} = 10 V, and load resistance (R_L) = 2kΩ. This is a unipolar operation. Load resistor (R_L) not applicable for I_{CC} and I_{EE} test.

2/ Calculations for dV_{OS}/dT, dAE/dT, dBPOE/dT, dBZE/dT, and dV_{REF}/dT are determined from measurements made at +125°C, +25°C, and -55°C for V_{OS}, AE, BPOE, BZE, and V_{REF} respectively.

3/ The gain error of a 12 bit D/A converter in % of full scale range corresponds to gain error in LSB units by the following relationship: 0.20% x 4096 LSB/100% = 8.192 LSB.

4/ Test bipolar mode over a -10 V to +10 V range. The scale factor is V_{FSR}/4096 LSB. (i.e. For V_{FSR} = 20 V, the scale factor is 20 V/4096 LSB = 4.88 mV/LSB.)

5/ The abbreviated integral linearity error test shown for subgroups 1, 2, and 3 shall represent the minimum number of tests required. The manufacturer shall add additional tests and/or calculations to assure that the worst positive and negative error values, as determined by the abbreviated test, are within 150 milli LSB of the worst positive and negative error values, as determined by the all codes test for subgroups 7 and 8.

6/ If not tested, shall be guaranteed to the limits specified in table I herein.

Device type	01
Case outline	J
Terminal number	Terminal symbol
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12 (LSB)
13	LOGIC SUPPLY
14	V_{EE}
15	V_{OUT}
16	REF INPUT
17	BIPOLAR OFFSET
18	10 V RANGE
19	20 V RANGE
20	SUMMING JUNCTION
21	COMMON
22	V_{CC}
23	GAIN ADJUST
24	6.3 V_{REF} OUT

FIGURE 1. Terminal connections.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroup 9 shall be guaranteed, if not tested, to the limits specified in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-12-16

Approved sources of supply for SMD 83003 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
8300301JA	24355	ADDAC87D-CBI-V/883B	M38510/13702BJA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462