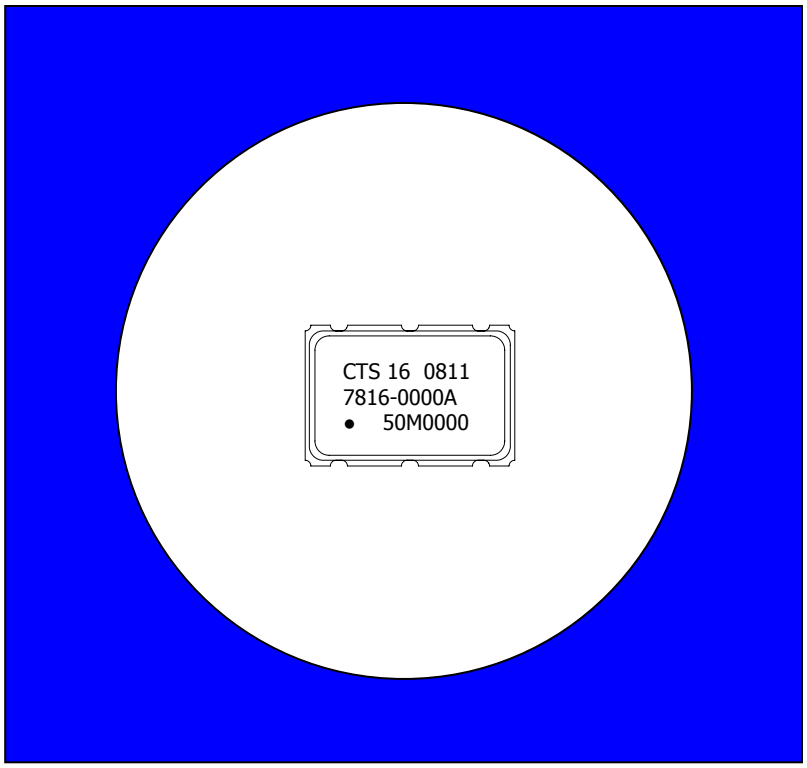
974-7816-0000A

Voltage Controlled Crystal Oscillator

FEATURES

- Standard 7x5mm Surface Mount Footprint
- HCMOS Compatible Output
- Frequency 50.0000 MHz
- **Fundamental Crystal Design**
- Frequency Stability ±25 ppm
- +3.3Vdc Operation
- Operating Temperature 0°C to +70°C
- Output Enable Standard
- Tape & Reel Packaging
- **RoHS/Green Compliant (6/6)**



DESCRIPTION

The 974-7816-0000A is a ceramic packaged Voltage Controlled Oscillator using a fundamental crystal.

ORDERING INFORMATION

CTS Part Number: 974-7816-0000A

Manufacturing Locations: 5, 12, 16

• • • CTS Electronic Components, Inc. • 171 Covington Drive • Bloomingdale, IL 60108 • • •
• • • www.ctscorp.com • • •

ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
	Maximum Control Voltage	V_C	-	-0.5	-	V_{CC}	V
	Storage Temperature	T_{STG}	-	-55	-	150	°C
	Frequency	f_O	-	-	50.0000	-	MHz
	Frequency Stability (Note 1)	$\Delta f/f_O$	V_C = +1.65V				
	0°C - 70°C			-	-	25	± ppm
	18°C - 43°C			-	-	10	
	Absolute Pull Range (Note 2)	APR	V_C = 0.3V to 3.0V	50	-	-	± ppm
	Aging	Δf	-	-	-	5	ppm/yr
	Operating Temperature	T_A	-	0	-	70	°C
Electrical and Waveform Parameters	Supply Voltage	V_{CC}	± 5 %	3.14	3.3	3.47	V
	Supply Current	I_{CC}	C_L = 50 pF	-	-	30	mA
	Output Load	C_L	-	-	-	50	pF
	Control Voltage	V_C	-	0.0	1.65	3.3	V
	Leakage Current @ V_C Input	-	-	-1	-	1.0	uA
	Setability	-	V_C for center frequency	1.25	-	2.05	V
	Pulling Sensitivity	K_V	V_C = 0.0V to 3.3V	-	50	-	ppm/V
	Linearity	L	Best Straight Line Fit	-	-	20	%
	Output Voltage Levels						
	Logic '1' Level	V_{OH}	CMOS Load	90%V_{CC}	-	-	V
	Logic '0' Level	V_{OL}	CMOS Load	-	-	10%V_{CC}	
	Output Current Levels						
	Logic '1' Level	I_{OH}	CMOS Load	-	-	-10	mA
	Logic '0' Level	I_{OL}	CMOS Load	-	-	10	
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	-	6.0	ns
	Output Duty Cycle	SYM	@ 50% Level	40	-	60	%
	Start Up Time	T_S	Application of V_{CC}	-	-	10	ms
	Input Impedance	Z_{Vc}	-	50	-	-	kOhms
	Modulation Roll-off	-	@ -3dB, V_C = 2.5V	10	-	-	kHz
	Transfer Function	-	-	-	Positive	-	-
	Phase Jitter	tjrms	Bandwidth 12 kHz - 20 MHz	-	-	1	ps RMS
	Enable Function						
	Enable Input Voltage	V_{IH}	Pin 2 Logic '1', Output Enabled	2.5	-	-	V
	Disable Input Voltage	V_{IL}	Pin 2 Logic '0', Output Disabled	-	-	0.5	
	Enable/Disable Time	T_{PLZ}	Pin 2 Logic '1'	-	-	100	ns

Notes:

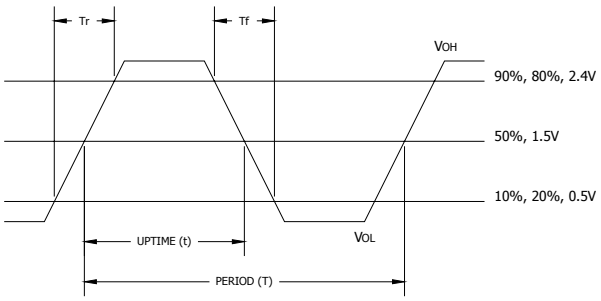
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load and operating temperature.
2. Minimum guaranteed frequency shift from f_O over variations in temperature, aging, power supply and load for 10 years.

SINGLE SIDE BAND PHASE NOISE

(Maximum)

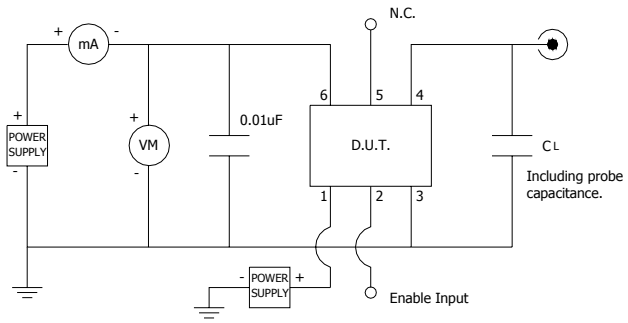
Frequency Offset	Phase Noise (dBc/Hz)
10 Hz	-
100 Hz	-
1 kHz	-
10 kHz	-110
100 kHz	-
1 MHz	-

CMOS/TTL OUTPUT WAVEFORM



DUTY CYCLE = t/T x 100 (%)

TEST CIRCUIT, CMOS LOAD



D.U.T. PIN ASSIGNMENTS

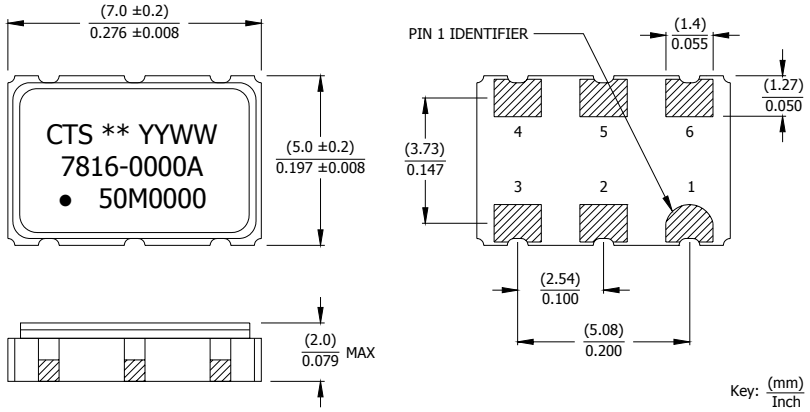
PIN	SYMBOL	DESCRIPTION
1	V_C	Control Voltage
2	EOH	Enable
3	GND	Circuit & Package Ground
4	Output	RF Output
5	N.C.	No Connect
6	V_{CC}	Supply Voltage

ENABLE TRUTH TABLE

PIN 2	PIN 4
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



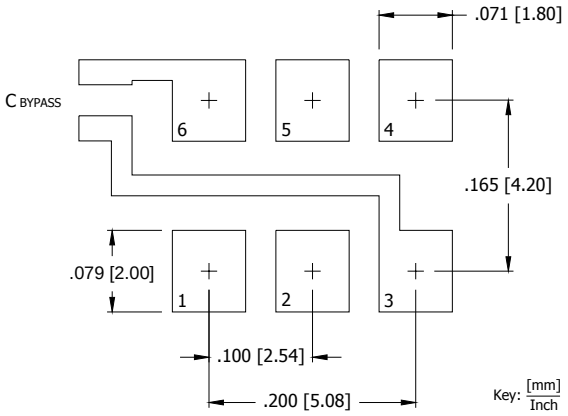
MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. YYWW – Date code, YY – year, WW – week.
3. Truncated CTS part number.
4. XXMXXXX - Frequency marked with 4 significant digits after the 'M'.

NOTES

1. Termination pads (e4), barrier-plating is nickel (Ni) with gold (Au) flash plate.
2. Reflow conditions per JEDEC J-STD-020.

SUGGESTED SOLDER PAD GEOMETRY



C_{BYPASS} should be ≥ 0.01 uF.

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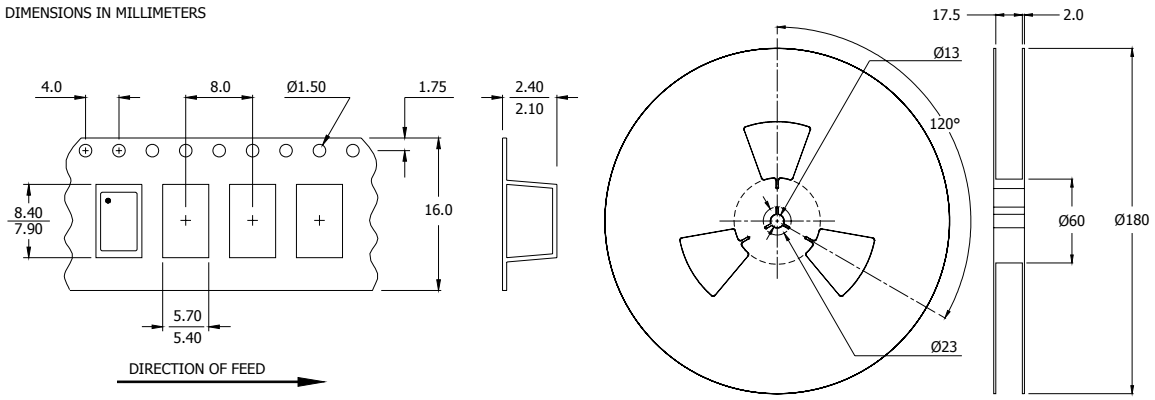
TAPE AND REEL INFORMATION



Device quantity is 1,000 pieces per 180mm reel.

ENVIRONMENTAL SPECIFICATIONS

Temperature Cycle:	400 cycles from –55°C to +125°C, 10 minute dwell at each temperature, 1 minute transfer time between temperatures.
Mechanical Shock:	1,500g's, 0.5mS duration, ½ sinewave, 3 shocks each direction along 3 mutually perpendicular planes (18 total shocks).
Sinusoidal Vibration:	0.06 inches double amplitude, 10 to 55 Hz and 20g's, 55 to 2,000 Hz, 3 cycles each in 3 mutually perpendicular planes (9 times total).
Gross Leak:	No leak shall appear while immersed in an FC40 or equivalent liquid at +125°C for 20 seconds.
Fine Leak:	Mass spectrometer leak rates less than $2x10^{-8}$ ATM cc/sec air equivalent.
Resistance to Solder Heat:	Product must survive 3 reflows of +260°C peak, 10 seconds maximum.
High Temperature Operating Bias:	2,000 hours at +125°C, maximum bias, disregarding frequency shift.
Frequency Aging:	1,000 hours at +85°C, full bias, less than ±5 ppm shift.
Moisture Sensitivity Level:	Level 1 per JEDEC J-STD-020.

QUALITY AND RELIABILITY

Quality systems meet or exceed the requirements of ISO 9000:2000 standards.