

2-22GHz LNA with AGC

GaAs Monolithic Microwave IC

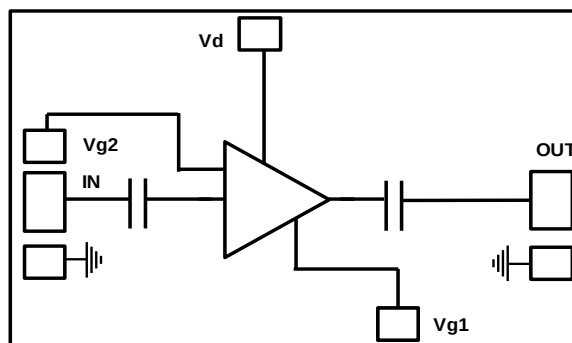
Description

The CHA3024-99F is a distributed Low Noise Amplifier with Adjustable Gain Control (AGC) which operates between 2 and 22GHz.

It is designed for a wide range of applications, such as electronic warfare, X and Ku Point to Point Radio, and test instrumentation.

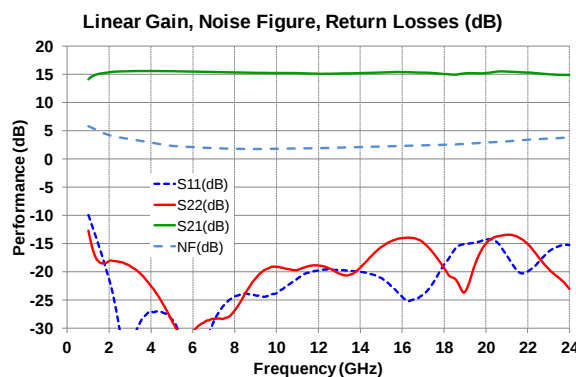
The circuit is manufactured using a 0.15 μ m gate length pHEMT process, with via holes through the substrate, air bridges and optical gate lithography.

The part is supplied as bare die and input and output RF accesses are matched to 50 ohms.



Main Features

- Broadband performances: 2-22GHz
- Typical Linear Gain: 15dB
- Up to 30 dB adjustable gain with Vg2
- P1dB: 18dBm
- Psat: 20dBm
- OIP3: 30dBm
- Typical Noise Figure: 3dB
- DC bias: Vd=5V@Id=100mA, Vg1=-0.3V and Vg2=1.7V.
- Chip dimensions: 3.04 x 1.73 x 0.1mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2		22	GHz
Gain	Linear Gain		15		dB
NF	Noise Figure		3		dB
Pout	Output Power @1dB comp.		18		dBm

Electrical Characteristics

Tamb.= +25°C, Vg1 to be set in order to have Idq=100mA, Vg2=1.7V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2		22	GHz
Gain	Linear Gain		15		dB
NF	Noise Figure		3		dB
IRL	Input Return Loss		17		dB
ORL	Output Return Loss		17		dB
P1dB	Output power for 1dB Compression		18		dBm
Psat	Saturated output power		20		dBm
OIP3	Output Third Order Intercept		30		dBm
Idq	Quiescent current on Vd		100		mA
Vd	Supply voltage on Vd	4.5	5	5.5	V
Id	Drain current @3dB gain compression		120		mA

The values are representative of typical “test fixture” measurements as defined on the drawing in paragraph “Evaluation test fixture”.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vg1	6	Gate control1 for the amplifier	-0.4	V
Vg2	2	Gate control2 for the amplifier	1.7	V
Vd	3	Drain Voltage	5	V

The associated drain current with no RF input power is Idq=100mA

This typical bias is recommended in order to get the best compromise between output power, linearity and Noise Figure performance vs. Temperature.

Absolute Maximum Ratings ⁽¹⁾T_{amb.} = +25°C

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	7V	V
I _{dq}	Drain bias current	190	mA
V _{g1}	Gate bias voltage V _{g1}	-2 to 0	V
V _{g2}	Gate bias voltage V _{g2}	1 to 2	V
P _{in}	Maximum peak input power overdrive	15	dBm
T _a	Operating temperature range (chip backside)	-40 to 85	°C
T _{stg}	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage: these maximum ratings parameters could not be cumulated.

These are stress ratings only, and functional operation of the device at these conditions is not implied.

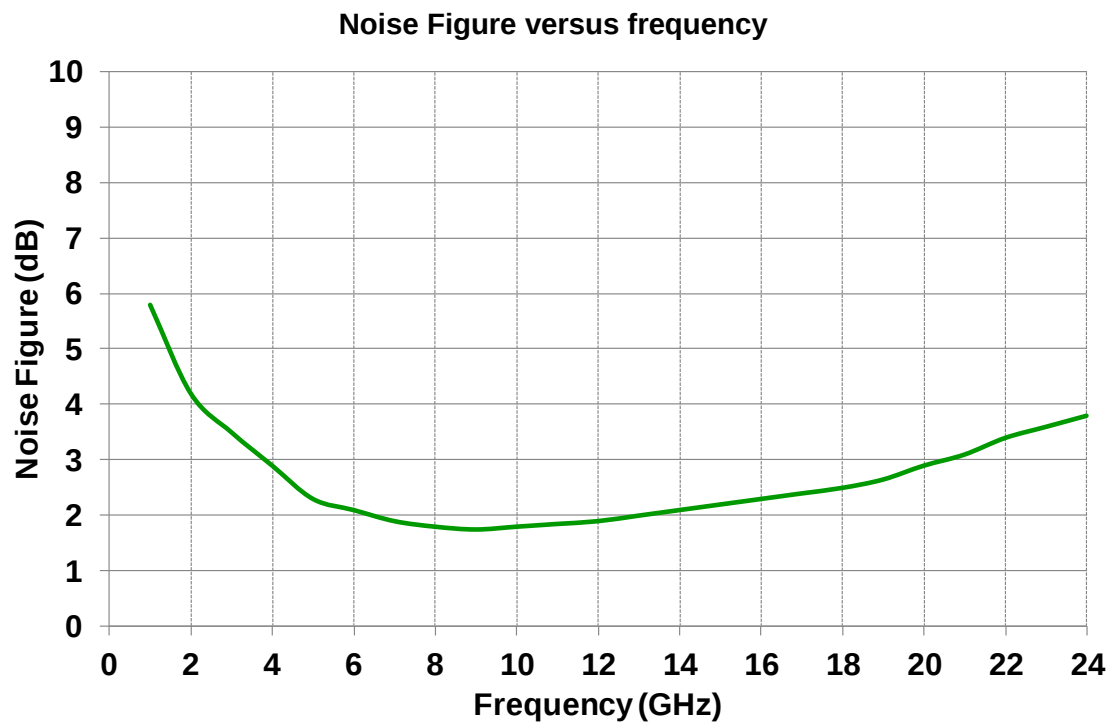
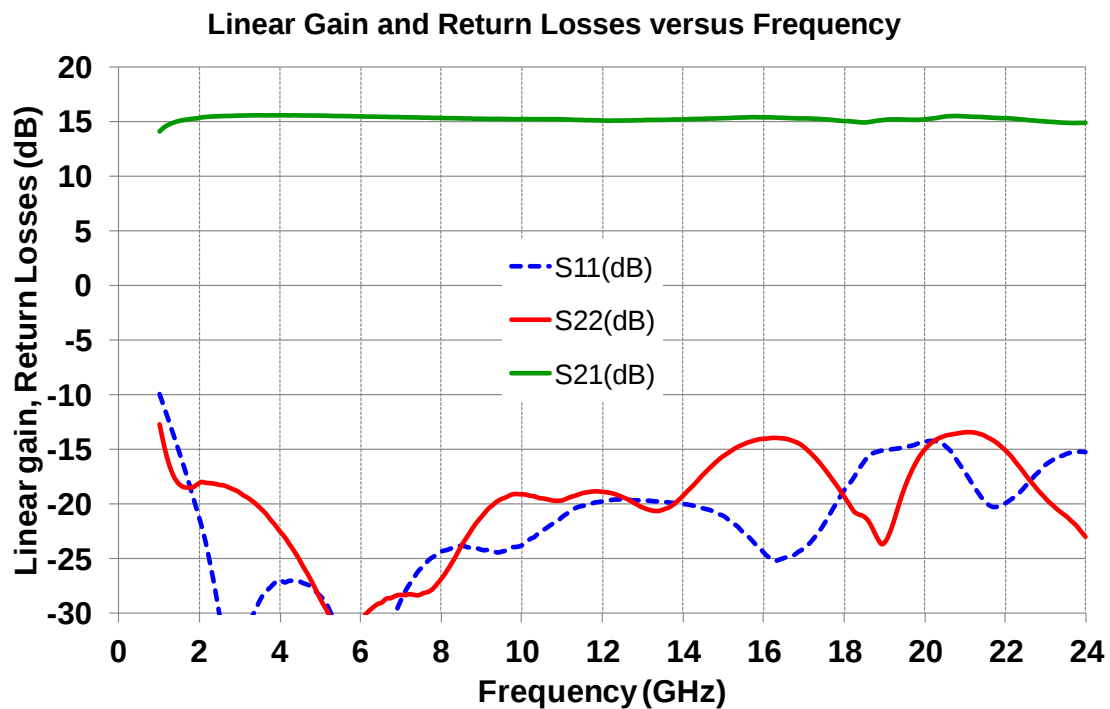
Maximum Junction temperature=115°C with T_a=+85°C.

R_{th_equivalent} = 60°C/W → chip's equivalent thermal resistance from channel to die bottom with T_a = +85°C and 5V & I_{dq}=100mA.

The R_{th_equivalent} is extrapolated, taking into account the full DC power and the channel temperature increase on the worst transistor.

Typical Jig Measurements

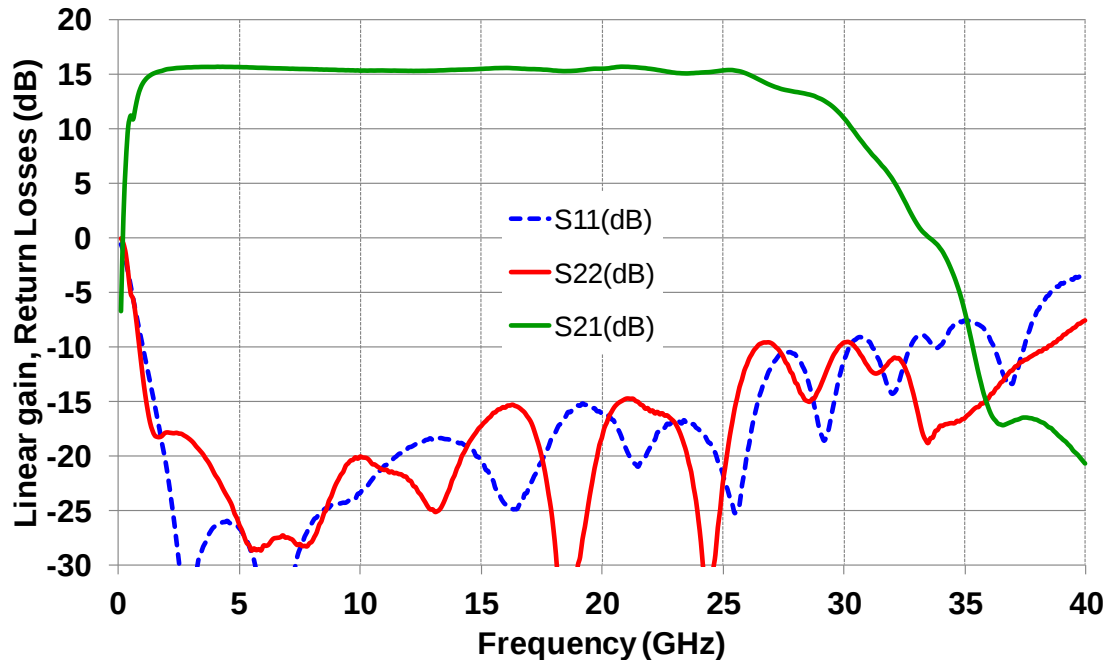
Tamb.= +25°C, Vd=5V, Vg1 set in order to get Idq =100mA, Vg2=1.7V



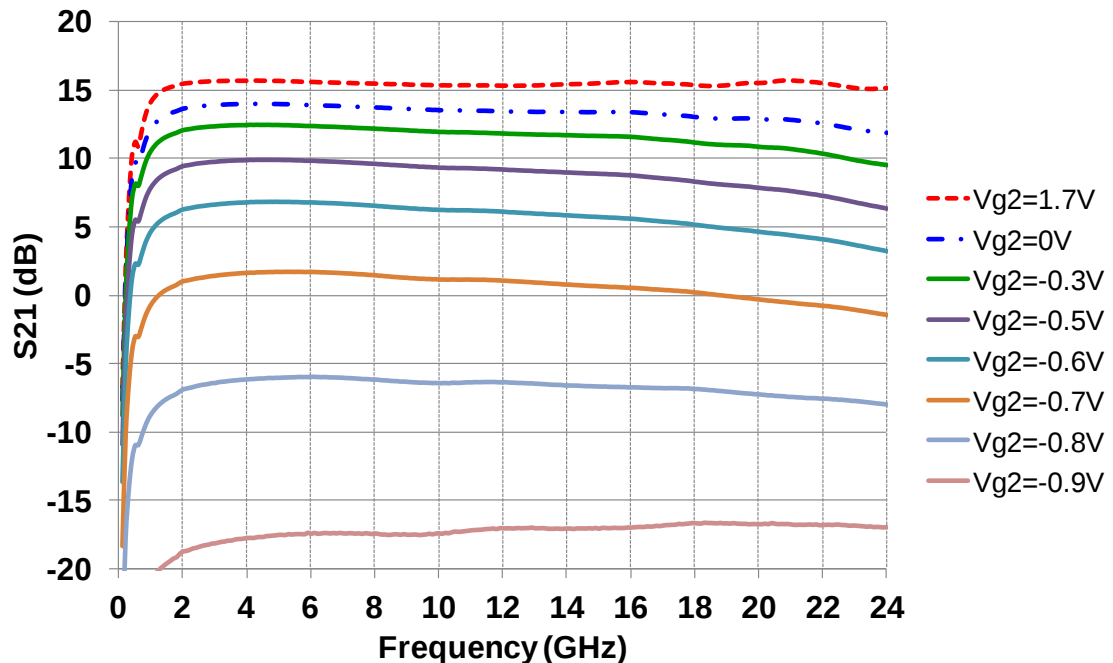
Typical Jig Measurements

Tamb.= +25°C, Vd =5V, Vg1 set in order to get Idq =100mA, Vg2=1.7V

Broadband Linear Gain and Return Losses versus Frequency

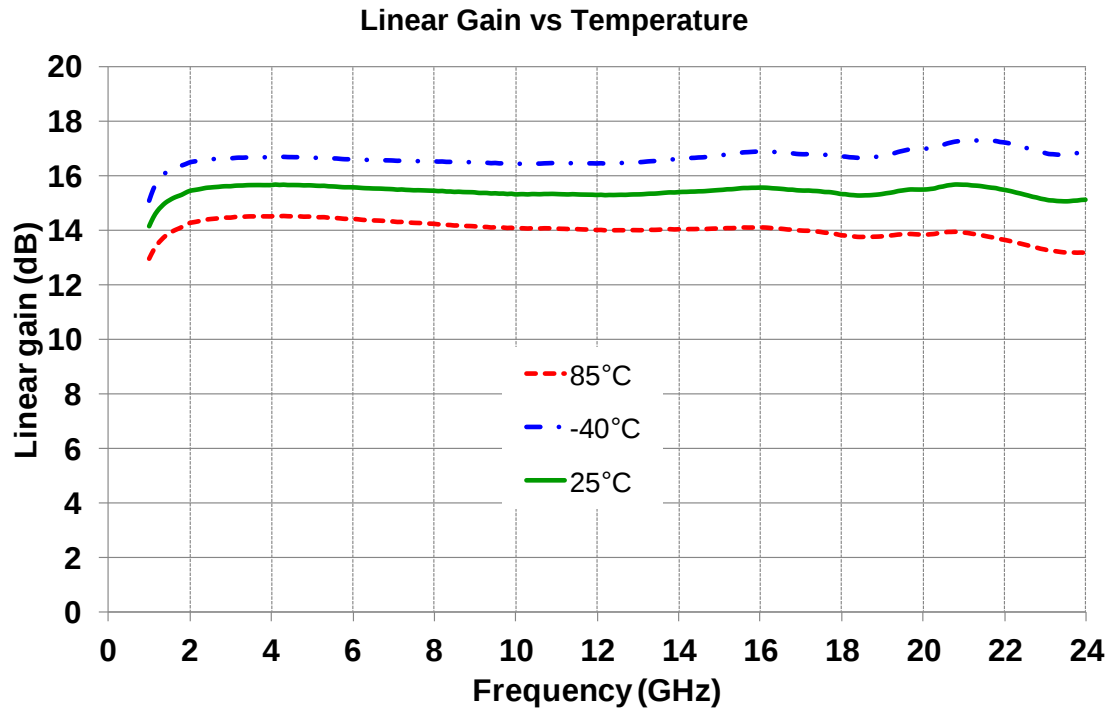


Gain tuning with Vg2 (Vd=5V and Vg1=-0.3V constant)



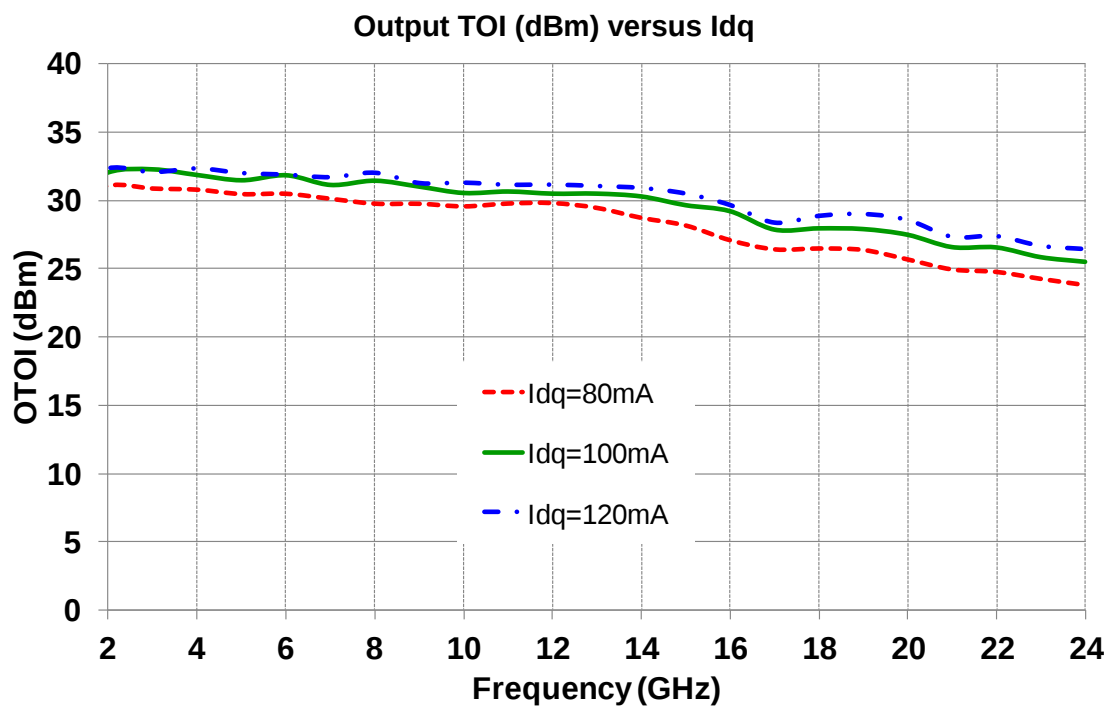
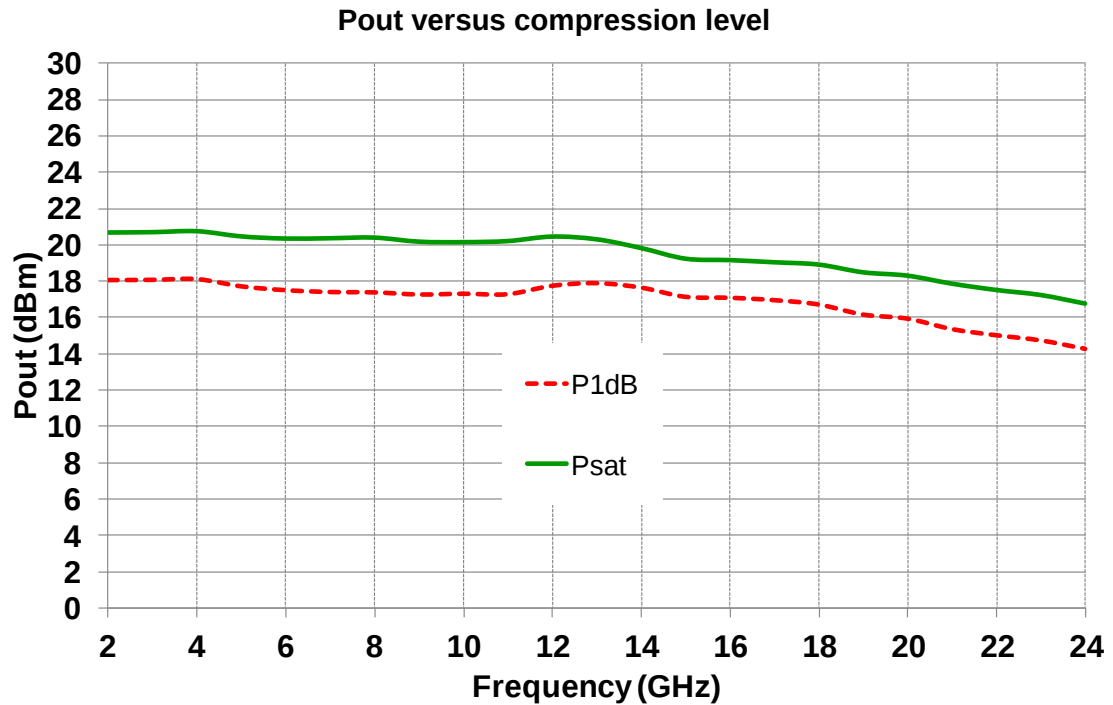
Typical Jig Measurements

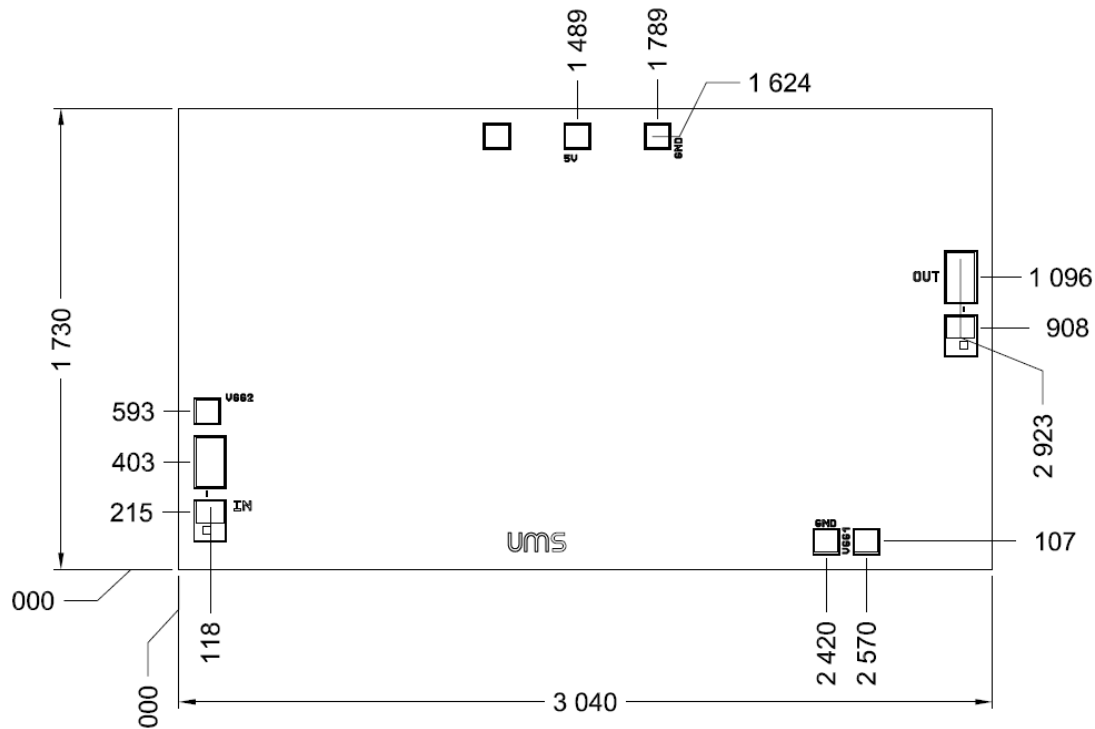
Tamb.= +25°C, +85°C, -40°C, Vd =5V, Vg1 set in order to get Idq =100mA, Vg2=1.7V
Vg1 and Vg2 remain constant versus temperature.



Typical Jig Measurements

Temperature.= +25°C, Vd =5V, Vg1 set in order to get Idq =100mA, Vg2=1.7V



Mechanical Data: outline drawing

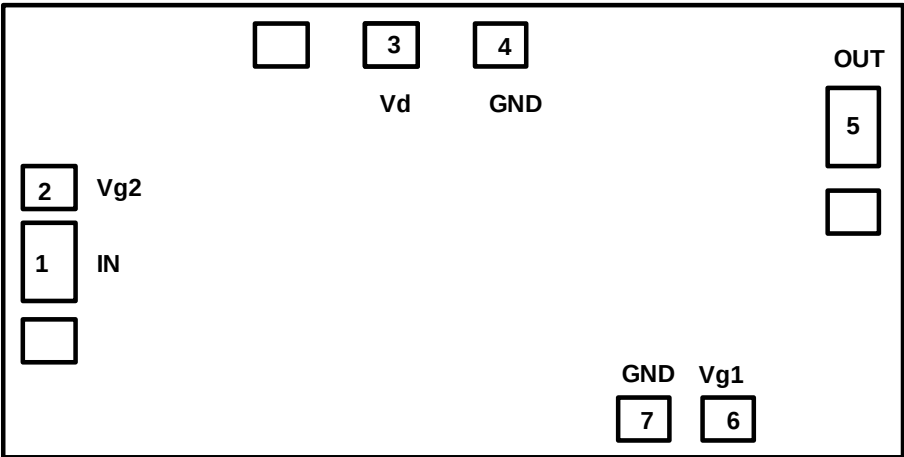
Chip size: 3040 μm x 1730 μm

Chip width and length are given with a tolerance of +/- 35μm.

Chip thickness is 100μm.

All pads are 100 μm x 100 μm, except IN and OUT pads that are 200 x 120 μm.

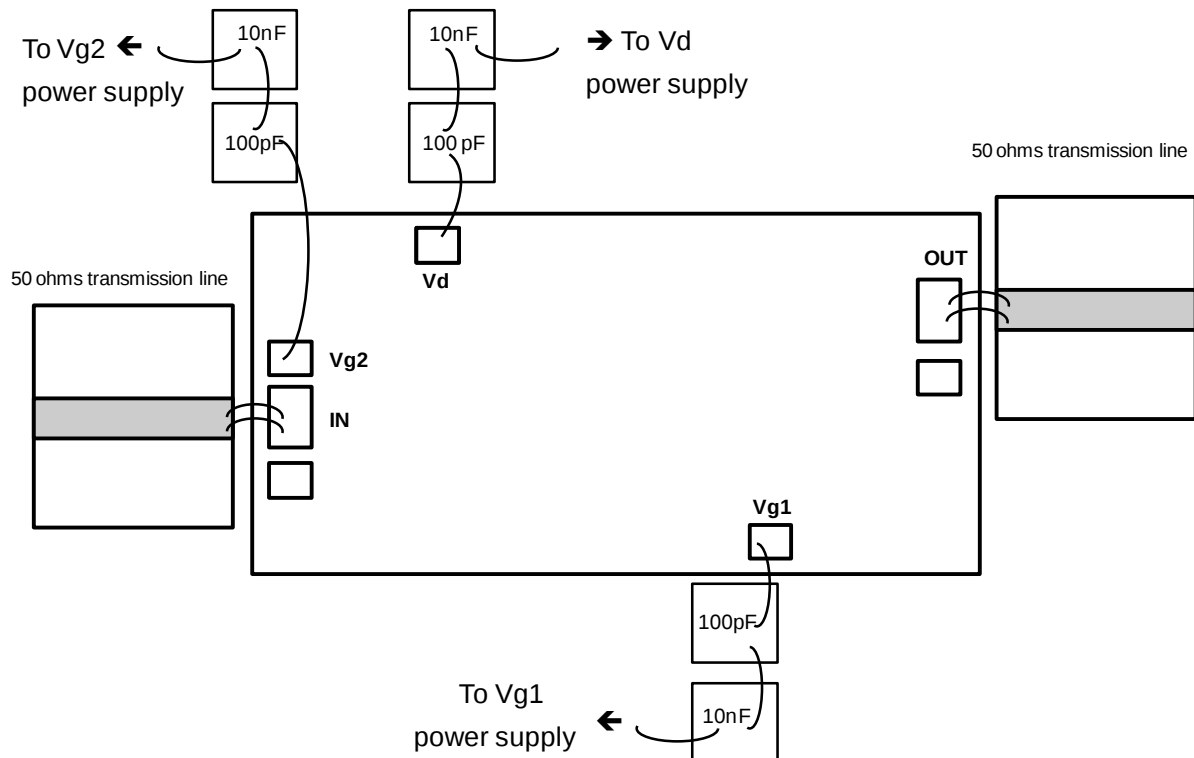
PAD Reference



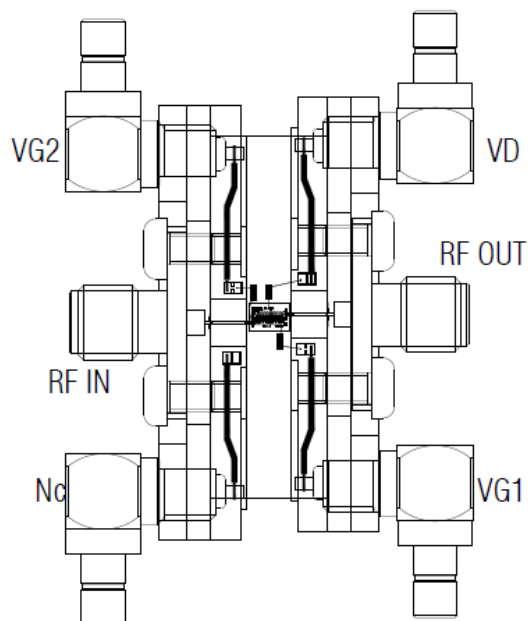
PAD Number	Name	Description
1	IN	RFIN is matched to 50 ohms
2	Vg2	Gate control 2 for amplifier: +1.7V should be applied for nominal operation.
3	Vd	Drain voltage of the part (5V)
4	GND	Not connected
5	OUT	RFOUT is matched to 50 ohms
6	Vg1	Gate control 1 for amplifier: about -0.3V for Idq=100mA
7	GND	Not connected
Die bottom	GND	Die bottom must be connected to RF/DC ground



Assembly Recommendations



Evaluation test fixture



Device Operation

Device Power Up instructions:

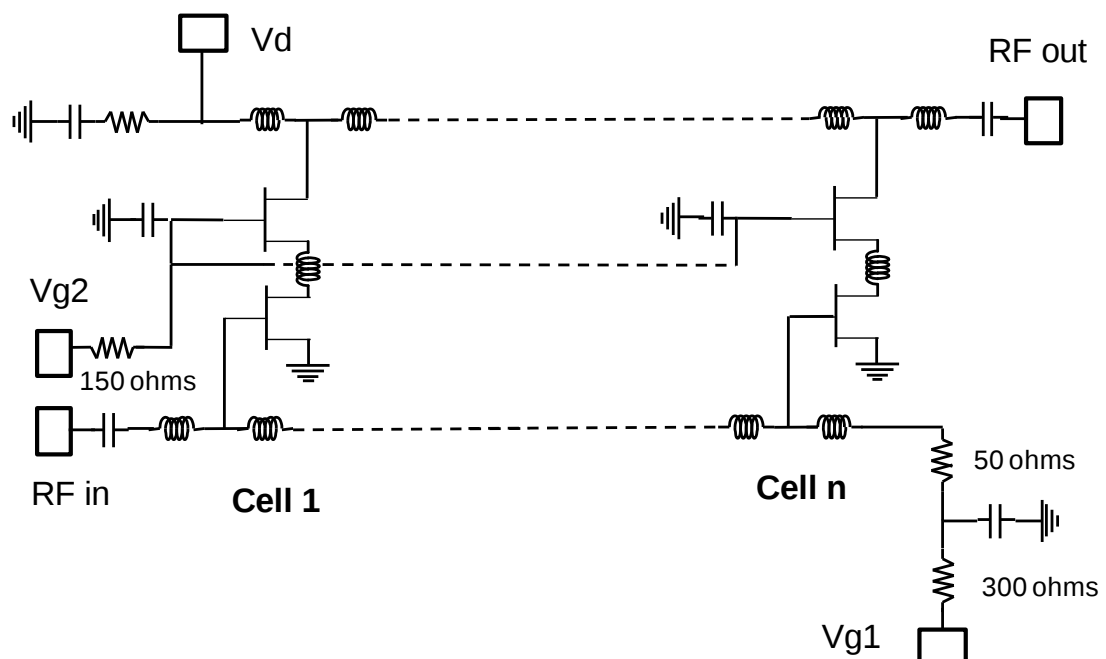
- 1) Ground the device
- 2) Set V_{g1} to -2V
- 3) Set V_{g2} to 1.7V (nominal value for V_{g2})
- 4) Set V_d to 5V (nominal value for V_d)
- 5) Set V_{g1} in the range of -0.3V for having $I_{dq}=100\text{mA}$
- 6) Apply RF input power

Device Power Down instructions:

- 1) Remove RF input power
- 2) Remove V_d
- 3) Remove V_{g2}
- 4) Remove V_{g1}

DC Schematic

$V_d=5\text{V}$, $V_{g1}=-0.3\text{V}$, $V_{g2}=1.7\text{V}$, $I_{dq}=100\text{mA}$



Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Chip form:

CHA3024-99F/00

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