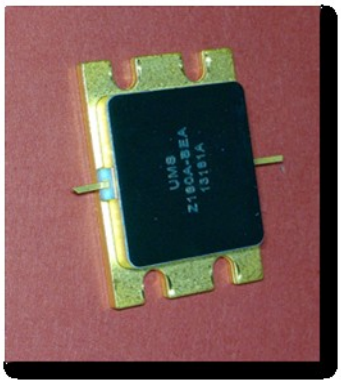
180W L-Band HPA

GaN HEMT on SiC in SEB Package

Description

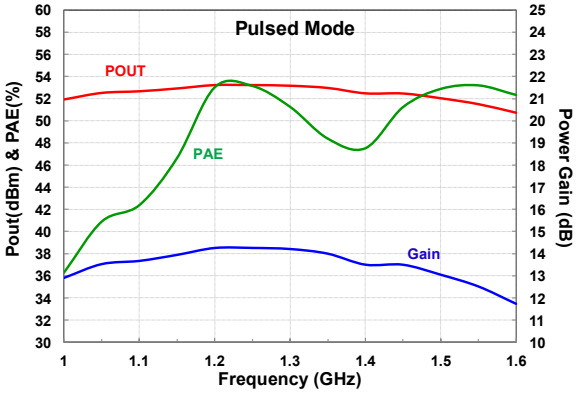
The CHZ180A-SEB is an input matched and output pre-matched packaged Gallium Nitride High Electron Mobility Transistor. It allows broadband solutions for a variety of RF power applications in L-band. It is well suited for pulsed radar application.
The CHZ180A-SEB is proposed on a 0.5µm gate length GaN HEMT process. It is based on Quasi-MMIC technology.
It is available in a hermetic flange ceramic metal power package providing low parasitic and low thermal resistance.



Main Features

- Wide band capability: 1.2 – 1.4GHz
- Pulsed operating mode
- High power : > 180W
- High PAE : up to 53%
- DC bias: V_{DS} =45V @ I_{D_Q} =1.3A
- MTTF > 10^6 hours @ Tj=200°C
- RoHS Hermetic Flange Ceramic package

V_{DS} = 45V, I_{D_Q} = 1.3A, Pin = 39dBm
Pulsed mode (100µs-10%)



Performances given at the connector access planes.

Main Electrical Characteristics

Tamb.= +25°C, Pulsed mode

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1.2		1.4	GHz
G_{SS}	Small Signal Gain		20		dB
P_{SAT}	Saturated Output Power	52	53	54	dBm
PAE_{max}	Max Power Added Efficiency	45	52		%
I_{DSAT}	Saturated Drain Current		9		A

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Recommended DC Operating Ratings

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage	20	45	50	V	
V_{GS_Q}	Gate to Source Voltage		-1.9		V	V_D=45V, I_{D_Q}=1.3A
I_{D_Q}	Quiescent Drain Current		1.3	3	A	V_D=45V
I_{D_MAX}	Drain Current in saturation		9.6	(1)	A	V_D=45V, Compressed mode
I_{G_MAX}	Gate Current (forward mode)		0	64	mA	Compressed mode
P_W	Pulse width			1.5	ms	
Dc	Duty cycle		10		%	
T_{j_MAX}	Junction temperature			200	°C	

(1) Limited by dissipated power

DC Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-3	-2	-1	V	V_D=45V, I_D=I_{DSS}/100
I_{D_SAT}(2)	Saturated Drain Current		30		A	V_D=7V, V_G=2V, (1)
I_{G_leak}	Gate Leakage Current (reverse mode)	-10			mA	V_D=45V, V_G=-7V, (1)
V_{BDS}	Drain-Source Break-down Voltage		200		V	V_G=-7V, (1)
R_{TH}	Thermal Resistance		0.75		°C/W	1ms – 10%

(1) Parameters extrapolated from unit cell measurement
(2) For information, limited by I_{D_MAX}, see on Absolute Maximum Ratings

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RF Characteristics(1)

Tcase= +25°C, pulsed mode(2), on board 61501354 , V_{DS}=45V, I_{D_Q}=1.3A

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1.2		1.4	GHz
G_{SS}	Small Signal Gain	17.5	20	22	dB
P_{SAT}	Saturated Output Power	51.5	53	54.5	dBm
PAE	Max Power Added Efficiency	45	52		%
G_{PAE_MAX}	Associated Gain at Max PAE		13.5		dB
I_{DSAT}	Saturated Drain Current		9	10	A
S_{11}	Input return loss		-12.5	-11	dB

(1) Measured on evaluation board 61501354 on the connector access planes.
(2) Input RF and gate voltage are pulsed. Conditions are 1.5ms width, 10% duty cycle and 1µs offset between RF and DC pulse.

Absolute Maximum Ratings

Tcase= +25°C (1), (2), (3)

Symbol	Parameter	Rating	Unit	Note
V_{DS}	Drain-Source Voltage	-0.5, +60	V	
V_{GS_Q}	Gate-Source Voltage	-10, +2	V	(4),(6)
I_{G_MAX}	Maximum Gate Current in forward mode	190	mA	
I_{G_MIN}	Maximum Gate Current in reverse mode	-25	mA	
I_{D_MAX}	Maximum Drain Current	16	A	(4)
P_{IN}	Maximum Input Power	44	dBm	(5)
P_{W_MAX}	Pulse width	3	ms	
D_{C_MAX}	Duty cycle	20	%	
Top	Operating temperature range	-40 to +85	°C	
T_j	Junction Temperature	220	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.
(3) The given values have not to be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.
(4) Max junction temperature has to be considered
(5) Linked to and limited by I_{G_MAX} & I_{G_MIN} values
(6) V_{GS_Q} max limited by I_{D_MAX} and I_{G_MAX} values

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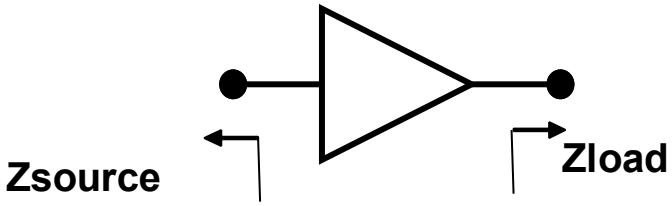
Simulated Source and Load Impedance

V_{DS} = 45V, I_{D_Q} = 1.3A



Frequency (GHz)	Source	Load
Typical [1.2-1.4]	50 - j0	16 - j20

These values are given in the reference plane defined by the connection between the package leads and the PCB. A gap of 200µm is considered between the edge of the package and the PCB.

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Typical Package Sij parameters (simulation)

Tamb.= +25°C, V_{DS}=45V, I_{D_Q}=1.3A

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
0	-0.47	0.0	47.51	180.0	-77.02	0.0	-18.39	-180.0
0.1	-1.49	172.7	22.04	49.6	-51.30	-40.2	-3.16	-166.6
0.2	-1.40	152.2	14.35	15.0	-52.98	-74.3	-1.61	-173.3
0.3	-1.45	132.6	9.82	-10.9	-53.99	-99.8	-0.96	178.9
0.4	-1.62	111.6	7.26	-33.5	-54.06	-122.0	-0.67	171.8
0.5	-1.90	87.7	6.18	-55.7	-53.21	-143.9	-0.53	165.1
0.6	-2.30	59.2	6.33	-79.4	-51.49	-167.2	-0.47	158.4
0.7	-2.83	24.0	7.54	-106.3	-48.96	166.2	-0.46	151.3
0.8	-3.46	-19.9	9.66	-138.0	-45.71	135.0	-0.50	143.1
0.9	-4.23	-73.2	12.58	-175.8	-41.78	97.6	-0.67	132.6
1	-5.73	-137.8	16.37	137.3	-37.10	51.0	-1.31	116.5
1.1	-11.31	122.4	20.60	71.8	-32.08	-14.2	-4.67	86.6
1.2	-10.89	-71.2	21.50	-14.7	-30.45	-100.3	-18.34	-173.0
1.3	-11.29	-156.4	18.87	-88.2	-32.42	-173.3	-5.28	174.8
1.4	-26.06	167.0	16.21	-149.7	-34.48	125.5	-2.92	156.8
1.5	-13.52	-79.2	13.85	152.4	-36.28	68.1	-2.31	141.0
1.6	-7.27	-109.9	11.70	95.6	-37.92	11.6	-2.78	126.5
1.7	-4.44	-138.7	9.83	38.5	-39.31	-45.1	-3.92	113.8
1.8	-3.19	-164.7	8.67	-23.2	-40.02	-106.4	-5.57	95.2
1.9	-2.82	173.9	7.50	-105.4	-40.77	171.8	-11.23	22.9
2	-2.17	154.2	0.27	159.7	-47.62	77.3	-5.67	-132.4
2.1	-2.01	131.0	-10.00	97.9	-57.52	15.9	-2.29	-172.6
2.2	-2.25	106.7	-19.45	55.4	-66.64	-26.2	-1.20	168.2
2.3	-2.73	79.9	-28.06	22.4	-74.93	-58.7	-0.77	155.6
2.4	-3.37	48.8	-35.84	-5.2	-82.41	-86.0	-0.58	147.4
2.5	-3.95	12.6	-43.78	-30.8	-90.07	-111.1	-0.40	139.9
2.6	-4.12	-26.8	-52.16	-50.5	-98.18	-130.4	-0.32	133.6
2.7	-3.75	-64.4	-61.62	-57.7	-107.40	-137.2	-0.29	128.0
2.8	-3.10	-96.5	-70.36	-28.1	-115.90	-107.2	-0.27	122.9
2.9	-2.47	-122.3	-70.64	4.2	-116.00	-74.4	-0.26	118.2
3	-1.96	-143.1	-70.13	4.6	-115.30	-73.5	-0.26	113.7
3.1	-1.58	-160.1	-70.49	-2.9	-115.40	-80.5	-0.27	109.3
3.2	-1.31	-174.3	-71.17	-12.1	-115.90	-89.3	-0.27	105.0
3.3	-1.11	173.5	-71.84	-21.5	-116.50	-98.2	-0.29	100.6
3.4	-0.97	162.9	-72.33	-30.9	-116.80	-107.1	-0.31	96.1
3.5	-0.86	153.3	-72.47	-40.3	-116.80	-116.0	-0.35	91.3
3.6	-0.78	144.7	-72.13	-50.0	-116.30	-125.1	-0.41	86.0
3.7	-0.71	136.7	-71.14	-60.7	-115.20	-135.3	-0.53	79.5
3.8	-0.67	129.3	-69.16	-74.3	-113.10	-148.4	-0.85	70.3
3.9	-0.63	122.3	-65.70	-97.0	-109.60	-170.6	-2.17	53.7
4	-0.60	115.7	-62.17	-151.7	-106.00	135.3	-16.09	53.3

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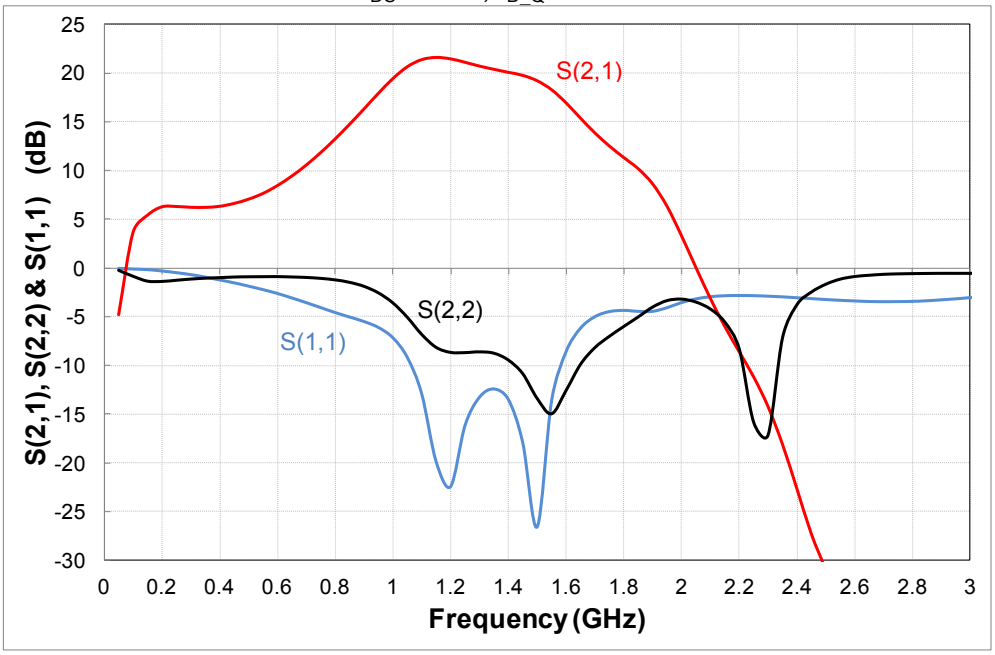
Typical Performance on Evaluation Board (Ref. 61501354)

Measured on the connector access planes.

Tcase = +25°C, Pulsed mode [1]

S Parameters

V_{DS} = 45V, I_{D_Q} = 1.3A



[1] Input RF and gate voltage are pulsed. Conditions are 100µs width, 10% duty cycle and 1µs offset between DC and RF pulse

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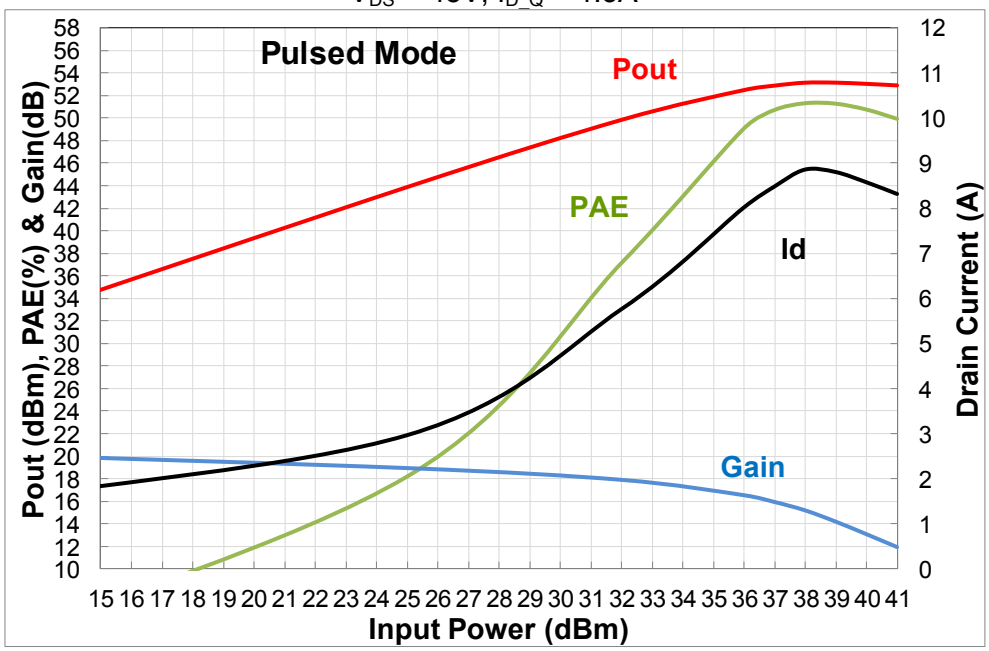
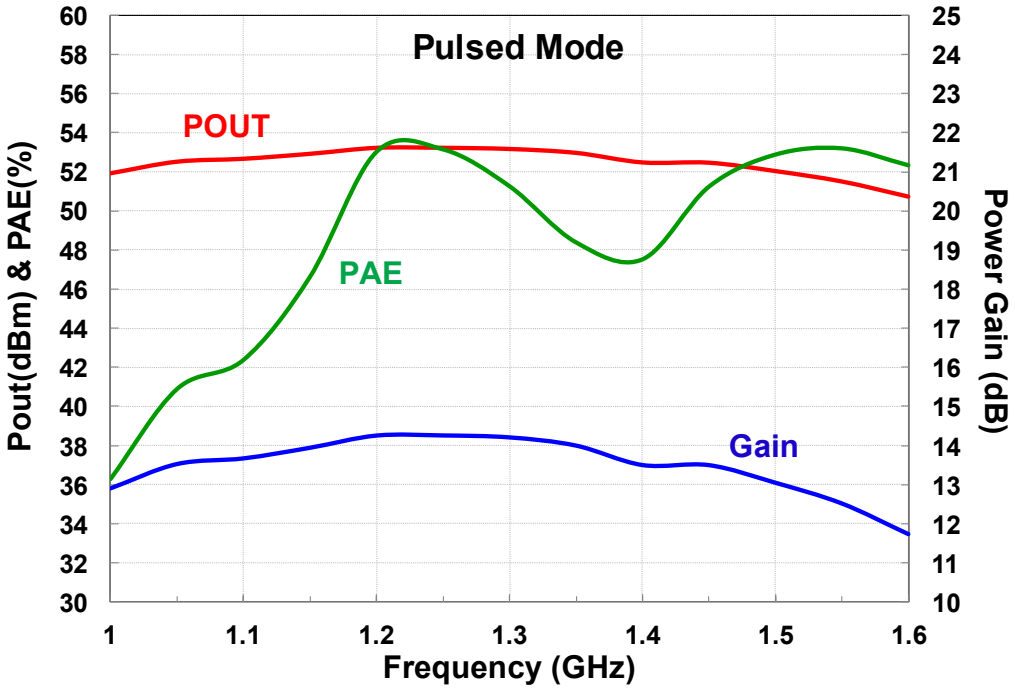
Typical Performance on Evaluation Board (Ref. 61501354)

Tcase = +25°C, Pulsed mode [1]. Measured on the connector access planes.

Pout, Gain, PAE & Id @1.3GHz
V_{DS} = 45V, I_{D_Q} = 1.3A



Pout, PAE & Gain @39dBm
V_{DS} = 45V, I_{D_Q} = 1.3A



[1] Input RF and gate voltage are pulsed. Conditions are 100µs width, 10% duty cycle and 1µs offset between DC and RF pulse.

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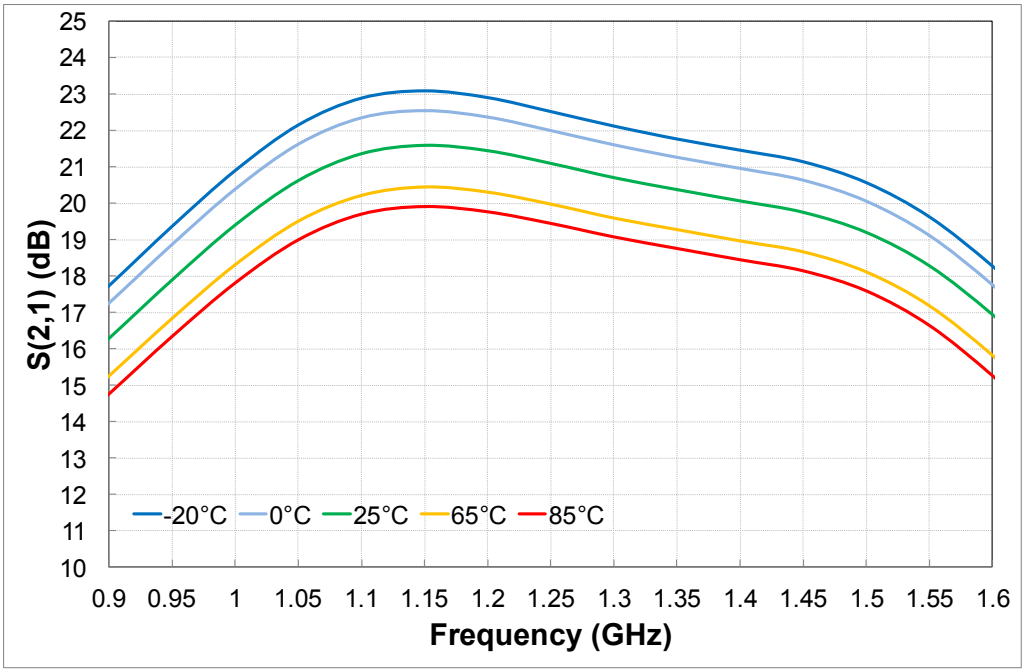
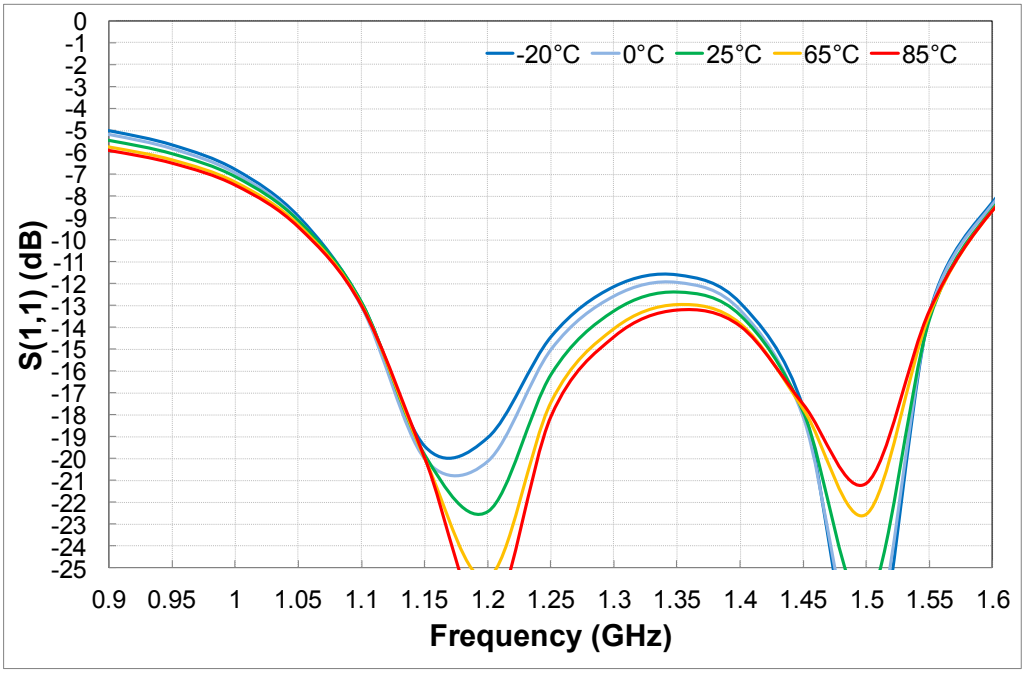
Typical Performance in Temperature (on evaluation board)

Measured on the connector access planes. (Board ref 61501354).
Tamb.= -20°C, +0°C, +25°C, +65°C & +85°C
Pulsed mode [1], V_{DS}=45V, I_{D_Q}=1.3A (fixed @+25°C)

Linear Gain versus temperature



Input Return Loss versus temperature



[1] Input RF and gate voltage are pulsed. Conditions are 100µs width, 10% duty cycle and 1µs offset between DC and RF pulse.

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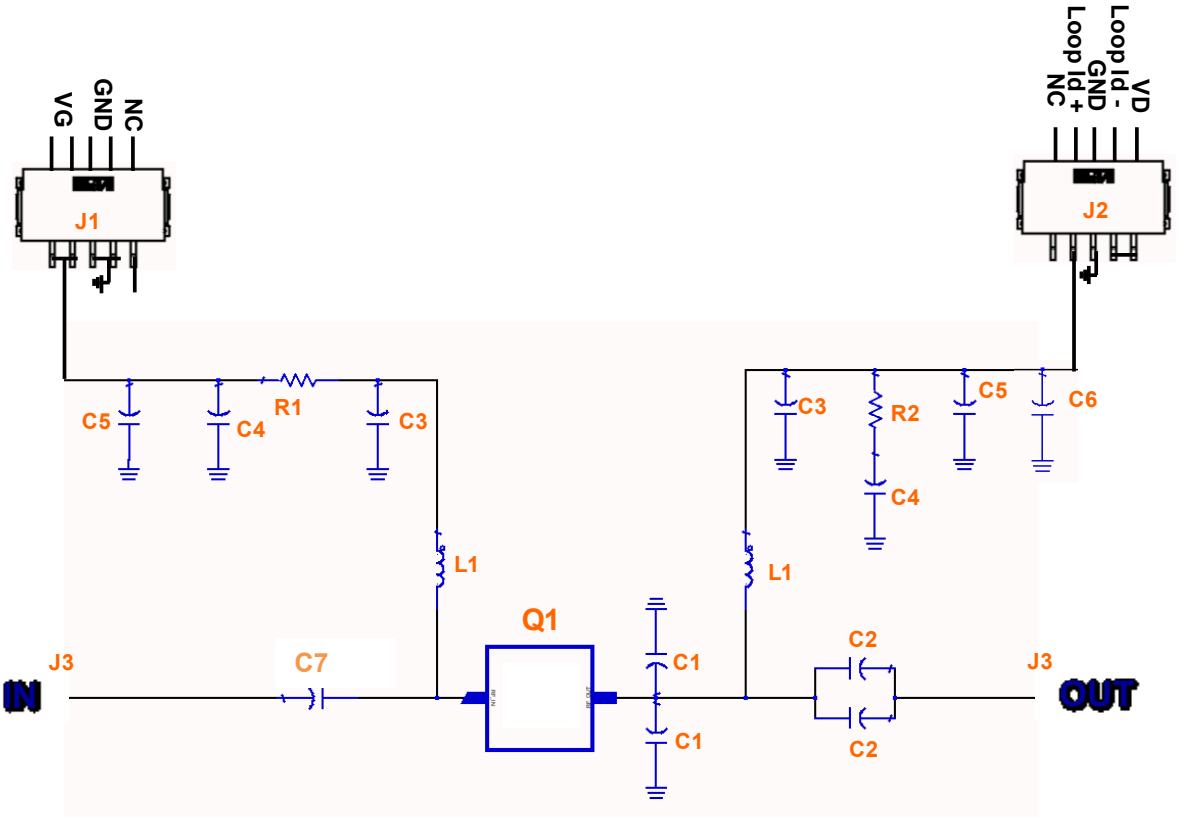
Demonstration Amplifier Low Frequency Equivalent Schematic (Ref. 61501354)



Demonstration Amplifier (Ref. 61501354) / Bill of Materials

Designator	Type	Value - Description	Qty
C1	Capacitor	1.5pF, +/- 0.1pF, 0603	2
C2	Capacitor	8.2pF, +/- 5%, 0603	2
C3	Capacitor	100pF, +/- 5%, 0603	2
C4	Capacitor	1nF, +/- 5%, 0805	2
C5	Capacitor	1µF, +/- 10%, 1812	2
C6	Capacitor	68µF, +/- 20%, H13	1
C7	Capacitor	10pF, +/- 5%, 0603	1
L1	Inductor	Air Inductor 22nH +/-5.2%	2
R1	Resistor	20Ω, +/- 1%, 0603	1
R2	Resistor	3Ω, +/- 1%, 0603	1
J1, J2	Connector	SMD 5 contacts	2
J3	Connector	N	2
Q1	HPA	CHZ180A-SEB	1
-	PCB	RO4003, Er=3.55, h=508µm	-

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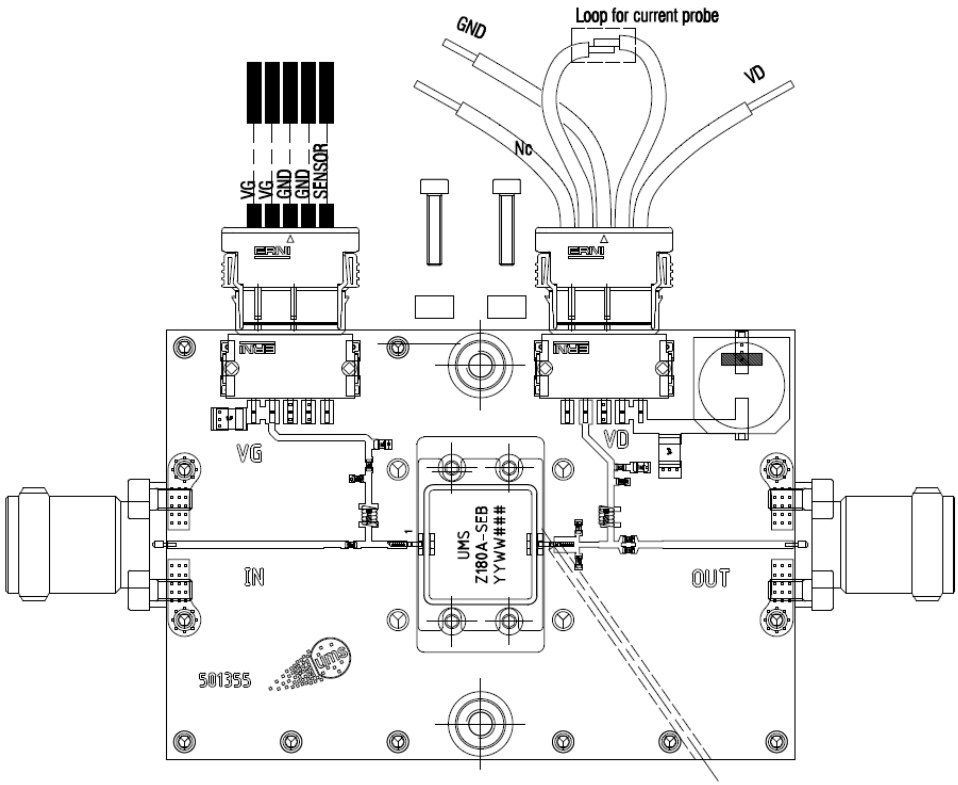
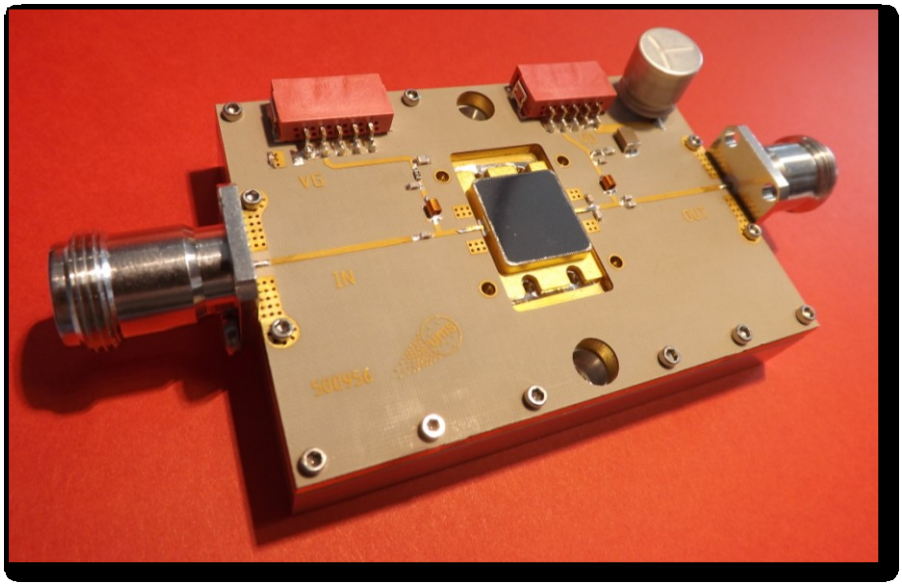
Amplifier Evaluation Board (Ref. 61501354)



Amplifier Evaluation Board



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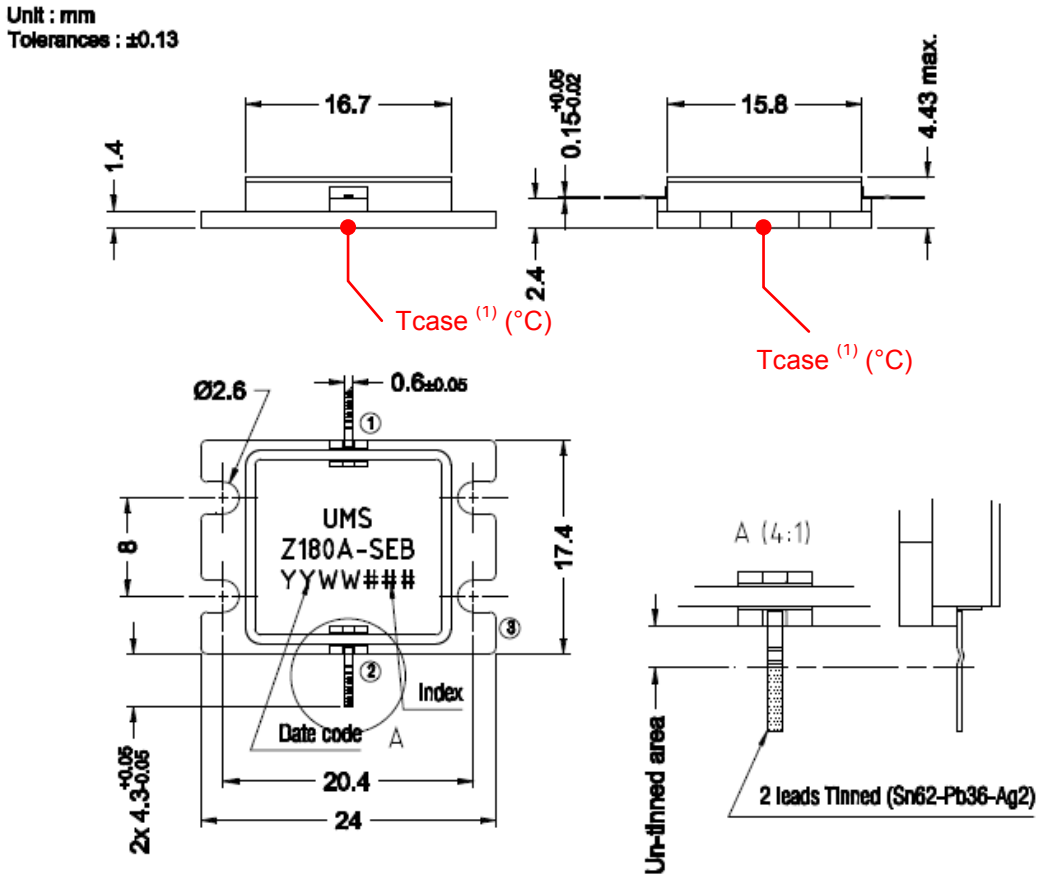
Package outline



PIN-OUT
1- RFIN+DC Gate voltage
2- RFOUT+DC Drain voltage
3- GND

(1) Tcase locates the reference point used to monitor the device temperature. This point has been taken at the device / system interface to ease system thermal design.
Chamfered lead indicates the gate access of the amplifier.

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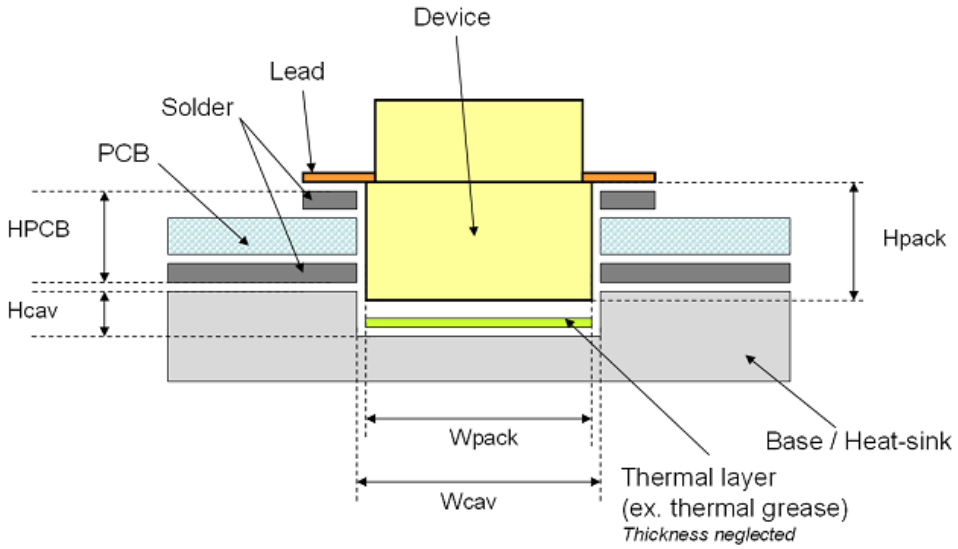
Recommended Assembly Procedure

CHZ180A-SEB is available as a flange package to be bolted down onto a thermal heat sink also used as main electrical ground. Use preferably screw M2 and flat washers.
Thermal and electrical resistance at the package to heat sink interface has to be as low as possible. Thermal electrically conductive grease or conductive thin layer like indium sheets are recommended between the package and the heat sink.
In case a thermal grease is selected, we recommend to use material offering thermal conductivity >5W/m.K and electrical resistivity <0.01 ohm.cm. The grease layer thickness should be about 25µm (1 mil).
Contact interface quality can be improved by cleaning process prior device mounting on the heat-sink. Such operation will enhance the thermal and electrical contact by oxide removal at each interface.
Package leads can be soldered on printed circuit board traces by using RoHS solder past.
Cavity depth and width to be performed into the heat-sink where the device will be mounted are important to achieve the best performances. These dimensions have to be optimized in order to minimize the distance between device and signal traces made on the printed circuit board (PCB). But they also have to be calculated in order to accommodate device variations in height. The following drawing gives the relationship between device dimensions (Hpack & Wpack) and optimal cavity depth (Hcav) and width (Wcav) depending on the printed circuit-board configuration (HPCB)



$Hcav = (Hpack_{min} - HPCB_{max})^{+0}{}_{/- 0.05}$
$Wcav = (Wpack_{max} + 0.4)_{+/- 0.05}$

dimensions are in mm

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Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Package :	CHZ180A-SEB/XY Tray: XY = 26

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