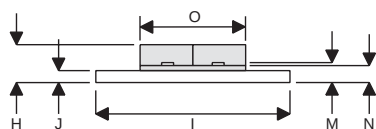
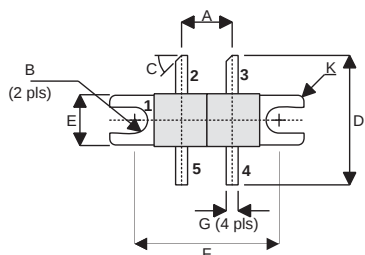


MECHANICAL DATA



DK

PIN 1 SOURCE (COMMON) PIN 2 DRAIN 1
PIN 3 DRAIN 2 PIN 4 GATE 2
PIN 5 GATE 1

DIM	mm	Tol.	Inches	Tol.
A	6.45	0.13	0.254	0.005
B	1.65R	0.13	0.065R	0.005
C	45°	5°	45°	5°
D	16.51	0.76	0.650	0.03
E	6.47	0.13	0.255	0.005
F	18.41	0.13	0.725	0.005
G	1.52	0.13	0.060	0.005
H	4.82	0.25	0.190	0.010
I	24.76	0.13	0.975	0.005
J	1.52	0.13	0.060	0.005
K	0.81R	0.13	0.032R	0.005
M	0.13	0.02	0.005	0.001
N	2.16	0.13	0.085	0.005

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 80W – 28V – 500MHz PUSH-PULL

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW C_{rss}
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 13 dB MINIMUM

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from 1 MHz to 500 MHz

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	175W
BV_{DSS}	Drain – Source Breakdown Voltage *	70V
BV_{GSS}	Gate – Source Breakdown Voltage *	$\pm 20V$
$I_{D(sat)}$	Drain Current *	10A
T_{stg}	Storage Temperature	-65 to $150^{\circ}C$
T_j	Maximum Operating Junction Temperature	$200^{\circ}C$

* Per Side

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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PER SIDE					
BV _{DSS} Drain-Source Breakdown Voltage	V _{GS} = 0 I _D = 100mA	70			V
I _{DSS} Zero Gate Voltage Drain Current	V _{DS} = 28V V _{GS} = 0			2	mA
I _{GSS} Gate Leakage Current	V _{GS} = 20V V _{DS} = 0			1	μA
V _{GS(th)} Gate Threshold Voltage *	I _D = 10mA V _{DS} = V _{GS}	1		7	V
g _{fs} Forward Transconductance *	V _{DS} = 10V I _D = 2A	1.6			S
TOTAL DEVICE					
G _{PS} Common Source Power Gain	P _O = 80W	13			dB
η Drain Efficiency	V _{DS} = 28V I _{DQ} = 0.4A	50			%
VSWR Load Mismatch Tolerance	f = 400MHz	20:1			—
PER SIDE					
C _{iss} Input Capacitance	V _{DS} = 28V V _{GS} = -5V f = 1MHz			120	pF
C _{oss} Output Capacitance	V _{DS} = 28V V _{GS} = 0 f = 1MHz			60	pF
C _{rss} Reverse Transfer Capacitance	V _{DS} = 28V V _{GS} = 0 f = 1MHz			5	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

R _{THj-case}	Thermal Resistance Junction – Case	Max. 1.0°C / W
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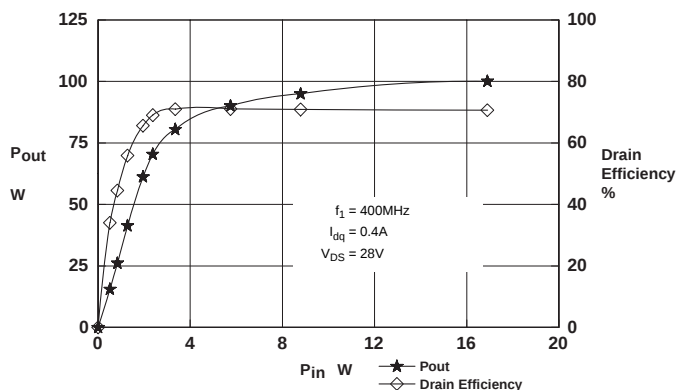


Figure 1 – Power Output and Efficiency vs. Power Input.

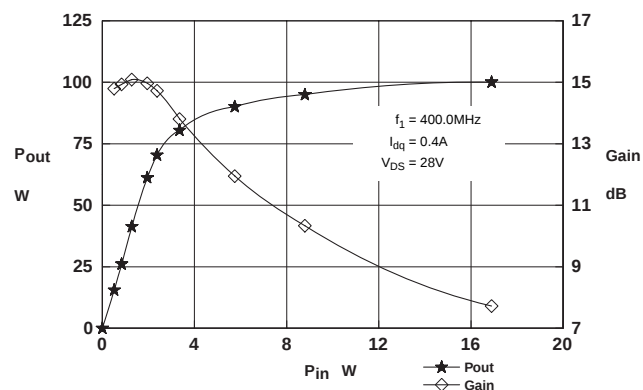


Figure 2 – Power Output & Gain vs. Power Input.

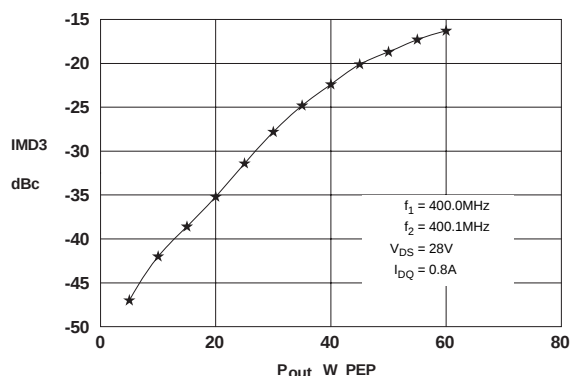


Figure 3 – IMD vs. Output Power.

D1008UK OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
400	$1.5 + j0.2$	$5.0 + j2.0$

Typical S Parameters

! Vds=28V, Idq=1A
MHz S MA R 50

!Freq MHz	S11 mag	ang	S21 mag	ang	S12 mag	ang	S22 mag	ang
100	0.794	-158	14.622	69	0.0115	-7	0.61	-145
200	0.881	-167	5.821	42	0.0061	3	0.794	-156
300	0.923	-171	3.02	28	0.0068	60	0.871	-162
400	0.923	-176	1.82	18	0.117	77	0.902	-167
500	0.937	-179	1.439	15	0.0168	76	0.923	-169
600	0.952	177	1.057	13	0.0234	75	0.945	-171
700	0.966	174	0.676	10	0.0285	74	0.966	-174
800	0.966	171	0.543	5	0.0335	69	0.955	-177
900	0.977	167	0.447	1	0.0394	64	0.966	178
1000	0.966	165	0.359	1	0.0432	64	0.955	178

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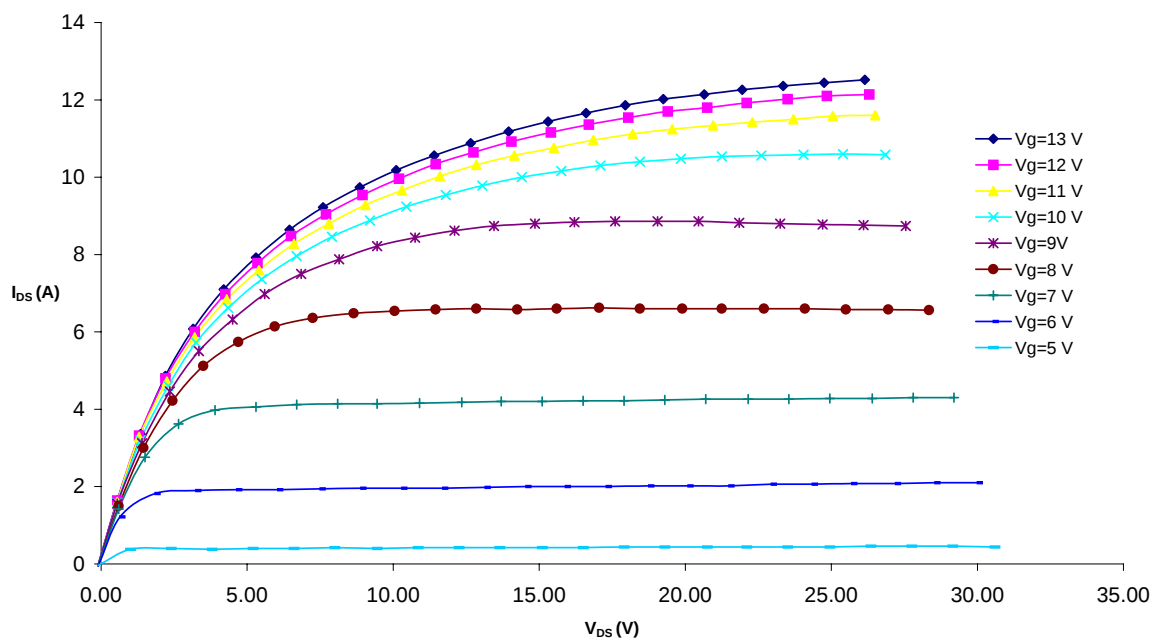


Figure 4 – Typical IV Characteristics.

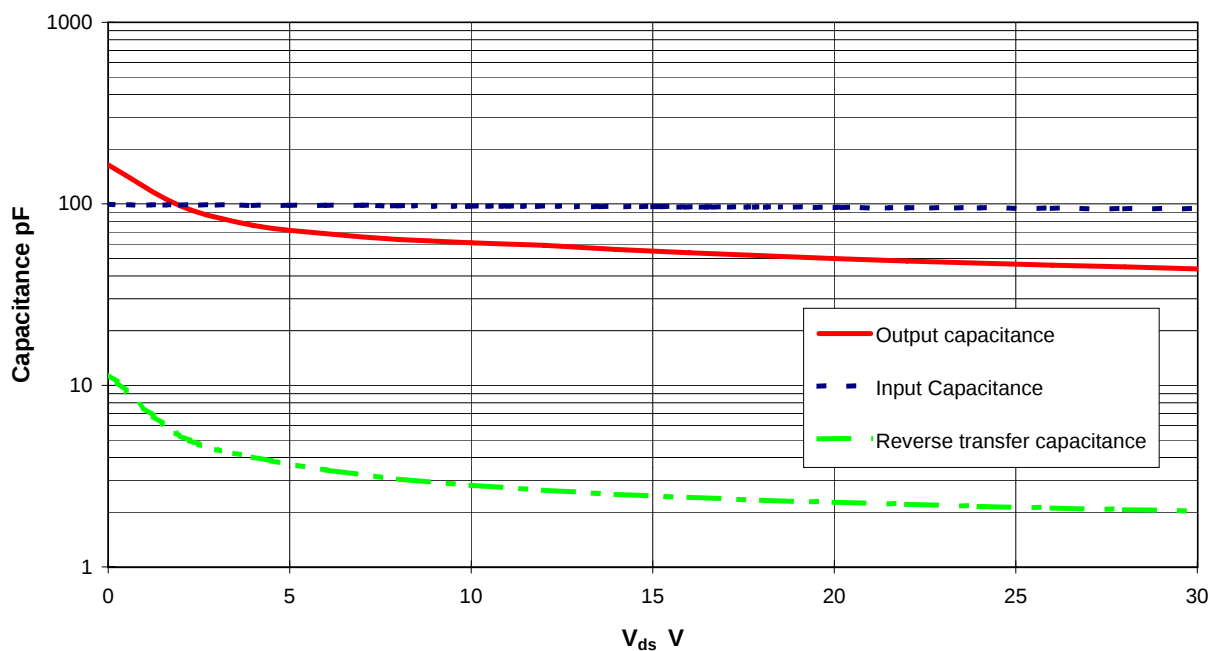
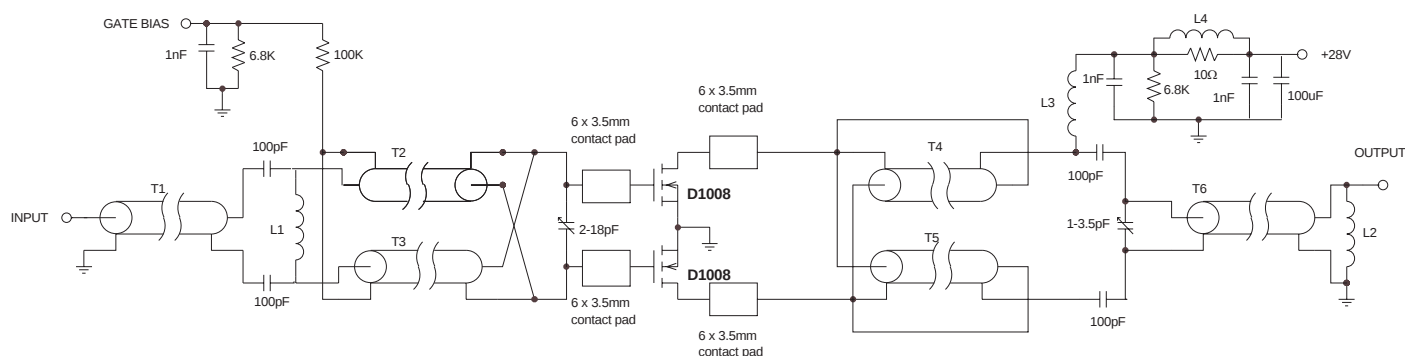


Figure 5 – Typical CV Characteristics.



D1008UK TEST FIXTURE

Substrate 1.6mm PTFE/glass, Er=2.5
All microstrip lines W=4.4mm

T1	70mm	50Ω UT34 SEMI RIGID COAX	L1	3.5 turns of 24swg ECW, 3mm ID
T2,T3	85mm	25Ω UT70-25 SEMI RIGID COAX	L2	5.5 turns of 24swg ECW, 4mm ID
T4,T5	100mm	15Ω UT85-15 SEMI RIGID COAX	L3	4 turns of 21swg ECW, 7mm ID
T6	70mm	50Ω UT85 SEMI RIGID COAX	L4	3 turns of 21swg ECW on Fair-Rite FT50-75 core

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