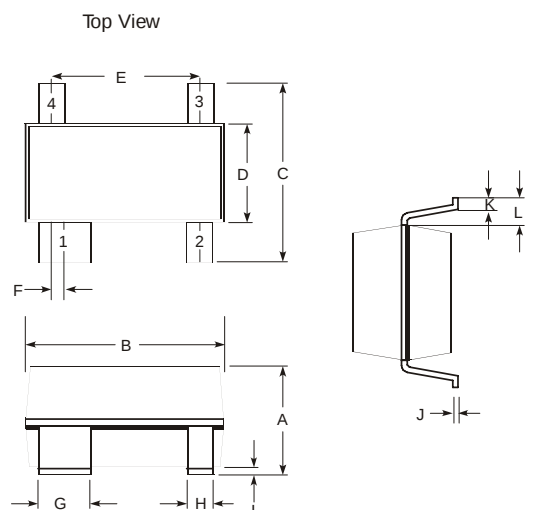


MECHANICAL DATA



SOT143 PACKAGE

PIN 1 – DRAIN
PIN 2 – SOURCE
PIN 3 – GATE
PIN 4 – SOURCE

Dim.	mm		Inches	
	min	max	min	max
A	0.89	1.12	0.035	0.044
B	2.80	3.04	0.110	0.120
C	2.10	2.64	0.083	0.104
D	1.20	1.40	0.047	0.055
E	1.92 BSC		0.075 BSC	
F	0.20 BSC		0.008 BSC	
G	0.76	0.94	0.030	0.037
H	0.37	0.51	0.015	0.020
I	0.05	0.15	0.002	0.006
J	0.09	0.18	0.004	0.007
K	0.40	0.60	0.016	0.024
L	0.55 REF		0.021 REF	

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 1W – 12.5V – 1GHz SINGLE ENDED

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- VERY LOW C_{rss}
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 10 dB MINIMUM

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
from 1 MHz to 1 GHz

P_D	Power Dissipation	1W
BV_{DSS}	Drain – Source Breakdown Voltage	40V
BV_{GSS}	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current	2A
T_{stg}	Storage Temperature	-65 to $125^\circ C$
T_j	Maximum Operating Junction Temperature	$150^\circ C$

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{DSS} Drain–Source Breakdown Voltage	V _{GS} = 0 I _D = 10mA	40			V
I _{DSS} Zero Gate Voltage Drain Current	V _{DS} = 12.5V V _{GS} = 0			1	mA
I _{GSS} Gate Leakage Current	V _{GS} = 20V V _{DS} = 0			1	μA
V _{GS(th)} Gate Threshold Voltage*	I _D = 10mA V _{DS} = V _{GS}	0.5		7	V
g _{fs} Forward Transconductance*	V _{DS} = 10V I _D = 0.2A	0.18			S
G _{PS} Common Source Power Gain	P _O = 1W	10			dB
η Drain Efficiency	V _{DS} = 12.5V I _{DQ} = 50mA	40			%
VSWR Load Mismatch Tolerance	f = 1GHz	20:1			—
C _{iss} Input Capacitance	V _{DS} = 0V V _{GS} = –5V f = 1MHz			12	pF
C _{oss} Output Capacitance	V _{DS} = 12.5V V _{GS} = 0 f = 1MHz			10	pF
C _{rss} Reverse Transfer Capacitance	V _{DS} = 12.5V V _{GS} = 0 f = 1MHz			1	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

THERMAL DATA

R _{THj-case}	Thermal Resistance Junction – Case	Max. 175 °C / W
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