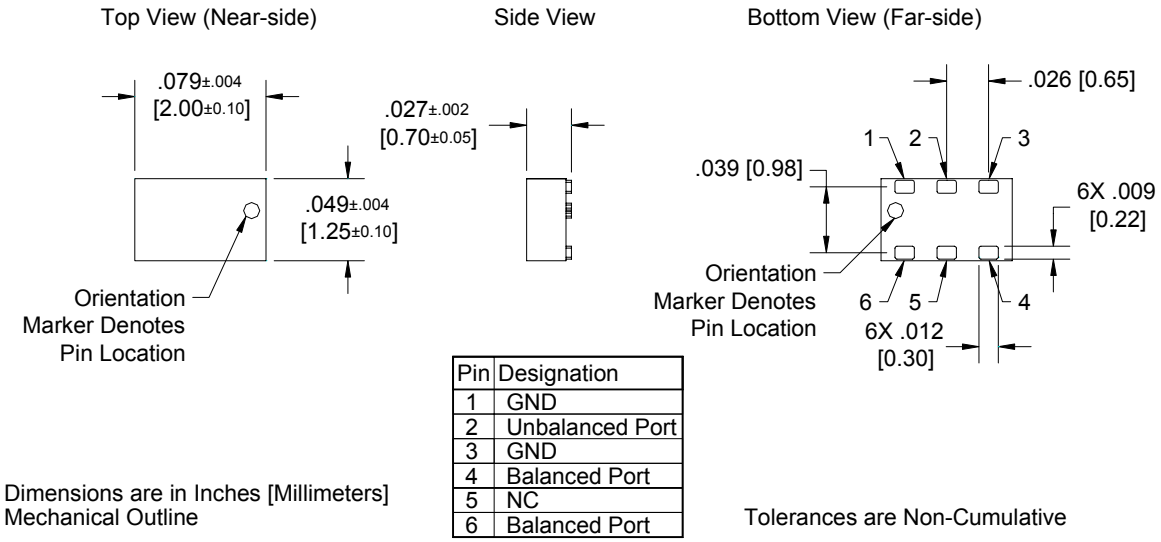
1 SCOPE

This document provides details on improving the unbalanced return loss of the B0922J7575 through the use of external capacitors connected to the unbalanced and balanced ports. Specifically, we are interested in improving the match at 950 MHz.

2 INTRODUCTION

The B0922J7575 is a balun providing transformation between balanced and unbalanced components. The B0922J7575 connects 75Ω unbalanced devices to 75Ω balanced devices over a 950MHz - 2150MHz frequency range. The B0922J7575 typically exhibits its worst case return loss at the lower frequency band (~950 MHz).

The pin layout is shown in Figure 1 below:



Pin	Designation
1	GND
2	Unbalanced Port
3	GND
4	Balanced Port
5	NC
6	Balanced Port

Figure 1 Pin layout of the B0922J7575 Balun

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3 Matching Capacitor on Unbalanced Port

In this case, matching is provided by tying a matching capacitor to the unbalanced pin (#2) as shown in the schematic below

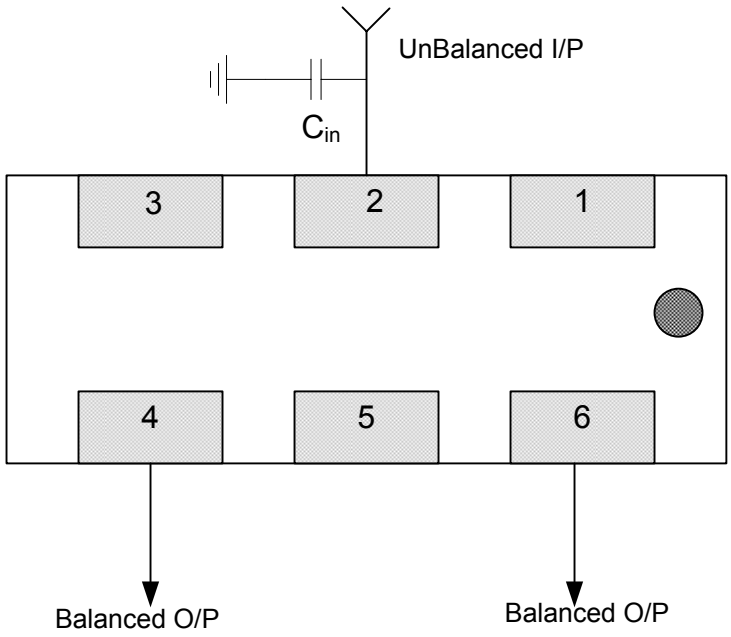

Figure 2 Schematic for 1 matching capacitor

A GENESYS model of the above was created and used to simulate the above configuration. The capacitor model used was a Modelithics model of an ATC 600S capacitor in a 0603 package. Parasitic reactance's were taken into account. The balun itself was modeled by using typical measured S-parameters.

The results are shown in Figure 3 and Figure 4 below for 4 values of capacitance (C = 0.0, 0.2, 0.4, 0.6 pF):

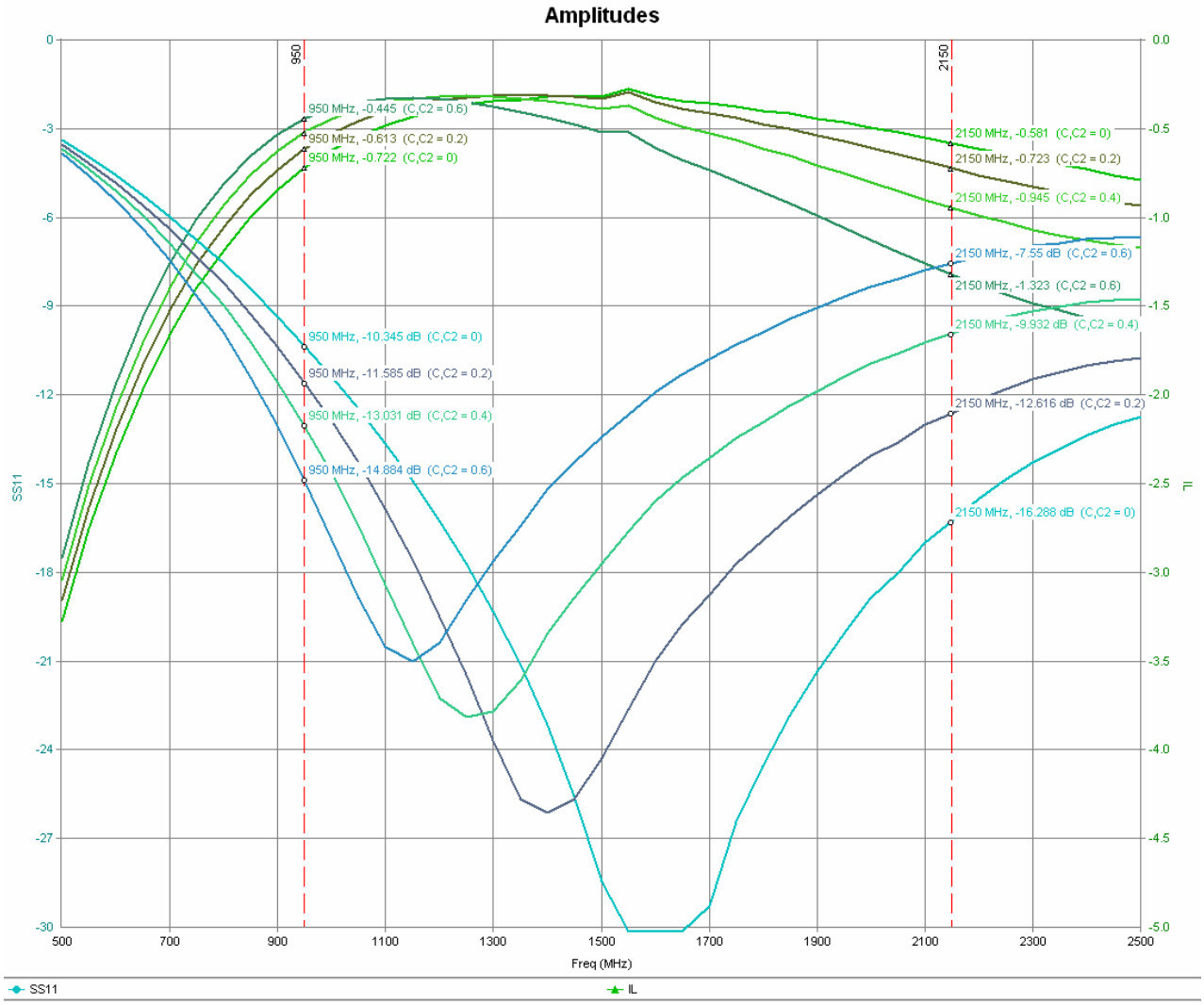

Figure 3 Insertion Loss and Unbalanced Port Return Loss for C =0, 0.2, 0.4 & 0.6 pF

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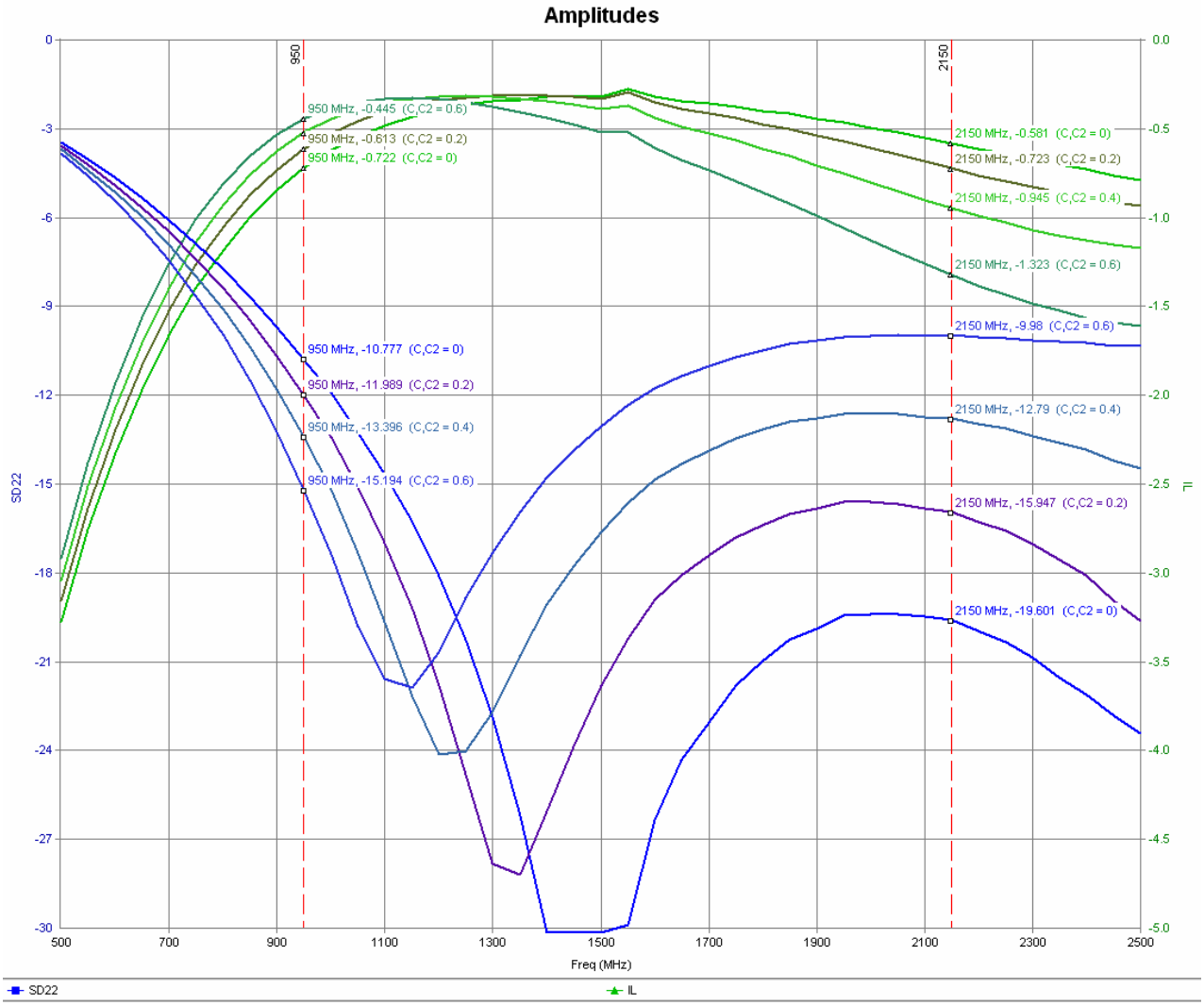

Figure 4 Insertion Loss and Balanced Port Return Loss for C=0, 0.2, 0.4 & 0.6 pF

The following table summarizes the results:

Frequency	C_{in} pF	Unbalanced Port Return Loss	Balanced Port Return Loss	Insertion Loss
950 MHz	0.0	-10.3	-10.8	-0.7
	0.2	-11.6	-12.0	-0.6
	0.4	-13.0	-13.4	-0.5
	0.6	-14.9	-15.2	-0.4
Worst Case Values	0.0	-10.3	-10.8	-0.6
	0.2	-11.6	-12.0	-0.7
	0.4	-9.9	-12.8	-1.0
	0.6	-7.5	-10.0	-1.3

It can be seen that the addition of a capacitor on the unbalanced port of the balun has a generally positive effect on the unbalanced and balanced port return losses at the low end of the band (950 MHz). However, at the high end (2150 MHz), the addition of this capacitor tends to degrade both insertion loss and both return losses.

An additional capacitor placed between the balanced ports can correct this problem as will be shown in the following section.

4 Matching Capacitor on Unbalanced & Balanced Ports

In this case, matching is provided by tying a matching capacitor to the unbalanced and balanced ports (pins # 2 and #4 & #6 respectively) as shown in the schematic below:

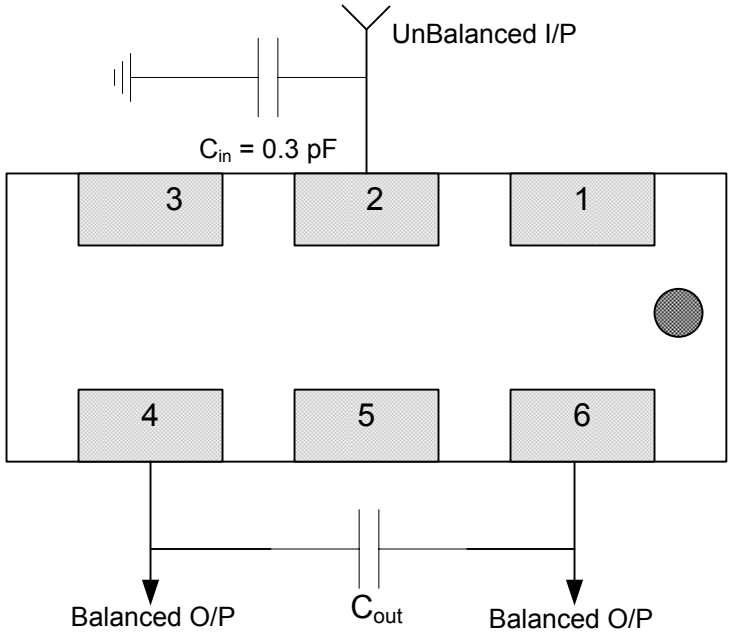

Figure 5 Matching Capacitors on unbalanced and balanced ports

As in the previous case, a GENESYS model was used to simulate the above configuration. The capacitor C_{in} was set to 0.3 pF while the capacitance between the balanced ports, C_{out}, was varied from 0.0 to 0.6 pF. As in the previous case, a Modelithics model of an ATC 600S capacitor with modeling of parasitics was used.

Figure 6 and Figure 7 show the results obtained for 4 values of C_{out}:

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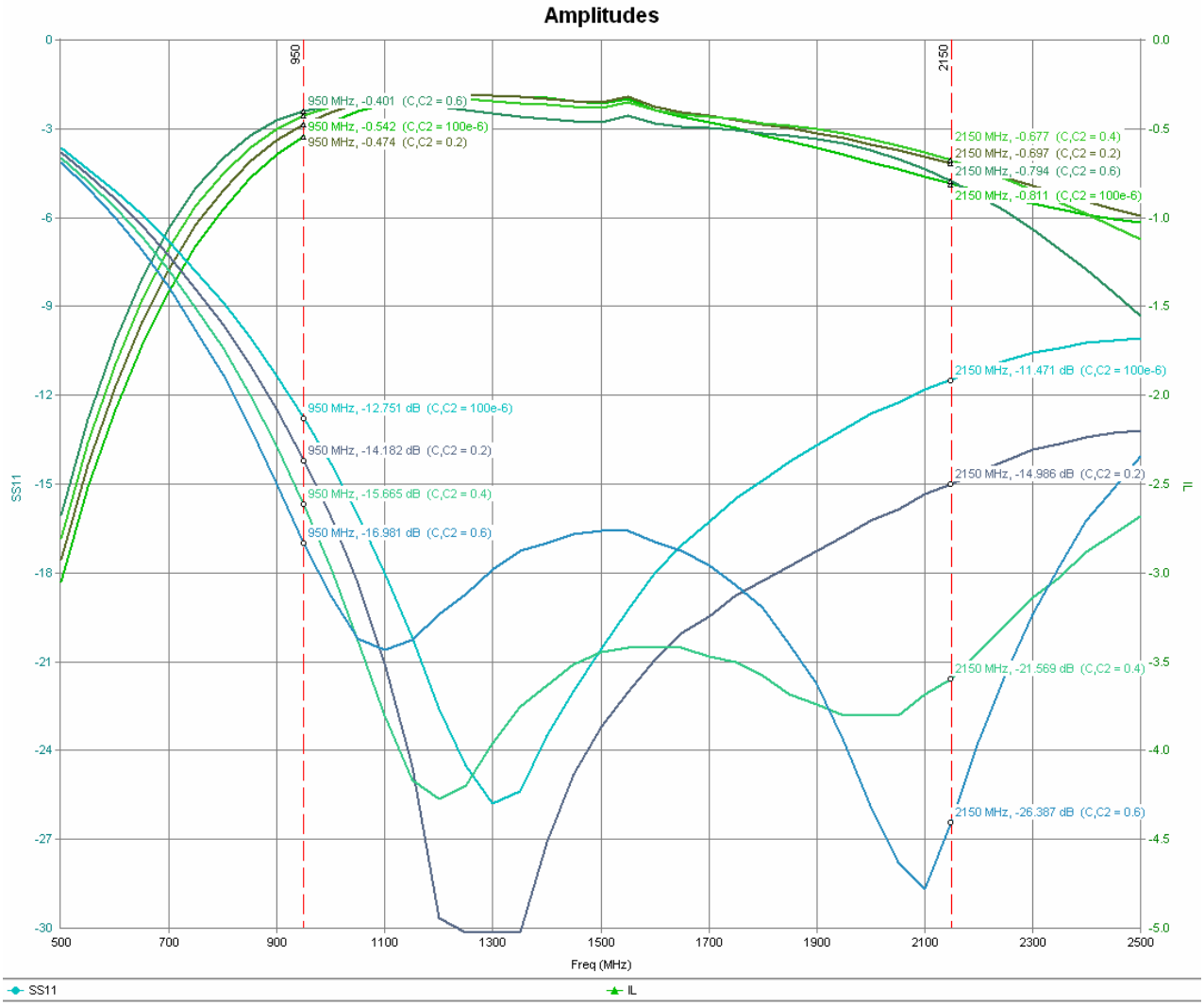

Figure 6 Insertion Loss & Unbalanced Port Return Loss for C_{out} = 0.0, 0.2, 0.4, & 0.6 pF

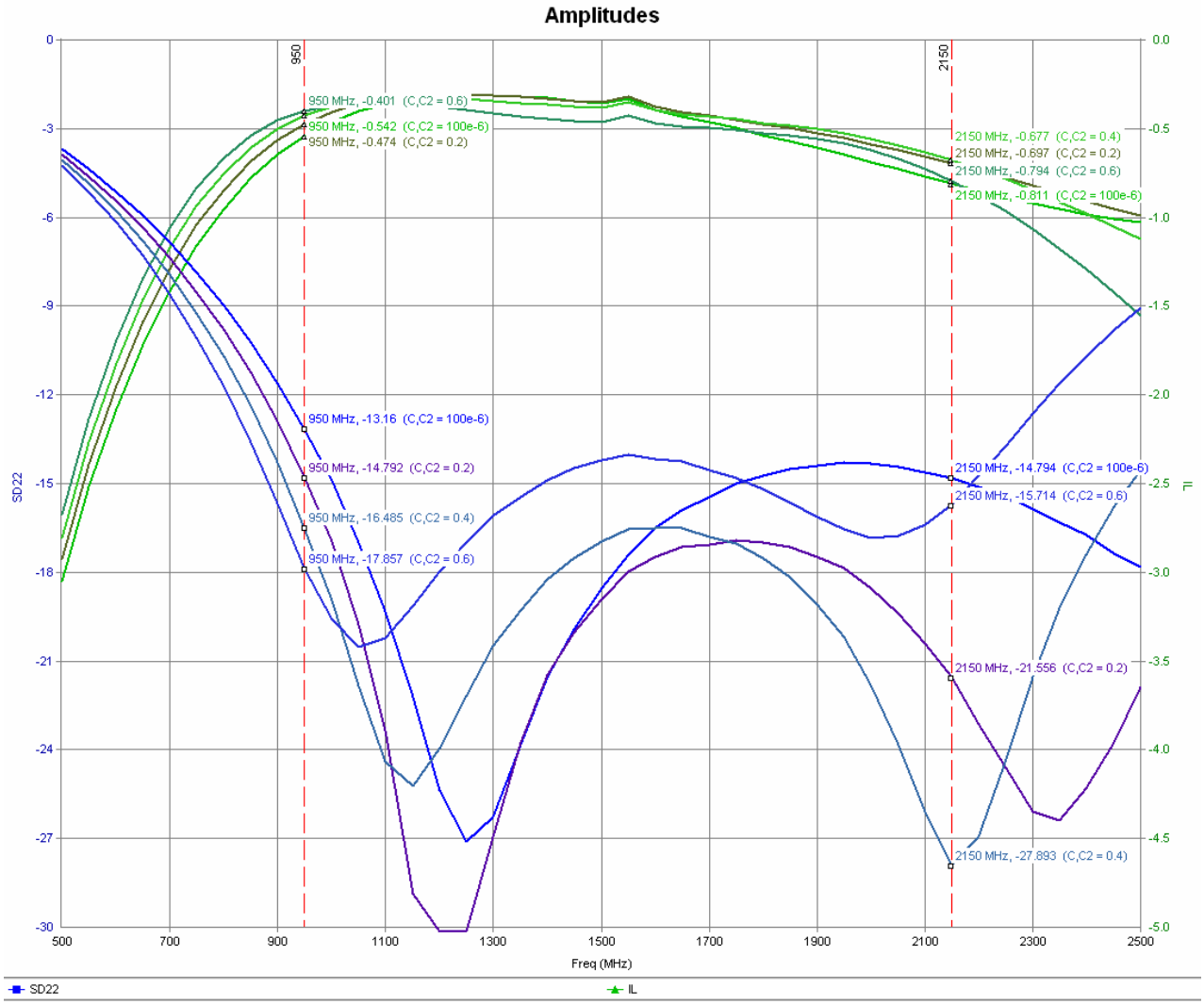

Figure 7 Insertion Loss & Balanced Port Return Loss for C_{out} = 0.0, 0.2, 0.4, & 0.6 pF

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The following table summarizes the results:

Frequency	C_{in} = 0.3 pF C_{out} pF	Unbalanced Port Return Loss	Balanced Port Return Loss	Insertion Loss
950 MHz	0.0	-12.8	13.2	-0.5
	0.2	-14.2	-14.8	-0.5
	0.4	-15.7	-16.5	-0.4
	0.6	-16.9	-17.8	-0.4
Worst Case Values	0.0	-11.5	-13.2	-0.8
	0.2	-14.2	-14.8	-0.7
	0.4	-15.7	-16.5	-0.7
	0.6	-17.0	-14.2	-0.8

The addition of a second capacitor between the balanced ports corrects to some extent the degradation of the return and insertion losses at the high end of the frequency band.

5 Sensitivity of Solution

As a test of the sensitivity of the solution and to gauge the effect of changing to another type of capacitor, the ATC 600S capacitor model was replaced with an ATC 100A capacitor model at the unbalanced and balanced ports as described in Section 4. The results for the same capacitor values as in the previous section (C_{in} = 0.3 pF and C_{out} = 0, 0.2, 0.4, & 0.6 pF) are shown in Figure 8 and Figure 9.

It can be seen that the results are similar. It may be inferred that the matching process is not overly dependant on the capacitor model but merely its overall capacitive rating.

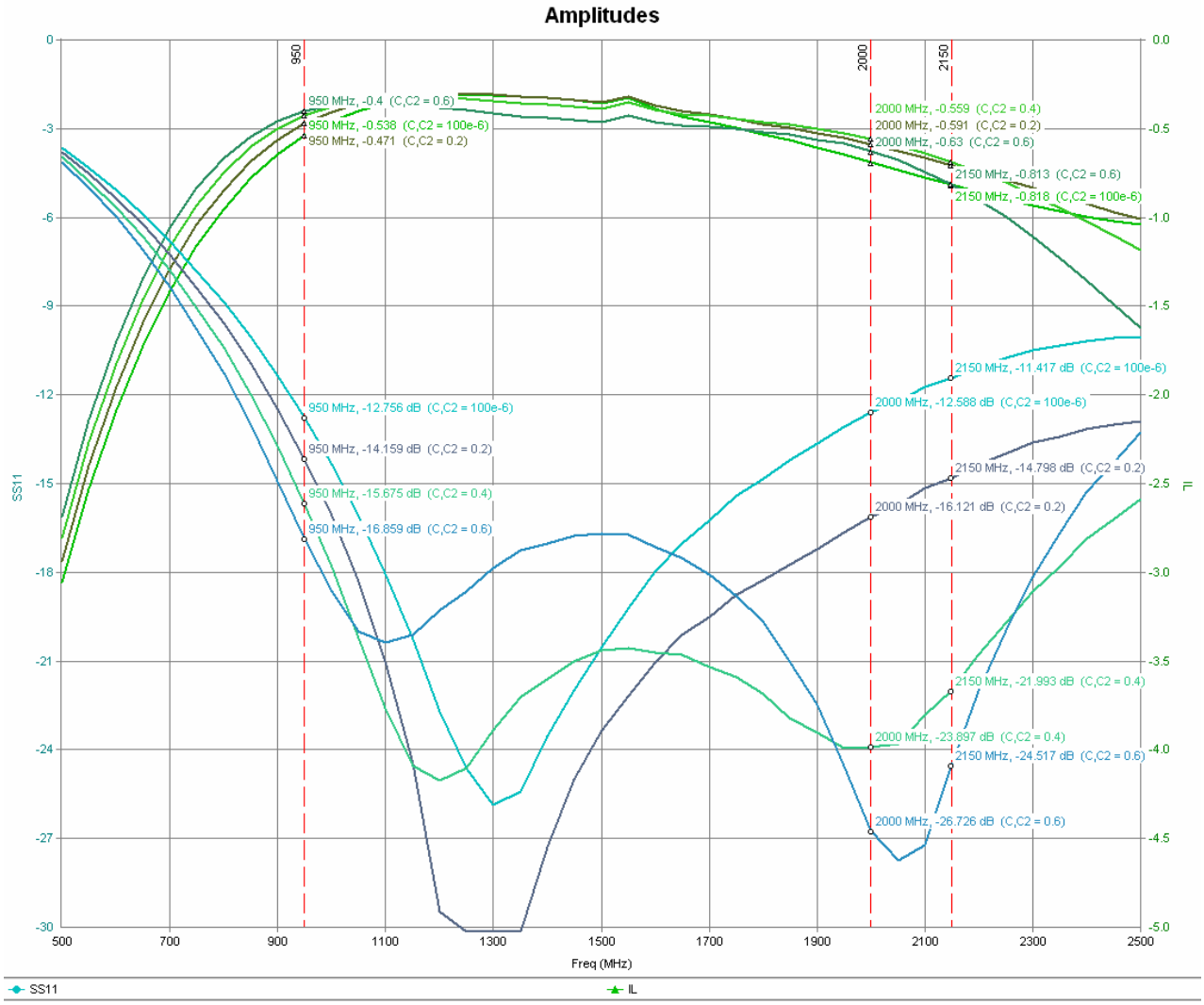

Figure 8 Insertion Loss & Unbalanced Port Return Loss for C_{out} = 0.0, 0.2, 0.4, & 0.6 pF using a different capacitor (ATC 100A)

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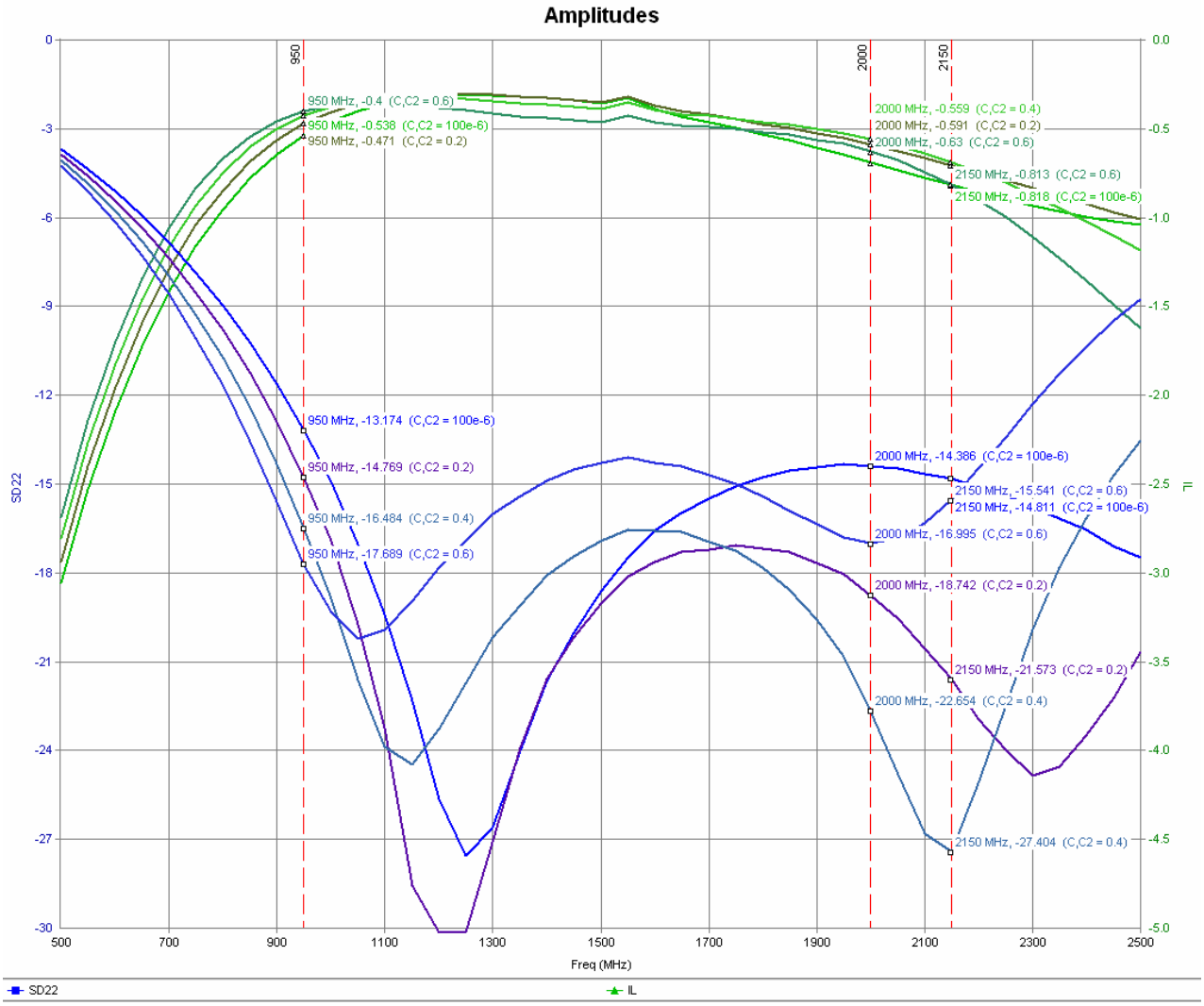

Figure 9 Insertion Loss & Balanced Port Return Loss for C_{out} = 0.0, 0.2, 0.4, & 0.6 pF using a different capacitor (ATC 100A)

6 Transmission Line Effects on Performance

6.1 Line Length Effects

A generic transmission line model was placed in front of the matching capacitances to simulate the effect of physical line lengths on matching performance. The line lengths examined were 0, 1.0°, 2.0°, 3.0°, & 4.0°. The characteristic impedances of the generic transmission lines were assumed to be 75Ω and 37.5Ω on the unbalanced and balanced ports respectively.

A GENESYS model of the configuration in Figure 5 was used to calculate the effects of these transmission lines. Figure 10 and Figure 11 show the return and insertion losses obtained with the

above line lengths. It can be seen that a degradation of the balanced and unbalanced return losses occurs at the upper frequency band with increasing line length. If the line lengths are kept to a minimum, the degradation can be kept to acceptable values.
Therefore, it is desirable to place the matching capacitors as close as possible to the balun ports in order to minimize transmission line effects.

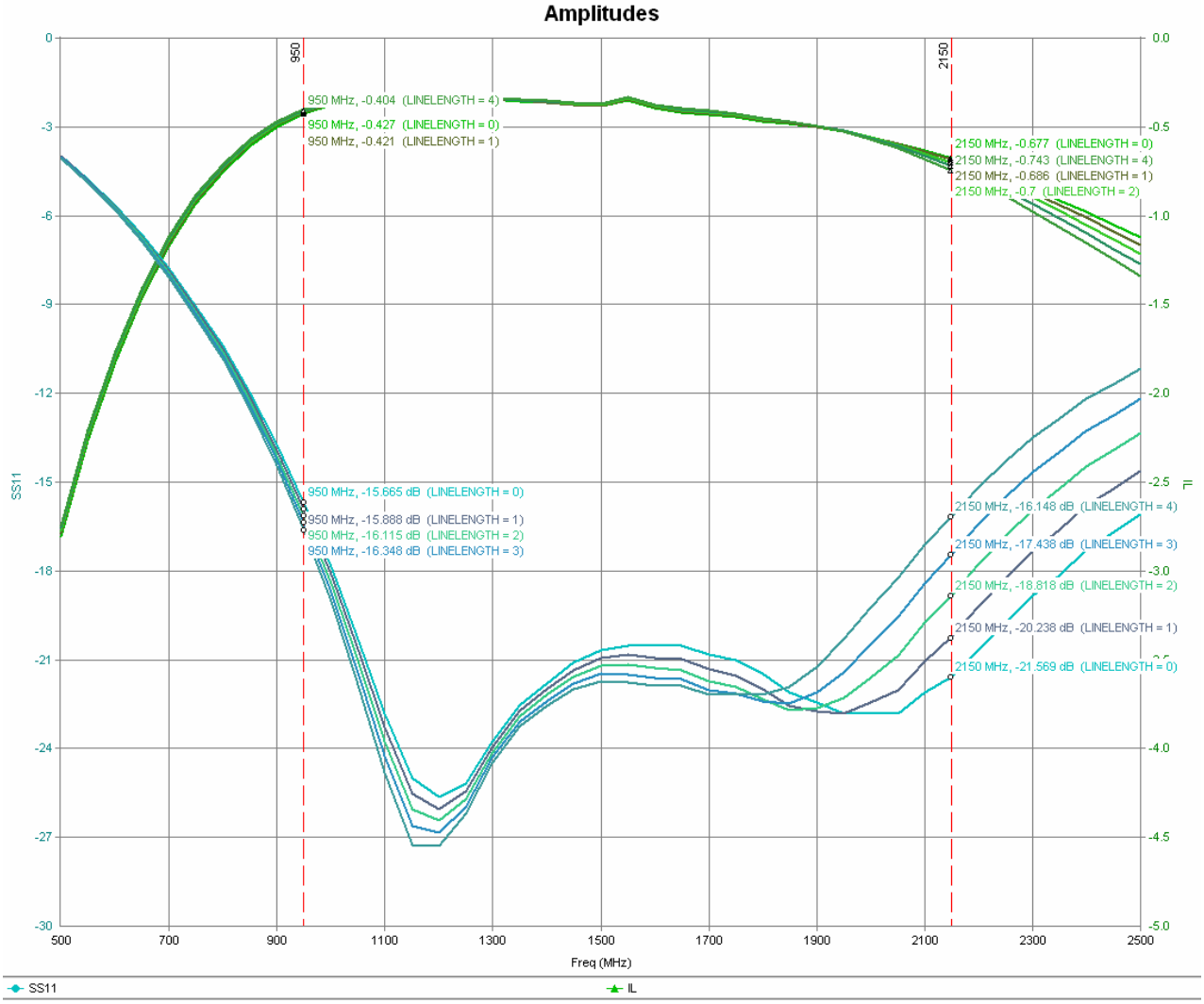

Figure 10 Effect of line lengths in front of matching capacitors: 0, 1.0°, 2.0°, 3.0°, & 4.0° on unbalanced return loss. Unbalanced and balanced port capacitors are set to 0.3 pF and 0.4 pF respectively

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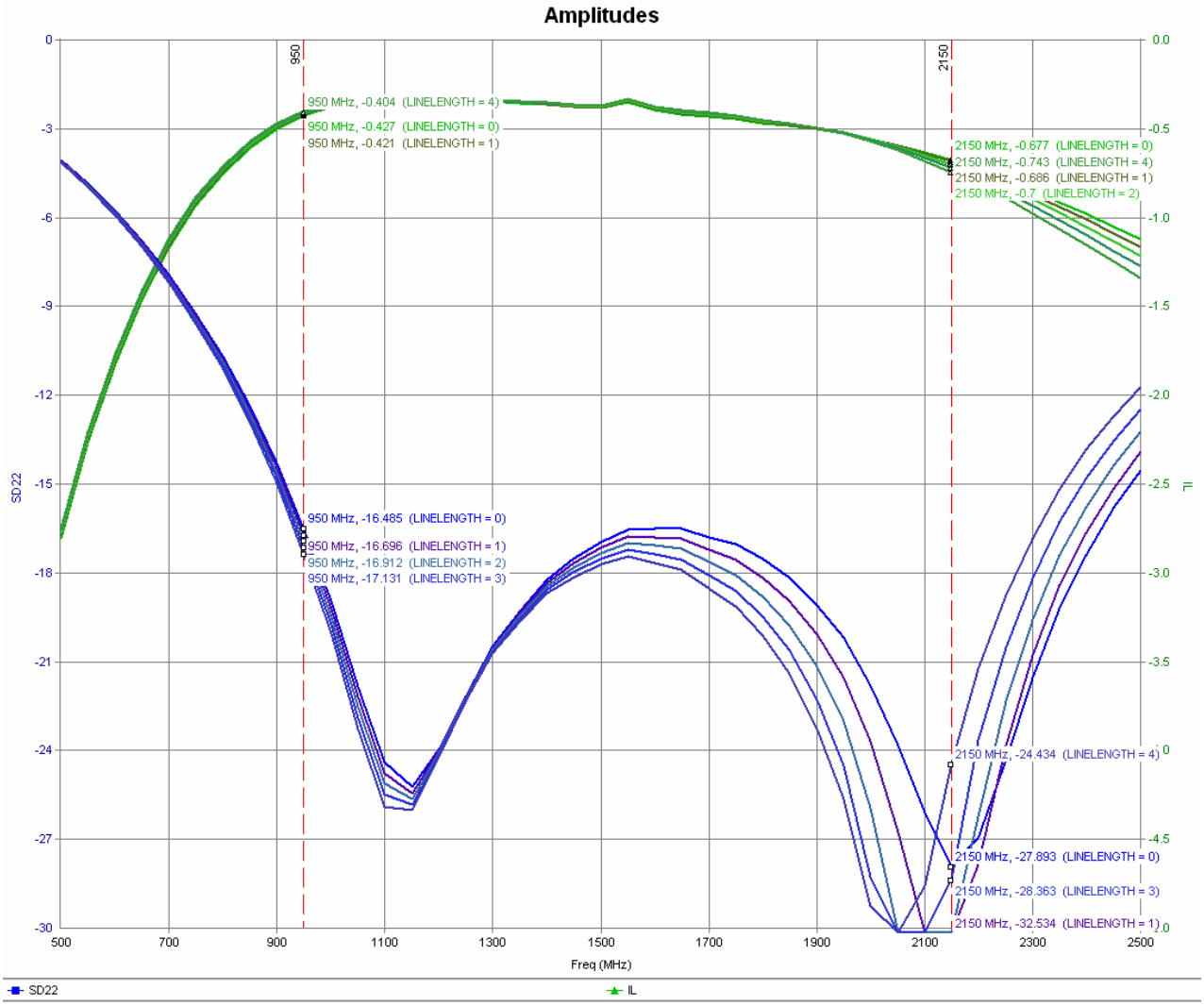

Figure 11 Effect of line lengths in front of matching capacitors: 0, 1.0°, 2.0°, 3.0°, & 4.0° on balanced port return loss.. Capacitors C_{in} and C_{out} are set to 0.3 pF and 0.4 pF respectively.

6.2 Variation of Characteristic Impedance

In order to assess the impact of variation of the characteristic impedance on performance, the Z_0 of the balanced port transmission lines was varied from 20 Ω to 55Ω. Two line lengths were examined: 2° and 4°.

For the 2° line length case, Figure 12 shows the unbalanced return loss for 5 impedances.

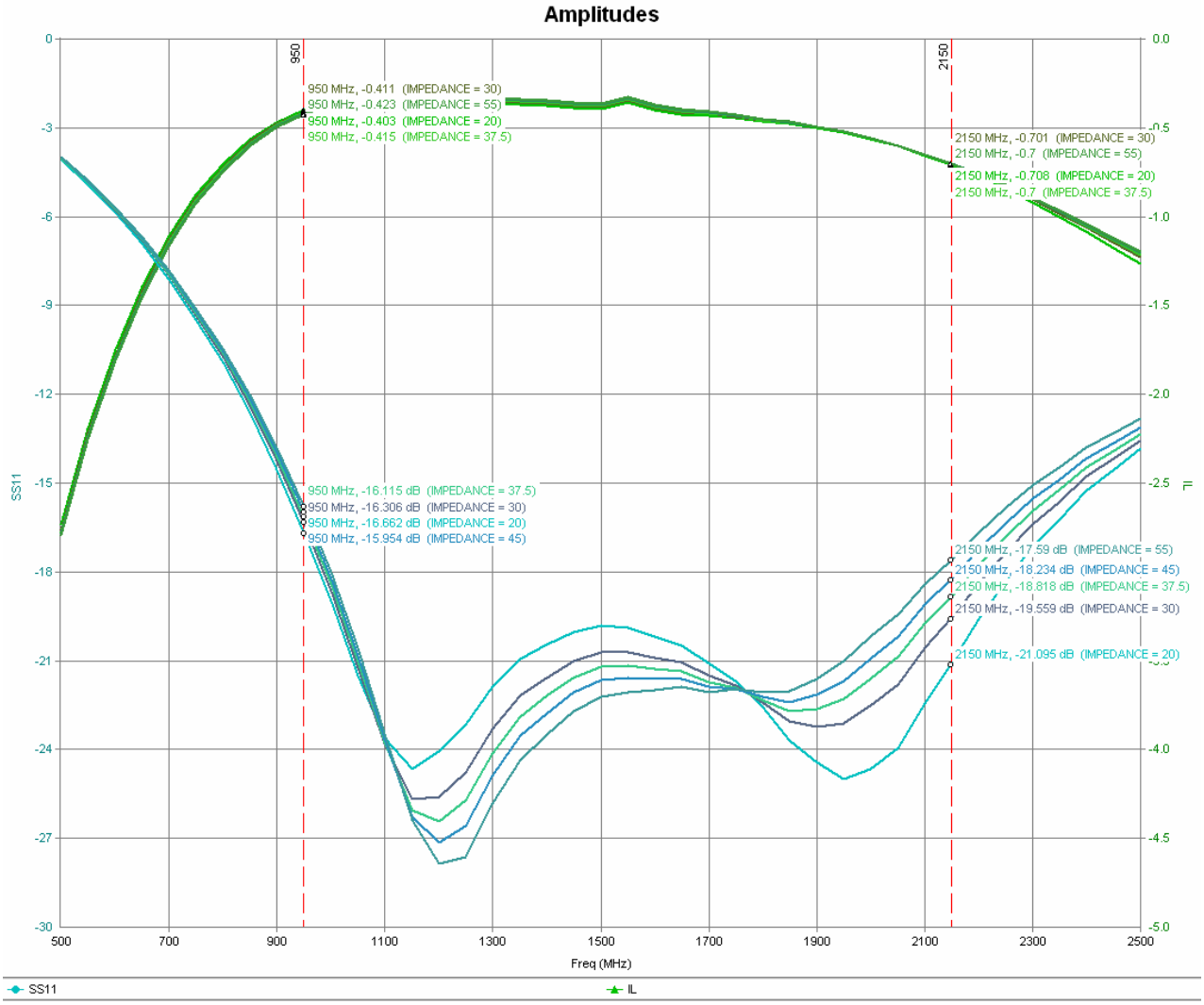

Figure 12 Unbalanced port return loss for Zo = 20, 30, 37.5, 45 & 55Ω. Linelengths = 2°

Increasing the line lengths to 4° yields the unbalanced port return loss curves shown in Figure 13. It can be seen that the longer line lengths result greater sensitivity to variations in characteristic impedance of the return loss, especially at the higher frequencies. Note that setting the line impedances to 37.5Ω gives the best compromise in return loss as expected.

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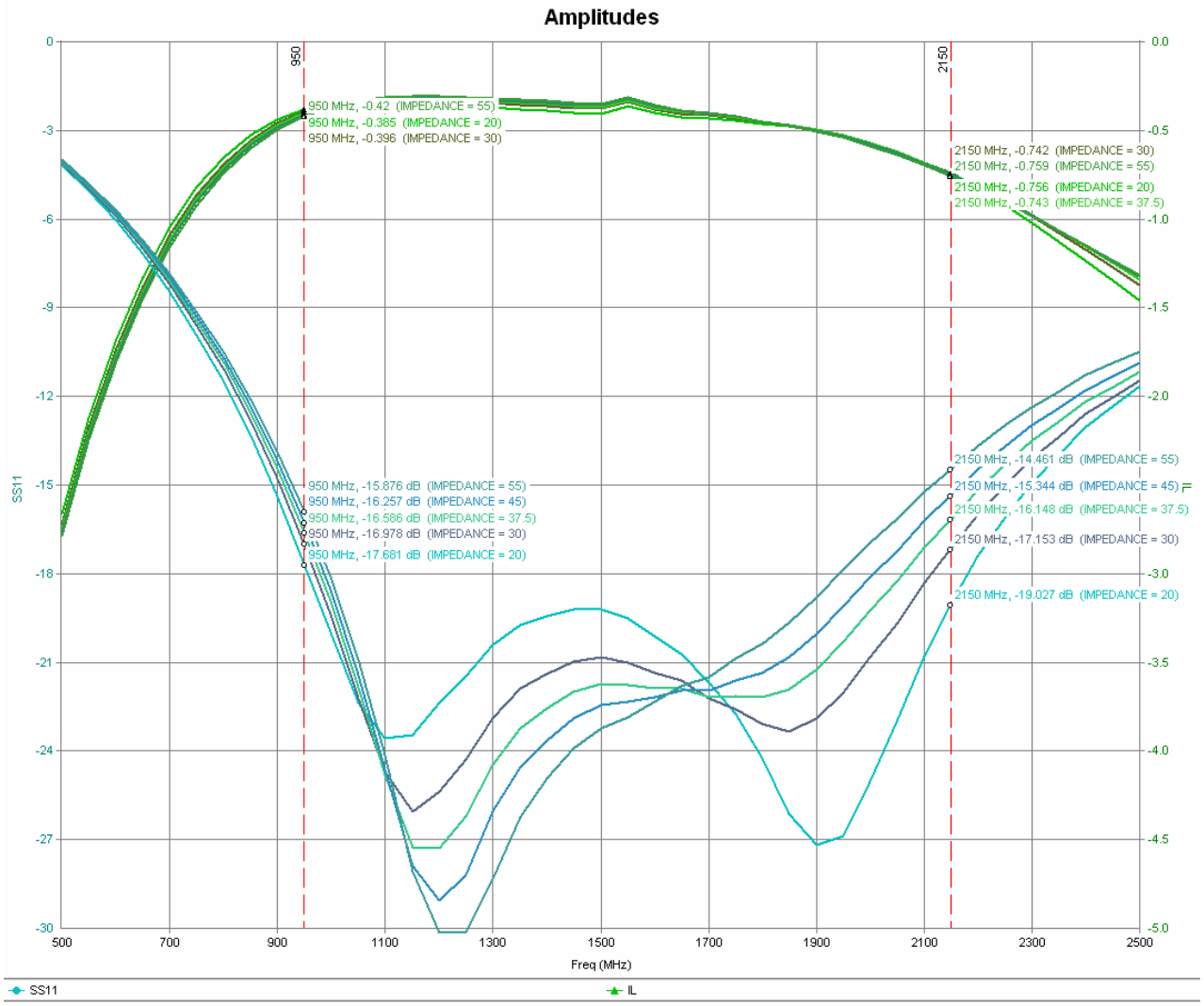

Figure 13 Unbalanced port return loss for Zo = 20,30 37.5 45 & 55Ω. Linelengths = 4°

7 Conclusion

A method of improving the unbalanced port return loss of the B0922J7575 balun has been presented. The addition of a single capacitor of about 0.2-0.6 pF will improve the return loss at the low end but at the expense of the insertion and return losses at the high end (2150 MHz). A second capacitor placed between the balanced ports will restore the high end return and insertion losses.

Therefore, in conclusion:

- The recommended capacitor combination is 0.3pF (C_{in}) on the unbalanced port to ground and 0.4pF (C_{out}) between the balanced ports.
- Care should be taken in the layout as the capacitors must be as close to the balun as possible because of the adverse transmission line effects as shown in Section 6.
- The unbalanced and balanced line impedances should be as close as possible to the nominal values of 75Ω and 37.5 Ω respectively.

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