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RF Power Reference Design

LTE 750 MHz Power Amplifier Lineup

InGaP HBT Driving GaAs pHEMT

MMG3014N Driving MRFG35010AN LTE

725–760 MHz, 1.0 W AVG., 12 V LTE AMPLIFIER LINEUP REFERENCE DESIGN

Amplifier Lineup Characteristics

This reference design provides a high-gain amplifier solution, specifically tuned for LTE and W-CDMA base station applications occupying the 725 to 760 MHz frequency band.

- Typical Single-Carrier LTE Performance
- GPA: V_{CC} = 5 Vdc, I_{CC} = 132 mAdc
- Power GaAs FET: V_{DD} = 12 Vdc, I_{DQ} = 180 mA, V_{GS} = –0.82 Vdc
- Output Power: 1.0 Watts Avg.
- 10 MHz Channel Bandwidth @ 10 MHz Offset
- Input Signal PAR = 10.5 dB @ 0.01% Probability on CCDF, IQ Magnitude Clipping

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
740 MHz	36.5	23.4	9.0	–40.3
750 MHz	36.4	24.1	9.0	–40.4
760 MHz	36.4	24.8	8.9	–40.4

- Output Capable of Handling 3:1 VSWR, @ 12 Vdc, 750 MHz, 10 Watts CW Output Power
- Designed for Digital Predistortion Error Correction Systems

MMG3014N/MRFG35010AN REFERENCE DESIGN

The amplifier lineup consists of a GaAs HBT pre-driver and GaAs pHEMT driver amplifier, tuned for optimal gain, efficiency, linearity and dynamic range performance at 1.0 Watts average output power. Performance characteristics of the reference design are provided in this document. Contact your local Freescale sales office or authorized Freescale distributor for additional information on reference design board availability for hands-on assessment and customization.

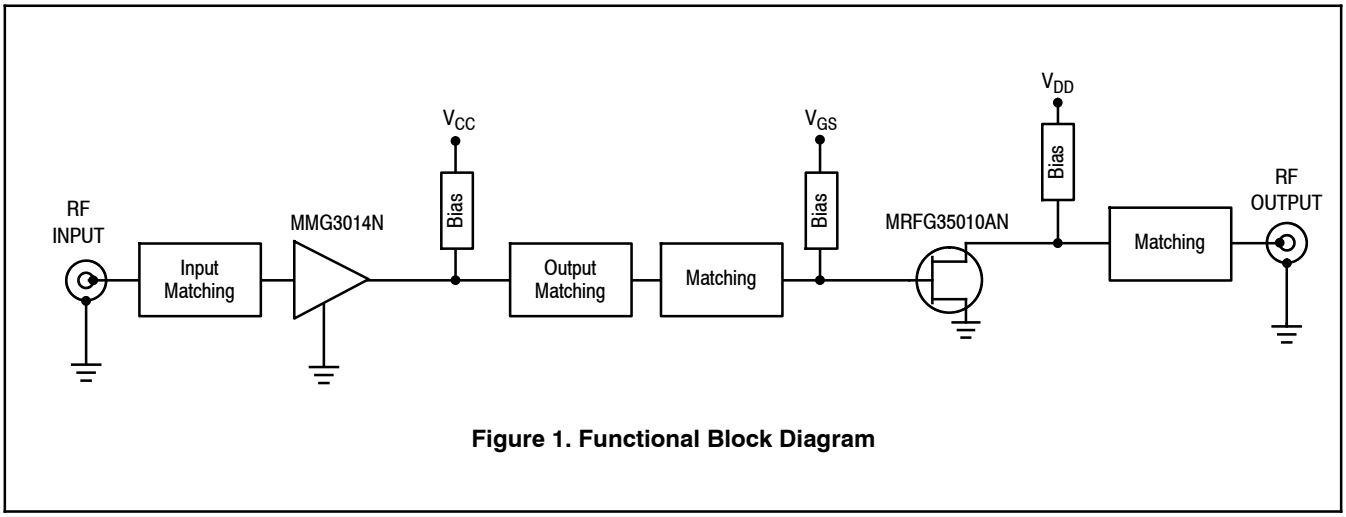


Figure 1. Functional Block Diagram

AMPLIFIER LINEUP TEST CONDITIONS

- GPA: V_{CC} = 5 Vdc, I_{CC} = 132 mAdc
- Power GaAs FET: V_{DD} = 12 Vdc, I_{DQ} = 180 mA, V_{GS} = –0.82 Vdc
- Output Power: 1.0 Watts Avg.
- IQ Magnitude Clipping

Note: Refer to Appendix A for Power–up Sequence

AMPLIFIER LINEUP — ALTERNATE CHARACTERISTICS

- Typical Single–Carrier W–CDMA Performance
- Measured in 3.84 MHz Channel Bandwidth @ 5 MHz Offset
- Input Signal PAR = 8.5 dB @ 0.01% Probability on CCDF

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
740 MHz	36.4	23.8	8.3	–40.9
750 MHz	36.3	24.5	8.2	–41.0
760 MHz	36.3	25.2	8.1	–41.0

REFERENCE DESIGN HARDWARE

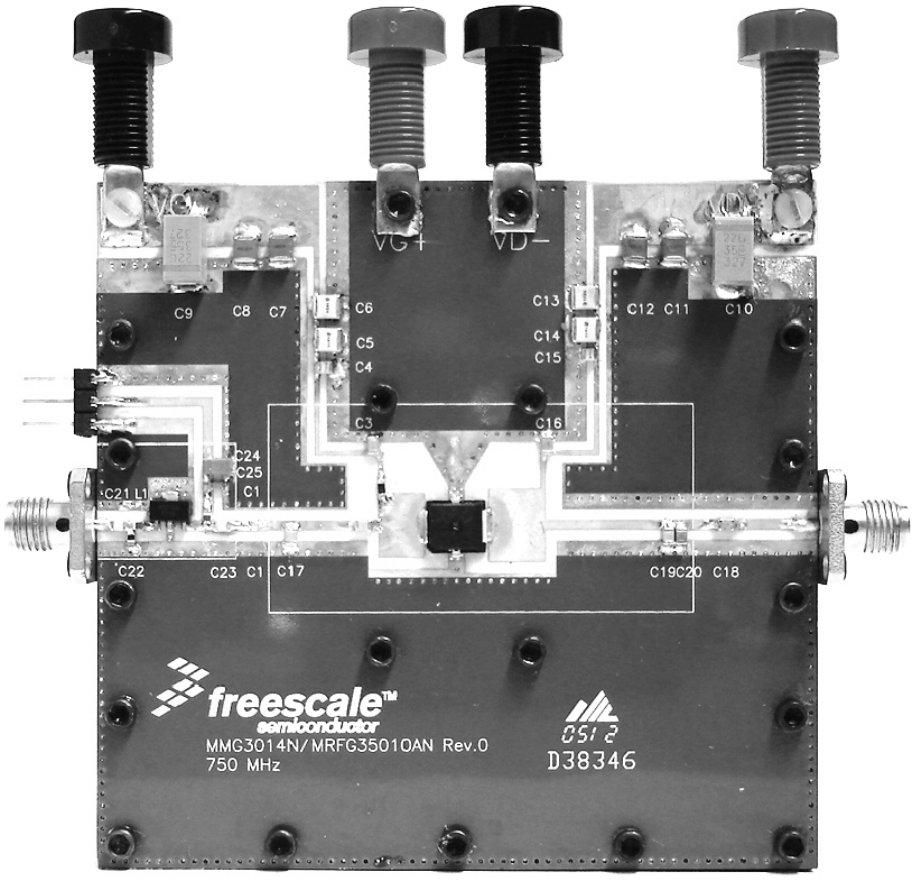


Figure 2. Performance Optimized Hardware

HEATSINKING

When operating this fixture it is important that adequate heatsinking is provided for the device. Excessive heating of the device may degrade the values of the included measurements and continued operation at excessive temperatures may destroy the device.

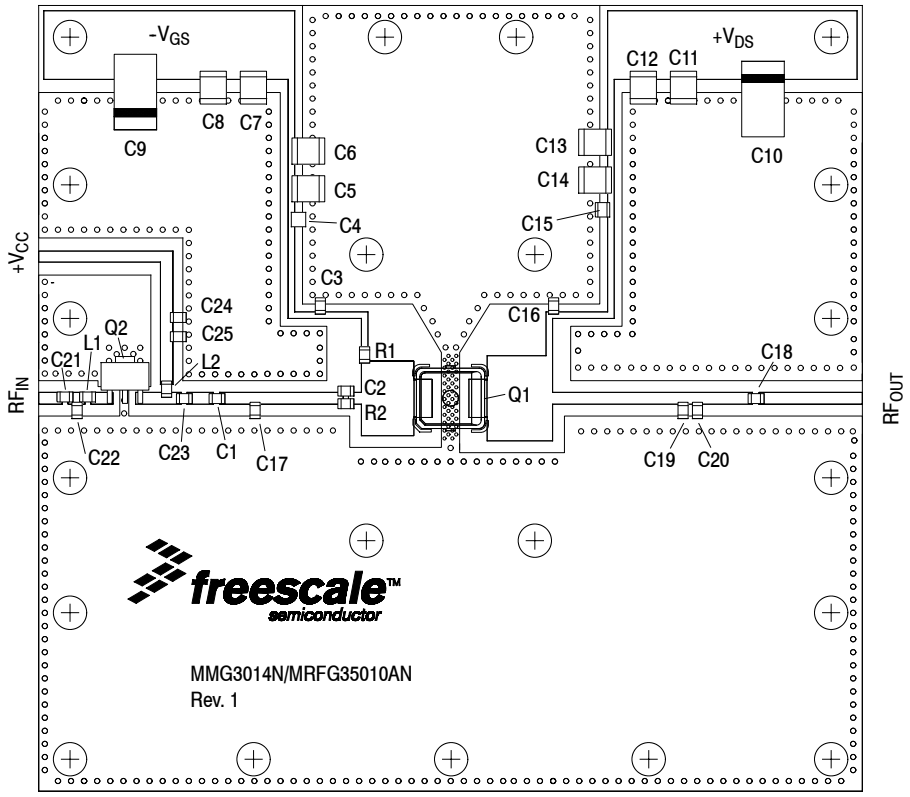


Figure 3. MMG3014N Driving MRFG35010AN Board Layout

Table 1. MMG3014N Driving MRFG35010AN Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C18	100 pF Chip Capacitors	ATC600F101JT250XT	ATC
C2	22 pF Chip Capacitor	ATC600F220JT250XT	ATC
C3, C16	10 pF Chip Capacitors	ATC100A100JP150XT	ATC
C4, C15	100 pF Chip Capacitors	ATC100A101JP150XT	ATC
C5, C14	100 pF Chip Capacitors	ATC100B101JP500XT	ATC
C6, C13	1000 pF Chip Capacitors	ATC100B102JP500XT	ATC
C7, C12	0.1 μF Chip Capacitors	CDR33BX104AKYS	Kemet
C8, C11	39K pF Chip Capacitor	ATC200B393KP50XT	ATC
C9, C10	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C17	12 pF Chip Capacitor	ATC600F120JT250XT	ATC
C19	1.8 pF Chip Capacitor	ATC600F1R8BT250XT	ATC
C20	8.2 pF Chip Capacitor	ATC600F8R2BT250XT	ATC
C21, C23	220 pF Chip Capacitors	C0805C221J5GAC	Kemet
C22	5.6 pF Chip Capacitor	06035J5R6BBS	AVX
C24	2.2 μF, 16 V Tantalum Capacitor	T491A225K016AS	Kemet
C25	0.1 μF Chip Capacitor	C0603C104J5RAC	Kemet
L1	4.7 nH Chip Inductor	LL1608-FH4N7S	TOKO
L2	10 nH Chip Inductor	LL1608-FH10NJ	TOKO
Q1	Power FET GaAs Transistor	MRFG35010ANT1	Freescale
Q2	InGaP HBT GPA	MMG3014NT1	Freescale
R1	51 Ω, 1/8 W Chip Resistor	RM73BIJT510J	KOA Speer
R2	5.1 Ω, 1/4 W Chip Resistor	CRCW08055R10JNEA	Newark
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

TYPICAL CHARACTERISTICS — 10 MHz LTE Test Signal

(Single−Carrier LTE, Test Model 1.1, 10 MHz, PAR = 10.5 dB @ 0.01% Probability on CCDF)

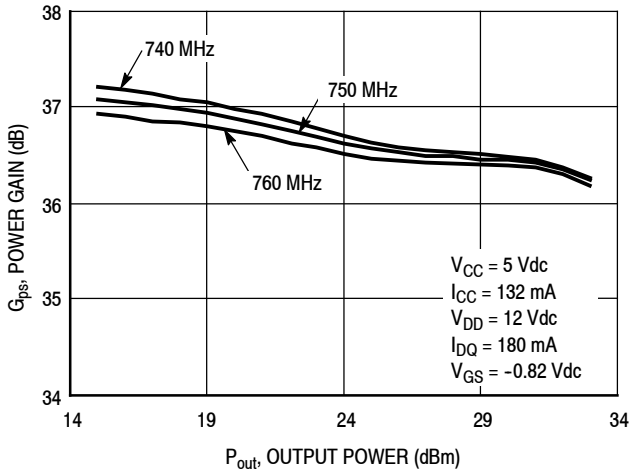


Figure 4. Power Gain versus Output Power

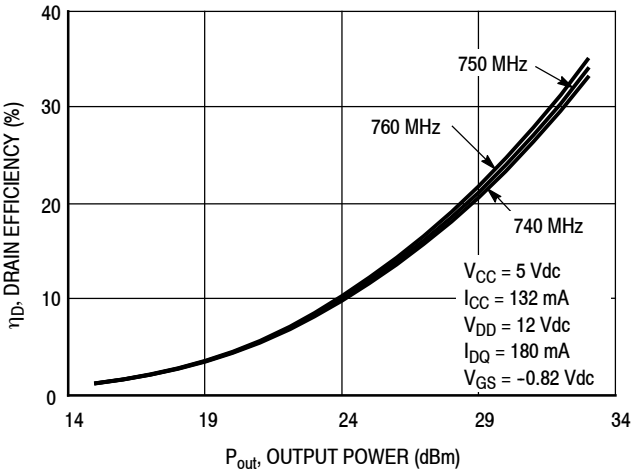


Figure 5. Drain Efficency versus Output Power

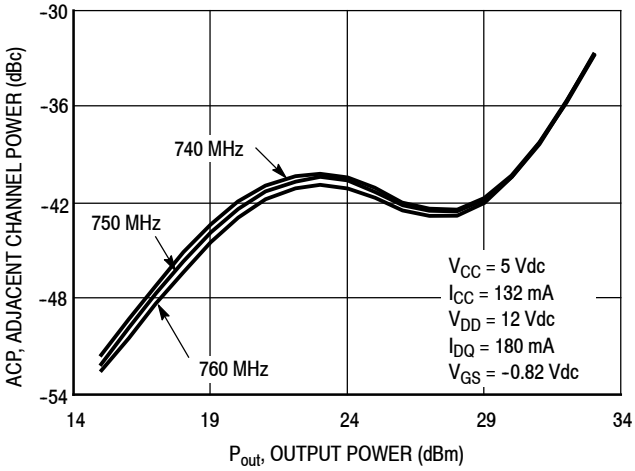


Figure 6. Adjacent Channel Power versus Output Power

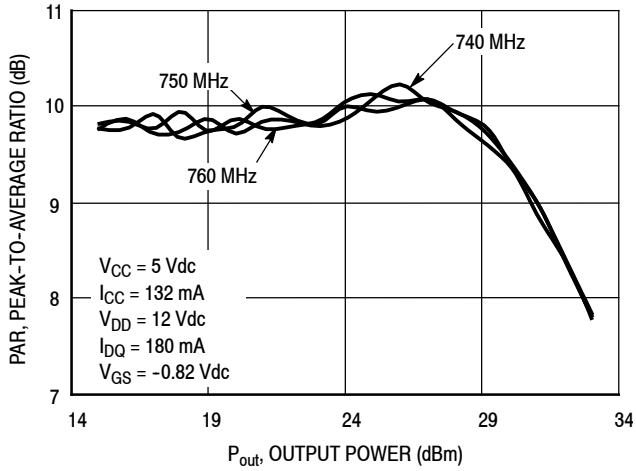


Figure 7. Peak−to−Average Ratio versus Output Power

10 MHz LTE TEST SIGNAL

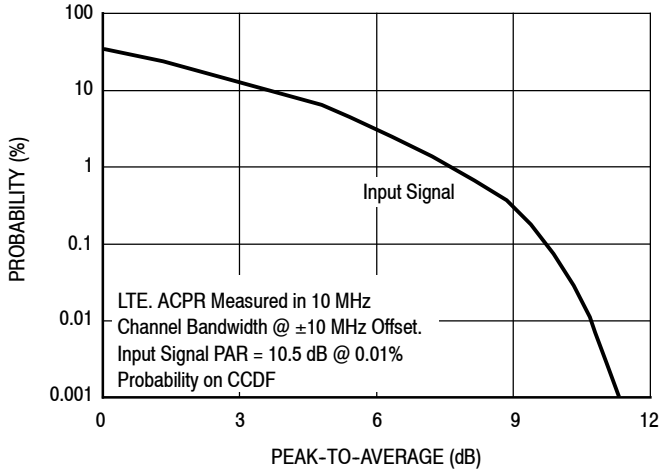


Figure 8. CCDF LTE IQ Magnitude Clipping, Single−Carrier Test Signal

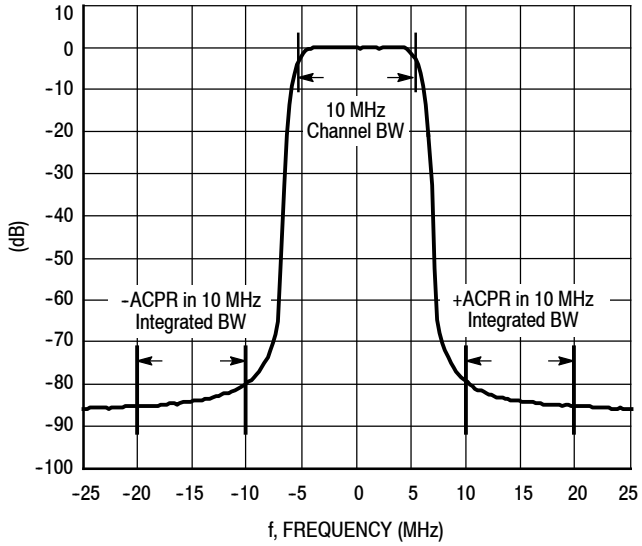


Figure 9. Single−Carrier LTE Spectrum

TYPICAL CHARACTERISTICS — 8.5 dB Input PAR W-CDMA Test Signal

(Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, PAR = 8.5 dB @ 0.01% Probability on CCDF)

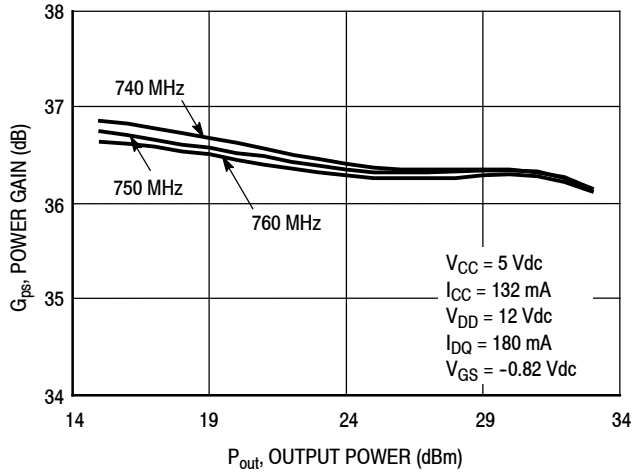


Figure 10. Power Gain versus Output Power

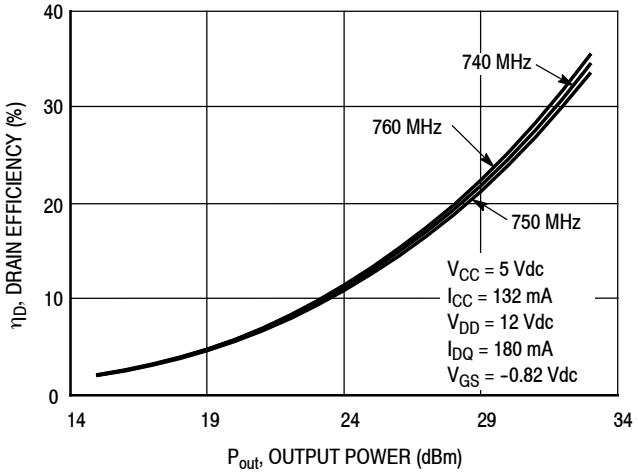


Figure 11. Drain Efficency versus Output Power

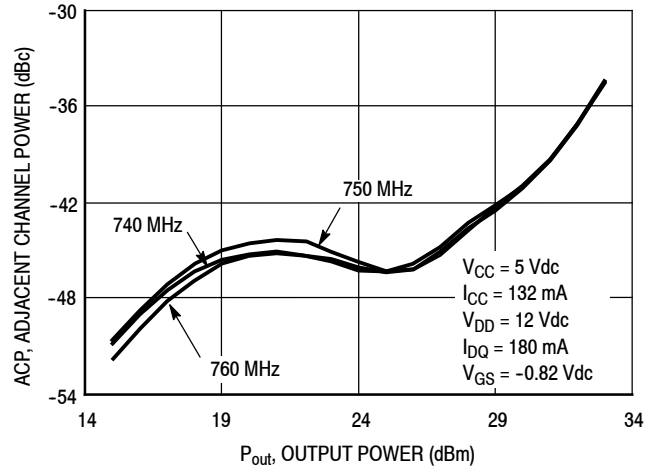


Figure 12. Adjacent Channel Power versus Output Power

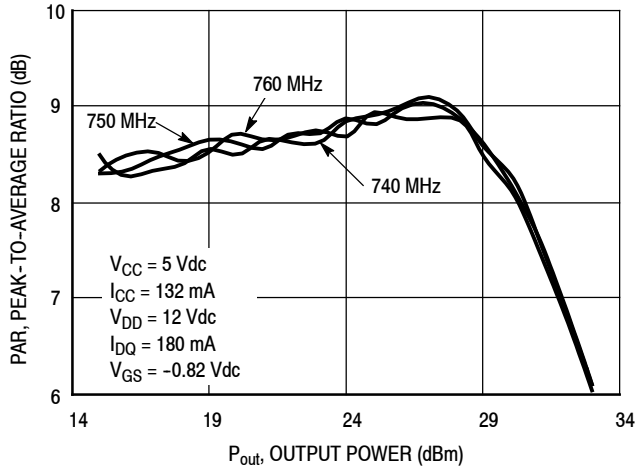


Figure 13. Peak-to-Average Ratio versus Output Power

8.5 dB W-CDMA TEST SIGNAL

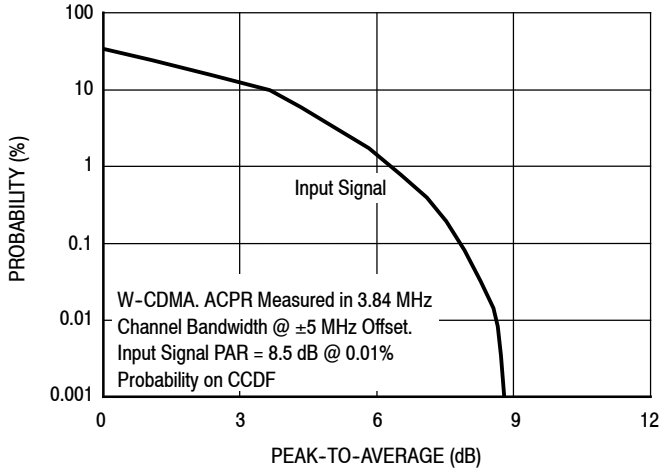


Figure 14. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

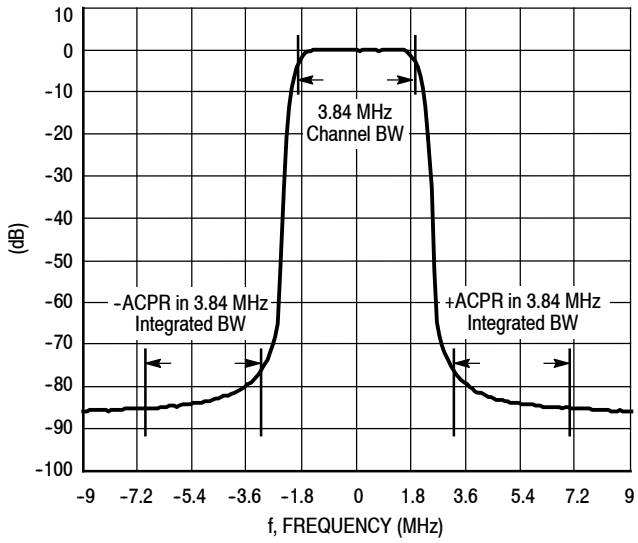
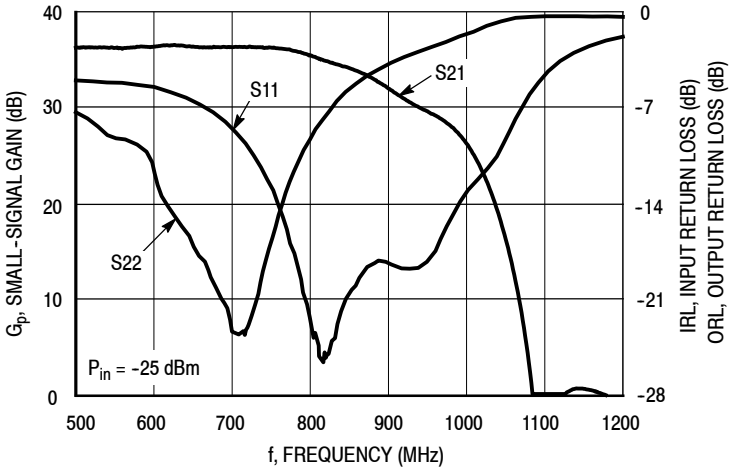


Figure 15. Single-Carrier W-CDMA Spectrum

MMG3014N Driving MRFG35010AN LTE Reference Design

CHARACTERISTICS — CW Test Signal



Note: Reference Impedance = 50 Ω

Figure 16. Small-Signal Gain, Input and Output Return Loss versus Frequency

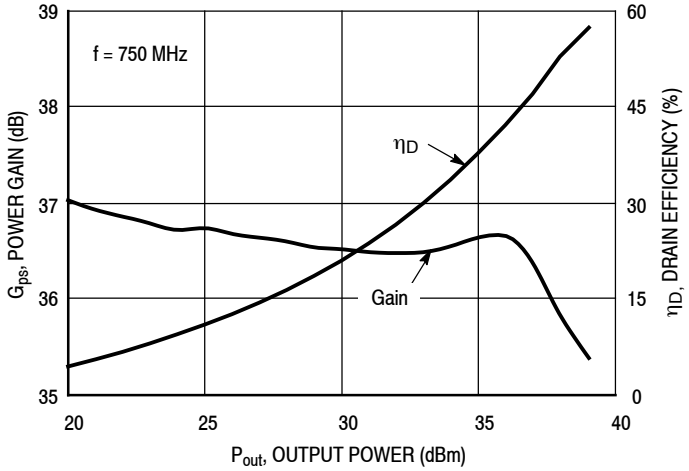


Figure 17. Power Gain and Drain Efficency versus Output Power

APPENDIX A

Power-Up Sequence

The MMG3014N and MRFG35010AN devices are biased separately. Apply bias as follows:

1. Terminate the RF input and output with 50 Ω impedances: no RF signal applied.
2. Apply −1.5 Vdc supply across the $-V_{GS}$ (negative gate voltage) and GND terminals of MRFG35010AN.
3. Apply +12 Vdc supply across the $+V_{DS}$ (positive drain voltage) and GND terminals of MRFG35010AN.
4. Increase the $-V_{GS}$ value to set the I_{DQ} (drain quiescent current) to 180 mA. $-V_{GS}$ should be approximately −0.82 Vdc.
5. Apply +5 V supply to V_{CC} terminal of MMG3014N.
6. I_{CC} should be around 132 mA.
7. Apply RF signal to input terminal and set signal level to −20 dBm.

Power-Down Sequence

1. Remove RF signal from input terminal.
2. Remove V_{CC} from MMG3014N.
3. Adjust MRFG35010AN's $-V_{GS}$ to −1.5 Vdc.
4. I_{DQ} should be near zero.
5. Remove $+V_{DS}$ from MRFG35010AN.
6. Remove $-V_{GS}$ from MRFG35010AN.

APPENDIX B

Tuning Tips

- Adjusting the value or location of C19 and C20 will have significant effect on ACPR, output return loss and efficiency.
- Adjusting the values or locations of C17 on MRFG35010AN input will have significant impact on gain and input return loss.

APPENDIX C

Simulation Models

Download simulation models of MMG3014N and MRFG35010AN from:

http://www.freescale.com/RFMMIC (click on the “Design Support” tab)

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