SAX280 Data Sheet

Small Form Factor
UHF [225 - 400] MHz Tunable Bandpass Filter

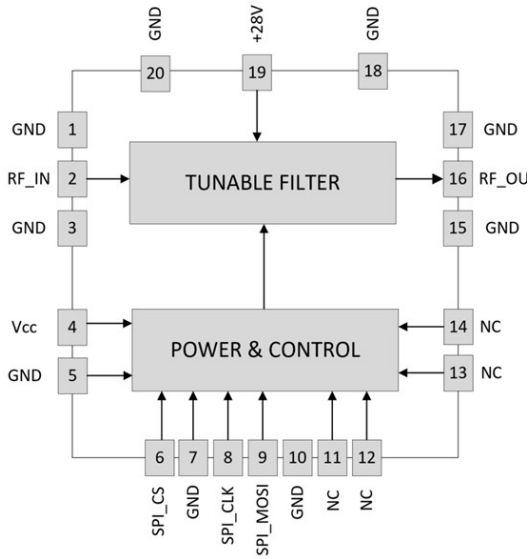
Applications

- Military Radios
- Military Radar
- SATCOM
- Test and Measurement

Features

- +27dBm CW Continuous Power Handling
- Low Insertion Loss [4.0dB typ]
- 15dB Selectivity [typ] @ +/- 10%
- Low Power Consumption [<100 mW]

Block Diagram



Specifications

Parameter	Specification	Min	Typ	Max	Units
Tunable Frequency Range	[225 - 400] MHz	225	-	400	MHz
Passband Bandwidth	[225 - 400] MHz	-	5	-	%
Input / Output Impedance	-	-	50	-	Ohms
Return Loss	[225 - 400] MHz	9.54	15.56	-	dB
Insertion Loss	[225 - 400] MHz	-	4.0	4.4	dB
Rejection	Fc +/- 10 %	14	15	-	dB
	10 MHz to 0.5*Ftune	30	50	-	dB
	2*Ftune to 750 MHz	30	50	-	dB
P1dB Input Power	[225 -400] MHz	-	27	-	dBm
Tuning Time	-	-	15	25	us
Tuning Step Size	[225 – 400] MHz	-	2	-	MHz
Vcc	+5.0V Supply Voltage	+4.9	+5.0	+5.1	V
Icc	+5.0V Supply Current	-	16	18	mA
Vbb	+28V Supply Voltage	+27	+28	+29	V
Ibb	+28V Supply Current	-	0.2	0.3	mA
Size	[0.5 x 0.5 x 0.19]				inch

Environmental

Vibration Testing	Vehicular to MIL_STD_810G Method 514.6
	Jet Fighter to MIL_STD_810F Method 514.5G
Operational Temperature	-40 to +85°C
Storage Temperature	-40 to +125°C

Timing / SPI Control

The SAX280 Tunable Filter is controlled as a slave SPI device. The SPI interface is used to input a 16-bit filter select word. This interface is Write-only so there are only three SPI signals required:

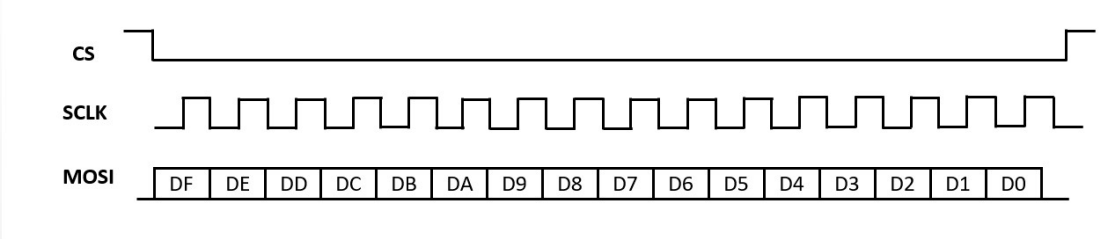
- CS input: When CS is low, the SPI bus is enabled.
  When CS is high, signals on the other SPI inputs are ignored.
- SCLK: Serial data clock generated by the SPI bus master.
- MOSI: Data from master to slave (Master Out, Slave In).
- MISO: Always Logic Low. [Internally factory set]

The timing of the SPI bus is:

- The base value of the clock is low (0).
- The unit reads the incoming data (MOSI) on the rising edge of the clock SCLK.
- The maximum allowed SCLK rate is 1.0 MHz.

The figure below shows the SPI bus set command operation:

- The SPI bus master sets CS low and generates the SCLK.
- The master sends a 16-bit filter select word (MSB first) on the MOSI line.
- After the last clock pulse, the SPI bus master sets CS high.

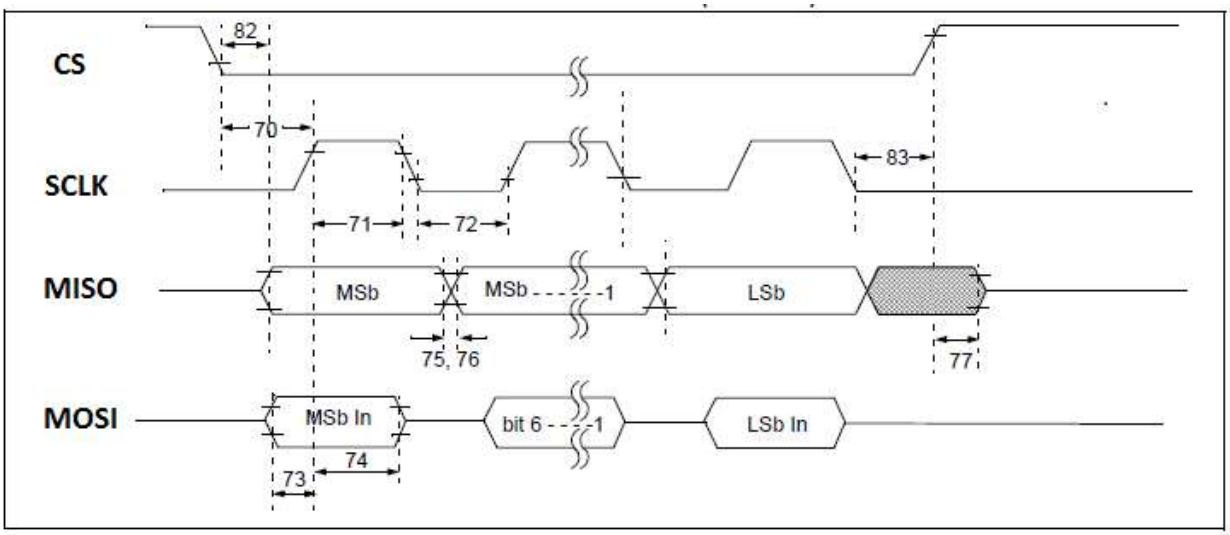


SAX280 uses a +28.0V supply for switches and a +5.0V supply for control.

All Digital I/O are supplied at +5.0V.

- CS input: Logic low = 0.8V Max., Logic High = 2.0V Min.
- SCLK: Logic low = 0.2V Max., Logic High = 4.0V Min.
- MOSI: Logic low = 0.2V Max., Logic High = 4.0V Min.
- MISO: Output is always Logic Low = 0.8V Max

SPI TIMING and REQUIREMENTS



Param. No.	Symbol	Characteristic	Min	Max	Units
70	TssL2sc	CS Fall or SCLK Fall or Rise	62.5	"	ns
71	TscH	SCLK Input High Time	25	"	ns
72	TscL	SCLK Input Low Time	30	"	ns
73	Tdi2sc	Setup Time of Data Input to SCLK Edge	25	"	ns
74	Tsc2di	Hold Time of Data Input to SCLK Edge	25	"	ns
75	TdoR	Data Output Rise Time	"	30	ns
76	TdoF	Data Output Fall Time	"	20	ns
77	TssH2Z	CS Rise to Data Output High Impedance	10	50	ns
82	Tss2doV	Data Output Valid After CS Falling Edge	"	60	ns
83	Tsc2ssH	CS Rise after SCLK edge	133.5	"	ns

Pinout Table

Pin No.	Label	Description, Conditions
1, 3, 5, 7, 10, 15, 17, 18, 20	GND	Digital and Analogue Ground
2	RF_IN	RF Input Signal
4	Vcc	+5.0V Supply Voltage Input
6	SPI CS	Serial Tune Chip Select
8	SPI CLK	Serial Tune Interface Clock. Data is latched onto the rising edge.
9	SPI MOSI	Serial Tune Interface Master Out Slave Input
11, 12, 13, 14	NC	Factory Use Only
16	RF_OUT	RF Output Signal
19	Vbb	+28V Supply Voltage

Outline