SFP HSSDC II Copper Module Transceiver

1. SCOPE

1.1. Content

This specification covers performance, tests and quality requirements for the Tyco Electronics Small Form Factor Pluggable (SFP) High Speed Serial Data Connector II (HSSDC II) Copper Module Transceiver for Fibre Channel and InfiniBand™ applications.

1.2. Qualification

When tests are performed on the subject product line, procedures specified in Figure 1 shall be used. All inspections shall be performed using the applicable inspection plan and product drawing.

1.3. Qualification Test Results

I Successful qualification testing on the subject product line was completed on 27May03. The Qualification Test Report number for this testing is 501-537. This documentation is on file at and available from Engineering Practices and Standards (EPS).

2. APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the latest edition of the document applies. In the event of conflict between the requirements of this specification and the product drawing, the product drawing shall take precedence. In the event of conflict between the requirements of this specification and the referenced documents, this specification shall take precedence.

2.1. Tyco Electronics Documents

- 109-197: AMP Test Specifications vs EIA and IEC Test Methods
- 501-537: Qualification Test Report
- I 502-1150:Engineering Report

2.2. Commercial Standards

- I BS/EN 61000-4-2: Electromagnetic Compatibility (EMC) - Part 4-2: Testing and Measurement I Techniques - Electrostatic Discharge Immunity Test
- EIA-364: Electrical Connector/Socket Test Procedures Including Environmental Classifications

3. REQUIREMENTS

3.1. Design and Construction

Product shall be of the design, construction and physical dimensions specified on the applicable product drawing.

3.2. Materials

Materials used in the construction of this product shall be as specified on the applicable product drawing.

3.3. Ratings

- Voltage: 3.13 to 3.46 volts DC
- Current: Signal application only
- Temperature: -10 to 70°C
- Humidity: 10 to 90% RH, non-condensing

3.4. Performance and Test Description

Product is designed to meet the electrical, mechanical and environmental performance requirements specified in Figure 1. Unless otherwise specified, all tests shall be performed at ambient environmental conditions per EIA-364.

3.5. Test Requirements and Procedures Summary

Test Description	Requirement	Procedure
Initial examination of product.	Meets requirements of product drawing.	EIA-364-18. Visual and dimensional (C of C) inspection per product drawing.
Final examination of product.	Meets visual requirements.	EIA-364-18. Visual inspection.
ELECTRICAL		
Functional test.	Specimens shall meet requirements	See paragraph 5.
Electrostatic Discharge (ESD), SFP transceiver.	1000 volts maximum.	BS/EN 61000-4-2. Contact and air. See Figure 9.
ESD, SFP transceiver through HSSDC II cable assembly.	500 volts maximum.	BS/EN 61000-4-2. Contact and air. See Figure 10.
MECHANICAL		
Vibration, random.	Using the circuit shown in Figure 4, monitor the LOS line for any state changes during testing. See Note (a).	EIA-364-28, Test Condition VII, Condition D. Subject mated specimens to 3.10 G's rms between 20-500 Hz. 15 minutes in each of 3 mutually perpendicular planes.
Mechanical shock.	Using the circuit shown in Figure 4, monitor the LOS line for any state changes during testing. See Note (a).	EIA-364-27, Method H. Subject mated specimens to 30 G's half-sine shock pulses of 11 milliseconds duration. 3 shocks in each direction applied along 3 mutually perpendicular planes, 18 total shocks.

Figure 1 (cont)

Test Description	Requirement	Procedure
Durability.	See Note (a).	EIA-364-9. Mate and unmate the SFP module to the PCB connector interface of each test specimen for 100 cycles at a maximum rate of 500 cycles per hour.
Mating force, SFP transceiver to PCB connector and SFP cage.	40 N [9 lb] maximum.	EIA-364-13. Measure force necessary to mate specimens at a maximum rate of 12.7 mm [.5 in] per minute.
Unmating force, SFP transceiver from PCB connector and SFP cage.	20 N [4.5 lb] maximum.	EIA-364-13. Measure force necessary to unmate specimens with latches disabled at a maximum rate of 12.7 mm [.5 in] per minute.
Retention, SFP transceiver.	90 N [20.2 lb] minimum. No damage to transceiver below 90 N [20.2 lb].	EIA-364-98. With latch enabled, apply force to failure at a maximum rate of 12.7 mm [.5 in] per minute. See Figure 8.
ENVIRONMENTAL		
Thermal shock.	See Notes (a) and (b).	EIA-364-32. Subject specimens to 5 cycles between -10 and 70°C.
Humidity-temperature cycling.	Using the circuit shown in Figure 4, monitor the LOS line for any state changes during testing. See Note (a).	EIA-364-31, Method III. Subject specimens to 10 cycles (10 days) between 25 and 65°C at 80 to 100% RH.
Temperature life.	Using the circuit shown in Figure 4, monitor the LOS line for any state changes during testing. See Note (a).	EIA-364-17, Method A, Test Condition 2, Test Time Condition C. Subject mated specimens to 70°C for 500 hours.

NOTE

(a) Shall meet visual requirements, show no physical damage, and meet requirements of additional tests as specified in the Product Qualification and Requalification Test Sequence shown in Figure 2.

(b) Functional test shall be conducted at the beginning and end of test group.

Figure 1 (end)

3.6. Product Qualification and Requalification Test Sequence

Test or Examination	Test Group (a)				
	1	2	3	4	5
	Test Sequence (b)				
Initial examination of product	1	1	1	1	1
Functional test	2,7	2,5	2,4	2,4	2,4
ESD, SFP transceiver				3	
ESD, SFP transceiver through HSSDC II cable assembly					3
Vibration	5				
Mechanical shock	6				
Durability	4				
Mating force, SFP transceiver	3				
Unmating force, SFP transceiver	8				
Retention, SFP transceiver	9				
Thermal shock		3			
Humidity-temperature cycling		4			
Temperature life			3(c)		
Final examination of product	10	6	5	5	5

NOTE *(a) See paragraph 4.1.A.*
(b) Numbers indicate sequence in which tests are performed.
(c) Precondition specimens with 10 durability cycles.

Figure 2

4. QUALITY ASSURANCE PROVISIONS

4.1. Qualification Testing

A. Specimen Selection

Specimens shall be prepared in accordance with applicable Instruction Sheets and shall be selected at random from current production. Test groups 1, 2 and 3 shall each consist of 4 specimens Test groups 4 and 5 shall each consist of 5 specimens.

B. Test Sequence

Qualification inspection shall be verified by testing specimens as specified in Figure 2.

4.2. Requalification Testing

If changes significantly affecting form, fit or function are made to the product or manufacturing process, product assurance shall coordinate requalification testing, consisting of all or part of the original testing sequence as determined by development/product, quality and reliability engineering.

4.3. Acceptance

Acceptance is based on verification that the product meets the requirements of Figure 1. Failures attributed to equipment, test setup or operator deficiencies shall not disqualify the product. If product failure occurs, corrective action shall be taken and specimens resubmitted for qualification. Testing to confirm corrective action is required before resubmittal.

4.4. Quality Conformance Inspection

The applicable quality inspection plan shall specify the sampling acceptable quality level to be used. Dimensional and functional requirements shall be in accordance with the applicable product drawing and this specification.

5. FUNCTIONAL TEST

Proper operation shall be verified with the following tests: Receiver Loss of Signal (LOS); Transmit Disable, and: Power On. Figure 3 illustrates the general test setup to be used. Testing at the specified data rates is not included because this testing is considered in a separate engineering evaluation. The serial ID portion is also not included since this is tested in production.

5.1. Equipment

- Signal generator (SG #1): 0 to 2 volts at 100 MHz.
- Power Supply (PS #1): 0 to 5 volts DC at 2 amperes
- Signal generator (SG #2): 0 to 2 volts at 500 Hz
- 4 Channel Digital Storage Oscilloscope with probes
- HSSDC2 Loop Back Connector
- Digital Voltmeter

5.2. Receiver Loss of Signal (LOS)

Figure 5 illustrates the test configuration to be used during this testing. The input power supply will be set to 3.30 volts DC and SG #1 will be adjusted to provide a 1,000 millivolt peak to peak differential signal at 100 MHz to the device under test. Use the oscilloscope to monitor the LOS line and the digital voltmeter to measure the input current (300 milliamperes maximum). The LOS line should be initially low. Remove the Loop-Back connector and verify that the LOS signal goes high. Insert the Loop-Back connector and verify that the LOS changes to its low state.

5.3. Transmit Disable (TX Disable)

Use the circuit shown in Figure 6. Set PS #1 to 3.30 volts DC, SG #1 at 1,000 millivolt differential signal at 100 MHz, and SG #2 at 0 to 2.0 volts at 500 Hz. Use the oscilloscope to monitor RD+, LOS, TX Fault and the TX Disable lines. Input current will be measured using the digital volt meter and R1.

A. TX Disable

1. Verify that the transmitter is “OFF” whenever TX Disable is high and “ON” whenever TX Disable is low.

2. Measure the time from the rising edge (10% level) of TX Disable to when the signal on RD+ stops. This should be no greater than 10 microseconds. Measure the time from the falling edge (90% level) of TX Disable to when the signal on RD+ starts. This should be no greater than 1 millisecond.

B. LOS

1. Measure the time from the end of data at RD+ to the rising edge (90% level) of LOS. This should be not greater than 100 microseconds.

2. Measure the time from the beginning of data at RD+ to the falling edge (10% level) of LOS. This should not be greater than 100 microseconds.

5.4. Power On

Using the circuit in Figure 7, perform the following tests. Set PS #1 to 3.47 volts DC. Apply input voltage to the module under test by closing switch, S1. Using the oscilloscope and R1, measure the peak inrush current. This should be no greater than 330 milliamperes. Also measure the time from when the input voltage reaches 3.13 volts DC and the falling edge (10% level) of TX Fault. This should be no greater than 300 milliseconds.

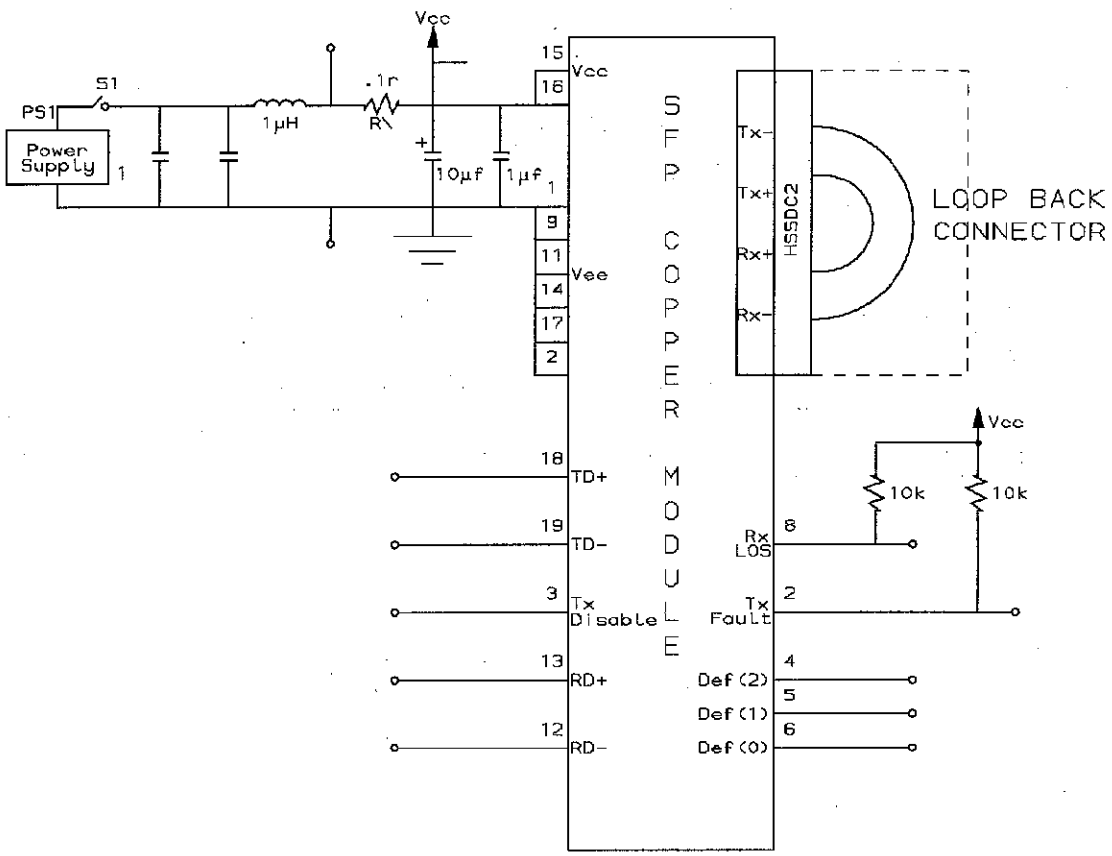

Figure 3
Elements Common to All Functional Tests

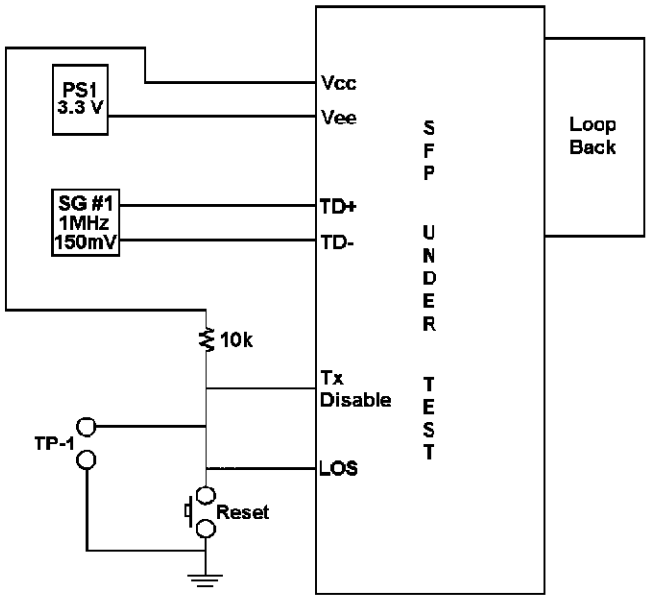

Figure 4
Vibration, Humidity-temperature Cycling and
Temperature Life LOS Monitoring

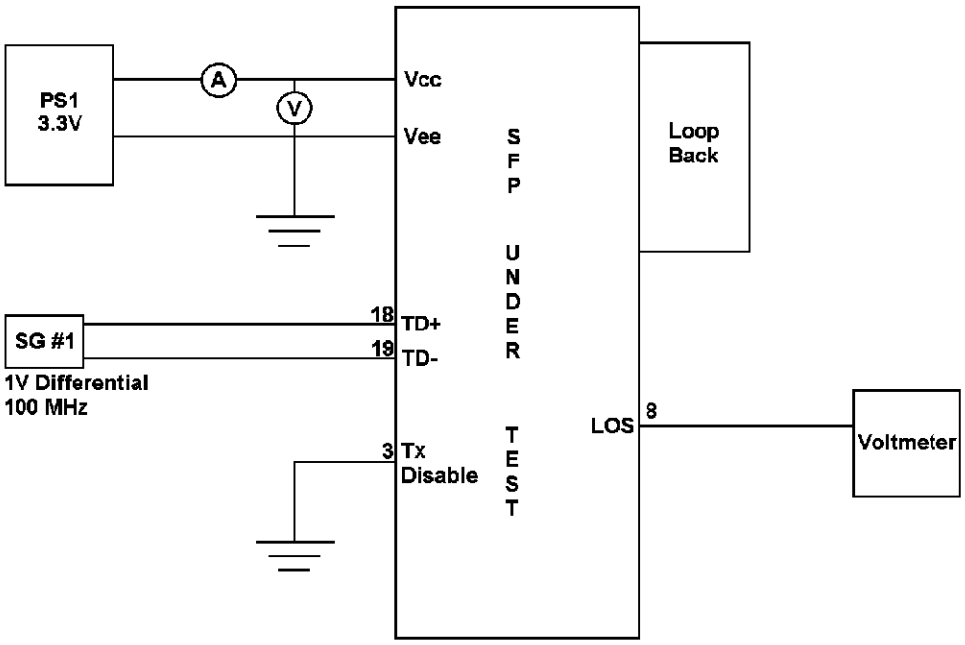

Figure 5
Loss of Signal

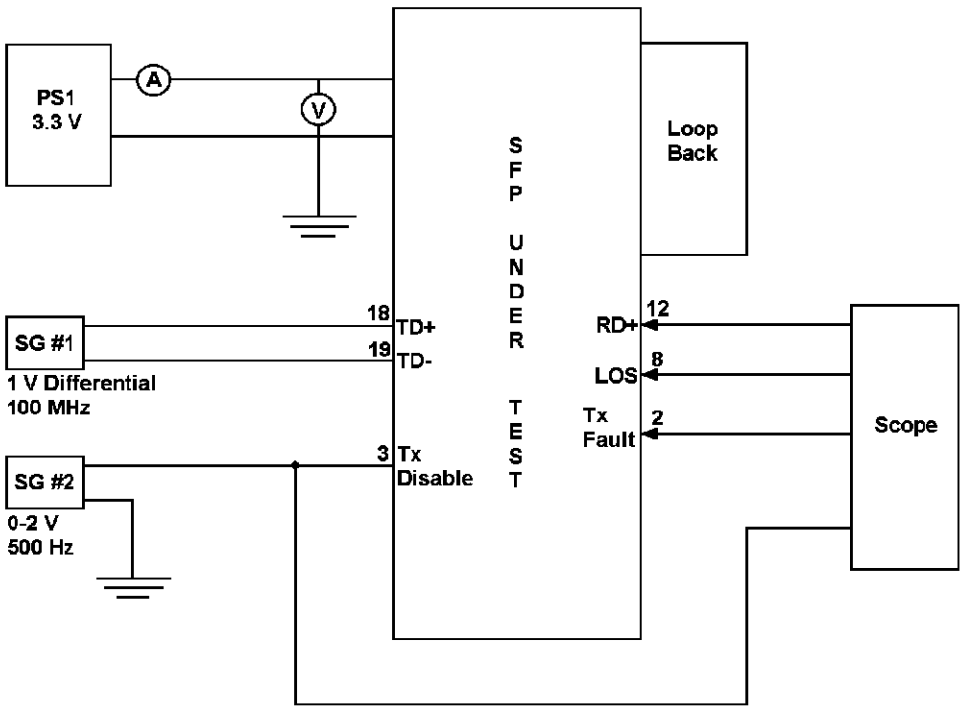

Figure 6
TX Disable

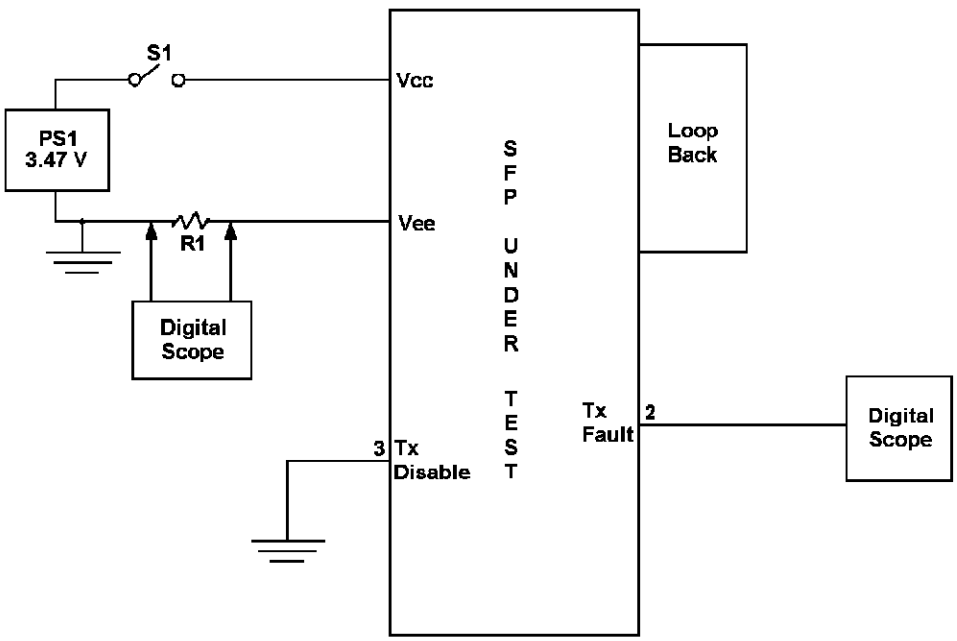

Figure 7
Power On

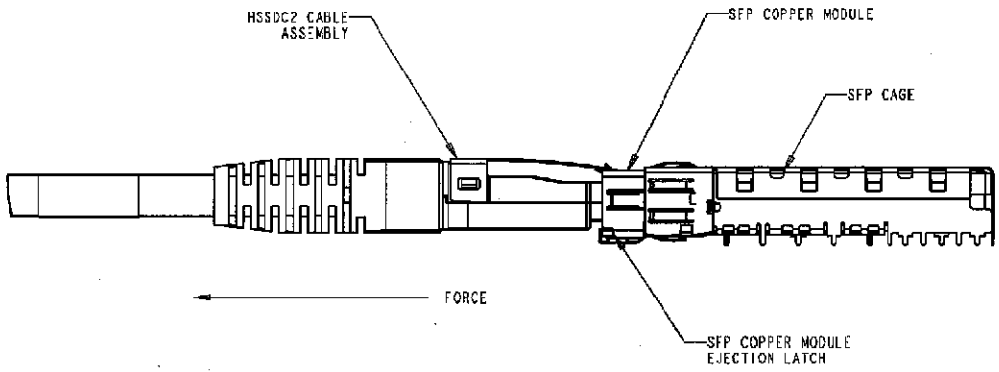

Figure 8
Retention

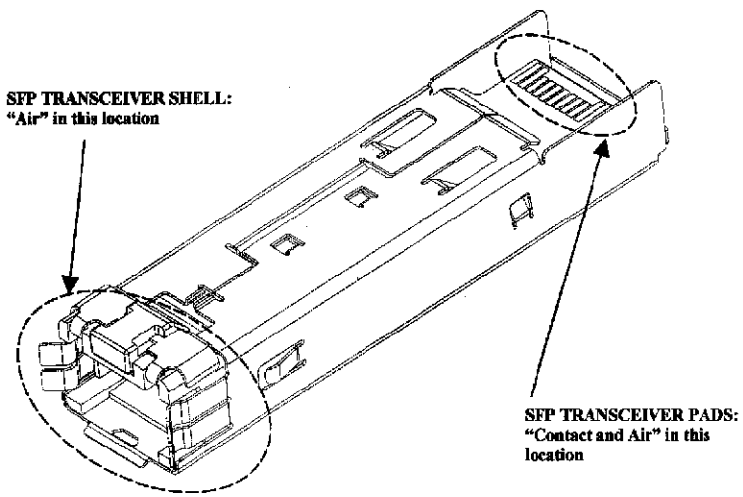

Figure 9
ESD, SFP Transceiver

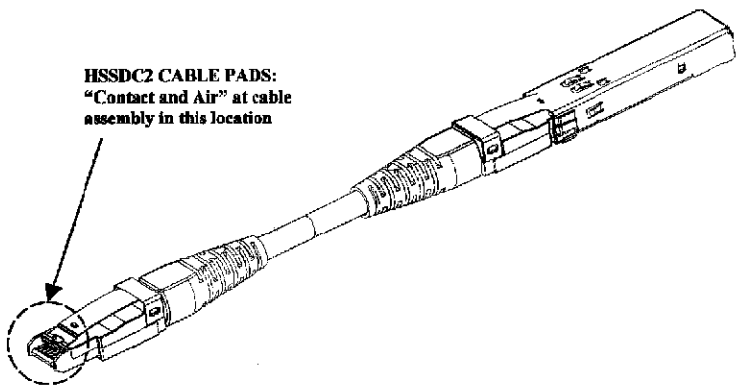

Figure 10
ESD, SFP Transceiver Through HSSDC II Cable Assembly