

65W Peak Power Broadband SPDT

FEATURES

- Low insertion loss
 - o 0.45dB @ 1GHz
- High isolation
 - o 40dB @ 1GHz
- High peak power handling
- No external DC blocking capacitors on RF lines
- Versatile 2.6-5.25V power supply

APPLICATIONS

- TDD Cellular infrastructure
- . LTE relays and microcells

DESCRIPTION

The TS7322K is a symmetrical reflective single pole dual throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 30MHz to 4GHz frequencies makes the TS7322K an excellent switch for all the applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS7322K is packaged into a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.

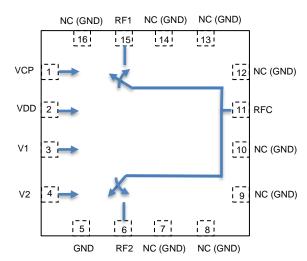


Figure 1: Functional Block Diagram (top view)

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable	
Dase Fait Number	r dekage rype	Form	Quantity	Part Number	
TS7322K	QFN 3 mm x 3 mm	Tape and Reel	3000	TS7322KMTRPBF	

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PIN DESCRIPTION

PIN NUMBER	PIN NAME	DESCRIPTION	
1	VCP	Input Pin. Connecting a SMD Capacitor (or capacitor in parallel with high value resistor) between this pin and ground enable faster switching time	
2	VDD	DC power supply	
3	V1	Switch control input 1	
4	V2	Switch control input 2	
5	GND	Ground	
6	RF2	RF throw 2	
7	NC	This pin is not connected to internal circuit. Connect to PCB ground plane if needed (e.g. coplanar access line)	
8	NC	This pin is not connected to internal circuit. Connect to PCB ground plane if needed (e.g. coplanar access line)	
9	NC	This pin is not connected to internal circuit. Connect to PCB grouplane if needed (e.g. coplanar access line)	
10	NC	This pin is not connected to internal circuit. Connect to PCB grouplane if needed (e.g. coplanar access line)	
11	RFC	RF Common port	
12	NC	This pin is not connected to internal circuit. Connect to PCB grouplane if needed (e.g. coplanar access line)	
13	NC	This pin is not connected to internal circuit. Connect to PCB ground plane if needed (e.g. coplanar access line)	
14	NC	This pin is not connected to internal circuit. Connect to PCB ground plane if needed (e.g. coplanar access line)	
15	RF1	RF throw 1	
16	NC	This pin is not connected to internal circuit. Connect to PCB ground plane if needed (e.g. coplanar access line)	

The backside ground slug of the package must be grounded directly to the ground plane to ensure proper operation

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
Power supply voltage	VDD	2.6 to 5.5	V
Storage temperature Range	T _{st}	-55 to +125	°C
Operating Temperature Range	T _{op}	-40 to +105	°C
RF Input Power CW 450MHz-4GHz (25degC)	RFx	43	dBm
RF Input Power CW <450MHz (25degC)	RFx	42.5	dBm

Exceeding one or a combination of the Absolute Maximum Ratings conditions may cause permanent damage to the device.

SWITCH TRUTH TABLE

V2	V1	RF PATH		
1	0	All OFF state		
0	0	RFC-RF1		
0	1	RFC-RF2		

Note: VDD should be applied first before V1 and V2.

There is an internal pull-down to ground on the V2 control pin: this pin can be left floating when the all OFF state is not used.

There is an internal pull-down to ground on the V1 control pin: default switch state at start-up without any control voltage applied will be RFC-RF1 on.

ELECTRICAL SPECIFICATIONS

Temperature=25°C, VDD=2.7V, 50Ω source and load conditions

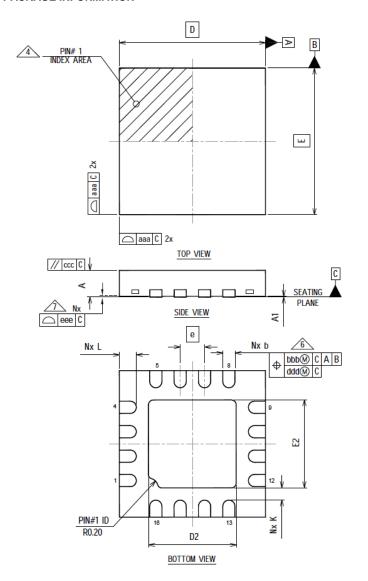
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating frequency		30		4000	MHz
	800MHz	800MHz 0.42			
Insertion loss	1.95GHz		0.55		dB
	2.7GHz		0.65		
	4GHz		0.8		
	800MHz		43		
loolation DEC DEv	1.95GHz		33		dB
Isolation RFC-RFx	2.7GHz 27				
	4GHz		23		
	800MHz		23		
Return Loss RFC, RFx	1.95GHz		25		dB
Retuin Loss RFC, RFX	2.7GHz	2.7GHz 22			
	4GHz		18		
Harmonic distortion					
H2	800MHz, Pin=35dBm		-49		dBm
Н3	800MHz, Pin=35dBm		-50		dBm
IIP3	800MHz		73		dBm
P0.1dB ¹	450MHz – 4000MHz CW signal		44		dBm
P0.1dB ¹	<450MHz CW signal		43		dBm
P0.1dB Peak ²	800MHz Pulsed Signal		48		dBm
Enhanced Switching Time	50% ctrl to 0.1dB of max RF power. C1=1nF (refer to figure 5 schematic)		2.5		μS
	Power Supply VDD	2.6	3.3	5.25	V
Control voltage	V1, V2 ctrl pin V _{ih}	0.67*VDD	VDD	VDD+0.3	V
	All control pin V _{ii}	-0.3		0.3*VDD	V
0	lil, V1 or V2 ctrl voltage =0.3*VDD		0		μА
Control current	lih, V1 or V2 ctrl voltage = VDD			7.5	μА
Current consumption	Active mode (VDD On)		225		μА

Note 1: P0.1dB is a Figure Of Merit.

Note 2: 1% Duty Cycle, 10us pulse width

Note 3: No external DC blocking capacitors required on the RF terminals unless DC voltage is applied on an RF terminal.

PACKAGE INFORMATION



Dimension Table				
Symbol A	V			NOTE
STADO/ S	MINIMUM	NOMINAL	MAXIMUM	
Α	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.20	0.25	0.30	6
D		3.00 BSC		
E		3.00 BSC		
е		0.50 BSC		
D2	1.65	1.80	1.90	
E2	1.65	1.80	1.90	
K	0.20			
L	0.30	0.35	0.40	
aaa		0.05		
bbb		0.10		
CCC	0.10			
ddd		0.05		
eee	0.08			
N	16			3
ND	4			5
NE	4			5
NOTES	1, 2			
LF DWG NO.	B-3490			
REV.	1			

Figure 2: Package drawings

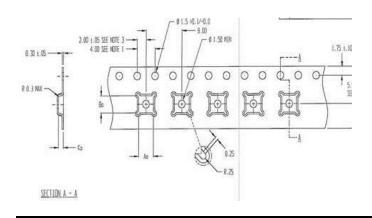


Figure 3: Tape drawing for 3x3mm packages Ao=3.30, Bo=3.30, Ko=1.10

EVALUATION KIT

The board consists of a 4 layer stack with 2 outer layers made of Rogers 4350B (Er = 3.48) and 2 inner layers of FR4 (Er = 4.80). The total thickness of the board is 62 mils (1.57mm). The inner layers provide a ground plane for the 50Ω transmission lines. The thickness between signal and ground plane is 16mils. Each transmission line is designed using coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813mm), gap of 15 mils (0.381mm, and a metal thickness of 1.4mils (0.051mm).

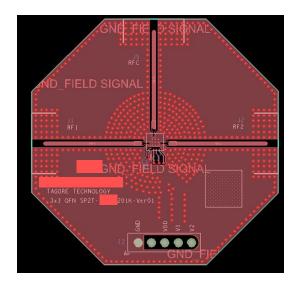


Figure 3: Evaluation board

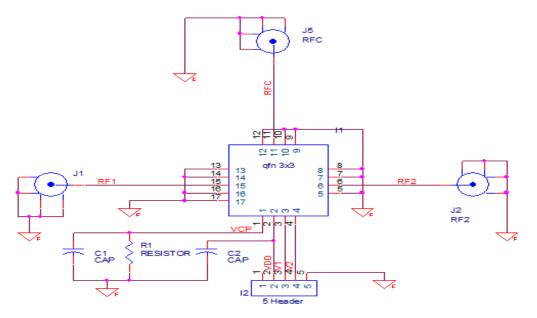


Figure 5: Evaluation board schematic

QUALIFICATION INFORMATION[†]

Qualification Level		Consumer		
Moisture Sensitivity Level		3x3 QFN MSL1		
Human Body Model Class 1A		s 1A		
	Charged Device Model	NA		
RoHS Compliant		Yes		

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