Design Resources

AC/DC Topologies: SpeedFit Examples

Jul 14, 2022

Wolfspeed SpeedFit 2.0 Design Simulator™ is a fast and useful simulation tool that helps the user in designing optimally for their application by quickly comparing different system specifications, topologies, devices and even thermal parameters. It is a user-friendly tool that can be used to estimate the losses, thermal behavior and efficiency of a system and observe important voltage and current waveforms. SpeedFit's features are discussed in more detail here.

SpeedFit 2.0 allows the user to simulate six different single-phase topologies for AC/DC applications (Figure 1). These topologies are active, single-phase boost mode circuits, used for Power Factor Correction (PFC) applications (Figure 2). Designs for PFCs are driven based on low cost and high efficiency. Standards such as 80 PLUS® for efficiency requirements of power supplies and IEEE 519 for harmonic content of power supplies keep getting more stringent. To be compliant with today's efficiency standards, it is required for power supplies to have a highly efficient PFC stage. SpeedFit Simulator provides the capability to evaluate designs using SiC devices for high frequency operation, and configurable Si or SiC diodes for low frequency operation to assist the user in designing their PFC.

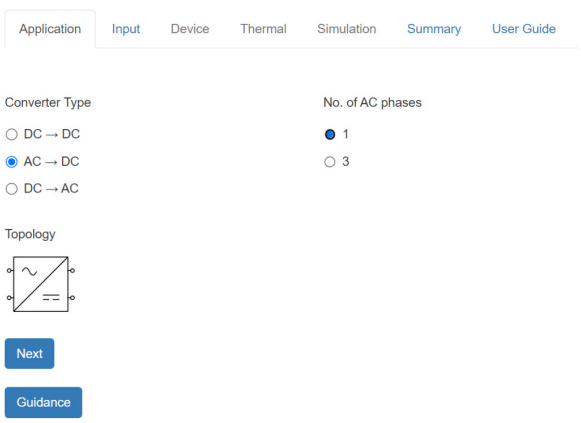


Figure 1: SpeedFit - Application Tab

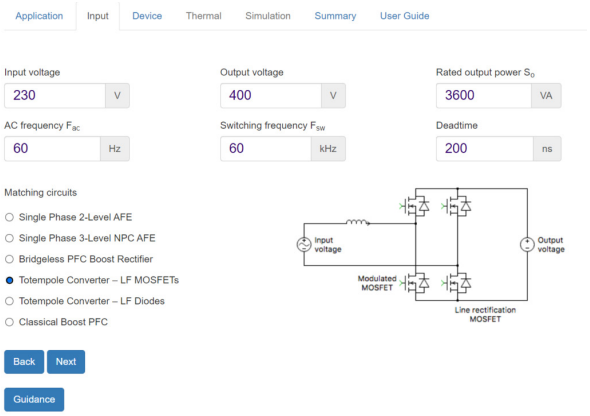


Figure 2: SpeedFit - Input Tab

This article focuses on highlighting how SpeedFit can help in comparing different topologies and assist in designing the most efficient converter using AC/DC applications as example. As an illustration, we compared three different topologies assuming a set of system specifications. These specifications are chosen based on Wolfspeed 3.6 kW Totem-Pole Converter Reference Design. The performance of these topologies for the chosen specifications are presented and compared. These topologies are: Classical Boost Converter, Totem-Pole Converter – LF Diodes, Totem-Pole Converter – LF MOSFETs.

Parameter	Value
Input Voltage	230 V (RMS) – Nominal
Voltage	420 V (DC)
Output Power	3.6 kW – Max
Line Frequency	50 - 60 Hz
Switching Frequency	60 kHz
Inductor Value	0.44 mH
Deadtime	200 ns

Table 1: Specifications from the 3.6 kW Totem-Pole PFC reference design

SpeedFit Parameters

The specifications from Table 1 can be entered in the different tabs in SpeedFit. More information related to the different tabs on SpeedFit is available here. The information given in Table 2 can be used to specify parameters in alignment with the 3.6 kW Totem-Pole Converter reference design.

Tab	Parameter	Value
Input	Input Voltage	230 V
Input	Output Voltage	420 V
Input	Related output power, So	3600 VA
Input	AC Frequency, Fac	60 Hz
Input	Switching Frequency	60 kHz
Input	Deadtime	200 ns
Device	Number of parallel MOSFETs	1
Device	Turn-on gate resistor, $R_{g\text{-}on,ext}$	4.7 Ohm
Device	Turn-off gate resistor, $R_{g\text{-}off,ext}$	2.2 Ohm

Thermal	Thermal interface resistance, $R_{th,ch}$	0.985 K/W
Thermal	Heatsink temperature, T_h	Variable
Thermal	Thermal resistance, $R_{th,ha}$	1.7 K/W
Thermal	Heatsink time constant, τ_{ha}	60
Thermal	Additional heat source on heatsink, P_{add}	0
Thermal	Ambient temperature, T_{amb}	50 °C
Simulation	Inductor, L	0.44 mH
Simulation	Silicon Diode Forward Voltage, V_f	0.92 V
Simulation	Silicon Diode On-Resistance, R_{on}	0.033 Ohms

Table 2: SpeedFit parameters and their values

The thermal parameters are in alignment with the 3.6 W Totem-Pole reference design. The thermal interface resistance, $R_{th,ch} = R_{th,} + R_{th,PCB} + R_{th,TIM}$ = (0.015 + 0.45 + 0.52) K/W = 0.985 K/W.

The heat sink to ambient thermal resistance is 3.4 K/W given in the reference design. However, this applicable to a heatsink for a half-bridge leg. Since we have two such legs, the affective heat sink resistance can be approximated to 1.7 K/W. Therefore, $R_{th,ha}$ = (3.4 / 2) K/W = 1.7 K/W.

In the Simulation tab (Figure 3), the forward voltage drop (V_f) and on-resistance (R_{on}) parameters are provided to include the losses in the rectifier diodes for the efficiency calculations. The user can edit these values based on the rectifier diode they intend to use. These diodes can be Si or SiC diodes. Since these diodes will be operating on low frequency waveforms, they contribute significantly only to the conduction losses. The losses in such devices are shown in the 'Device Overview' table.

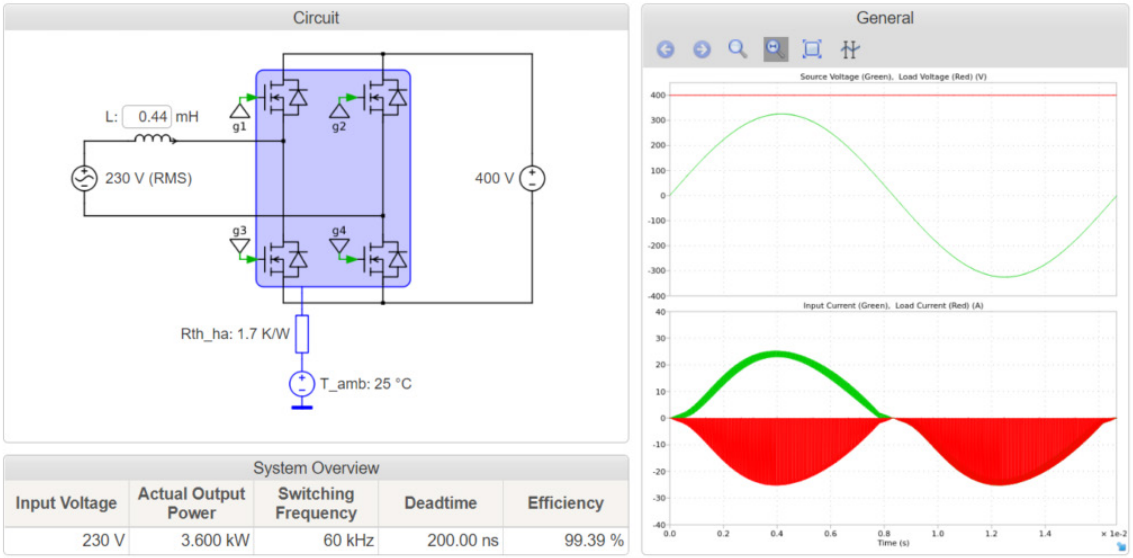


Figure 3: SpeedFit - Simulation Tab

The Summary tab shows a system overview of losses and waveforms. Specifically, for the AC/DC topologies, the rectifier diode losses and LF MOSFETs fields are also included.

Topology Comparison

For illustration in this article, three different PFC topologies are compared. This section contains important notes and observations about these topologies and focuses on how SpeedFit can assist in comparing these different topologies.

Classical Boost PFC

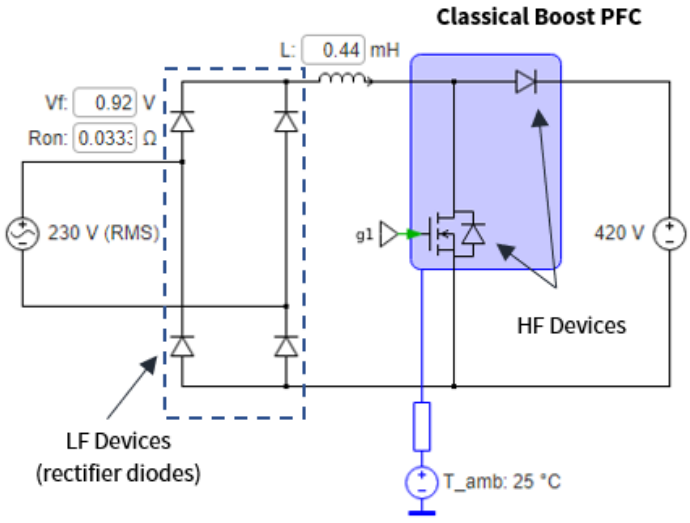


Figure 4: Classical Boost PFC Topology

The Classical Boost topology is comprised of a full-wave rectifier tied to a boost converter. The rectifier diodes do not see

the switching frequency; therefore, Si rectifier diodes can be used for this the rectification stage. However, the current passing through the rectification stage adds only to the conduction losses in the converter. Therefore, the V_f and R_{on} parameters are sufficient to define the losses in these diodes. It can be observed from Figure 6, the rectifier diodes are the least efficient devices, impacting the total efficiency of this topology. Therefore, it is crucial to observe the losses in all the components of a system while evaluating efficiency of a topology. Owing to its lower efficiency, Classical Boost PFCs are appropriate for low-power applications. This topology is appropriate to comply with Silver or Gold 80 Plus Standards.

In SpeedFit, the rectifier diodes are configurable by the user in terms of forward voltage and on-resistance: i.e. V_f and R_{on}. The 'Device Overview' table shown in Figure 6 shows the distribution of losses in the different devices – MOSFET, Diode (boost stage) and rectifier diodes (rectification stage).

Totem-Pole Converter – LF Diodes

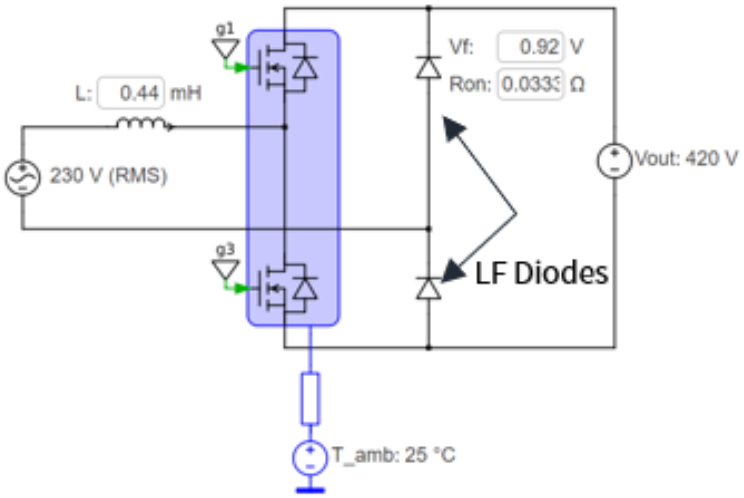


Figure 5: Totem-Pole Converter - LF Diodes Topology

The Totem-Pole Converter with Low Frequency (LF) Diodes is comprised of two MOSFETs operating at the switching frequency and two diodes which see the line frequency waveforms. The users can choose Wolfspeed MOSFETs from the device tab and can configure their diodes based on specifications such as forward voltage (V_f) and R_{on} (On-resistance) of the Si or SiC diodes they intend to use. It is a cost-effective topology with least number of components. It is an improvement over the classical boost PFC since it eliminates the line-frequency rectifier, but slightly less efficient than the Totem-Pole Converter with LF MOSFETs due to higher conduction losses in the rectifier leg.

System Overview				
Input Voltage	Actual Output Power	Switching Frequency	Deadtime	Efficiency
230 V	3.600 kW	60 kHz	—	98.46 %

Device Overview (combined total losses of all devices of a given type)				
	Switching	Conduction	Combined Losses	Peak Junction Temperature
MOSFETs	2.76 W	3.90 W	6.66 W	61.1 °C
Diodes	0 W	7.19 W	7.19 W	69.8 °C
LF MOSFETs (Totempole)	—	—	—	—
Rectifier Diode Losses			41.71 W	
Converter Losses			55.56 W	

Figure 6: Simulation Overview - Classical Boost ConverterTopology

System Overview				
Input Voltage	Actual Output Power	Switching Frequency	Deadtime	Efficiency
230 V	3.600 kW	60 kHz	200.00 ns	98.97 %

Device Overview (combined total losses of all devices of a given type)				
	Switching	Conduction	Combined Losses	Peak Junction Temperature
MOSFETs	2.59 W	13.81 W	16.39 W	71.8 °C
Diodes	—	—	—	—
LF MOSFETs (Totempole)	—	—	—	—
Rectifier Diode Losses			20.57 W	
Converter Losses			36.96 W	

Figure 7: Simulation Overview – Totem-Pole Converter - LF Diodes

System Overview				
Input Voltage	Actual Output Power	Switching Frequency	Deadtime	Efficiency
230 V	3.600 kW	60 kHz	200.00 ns	99.39 %

Device Overview (combined total losses of all devices of a given type)				
	Switching	Conduction	Combined Losses	Peak Junction Temperature
MOSFETs	2.61 W	14.05 W	16.66 W	81.2 °C
Diodes	—	—	—	—
LF MOSFETs (Totempole)	0.00 W	5.13 W	5.13 W	66.1 °C
Rectifier Diode Losses			0 W	
Converter Losses			21.79 W	

Figure 8: Simulation Overview – Totem-Pole Converter - LF MOSFETs

Totem-Pole Converter – LF MOSFETs

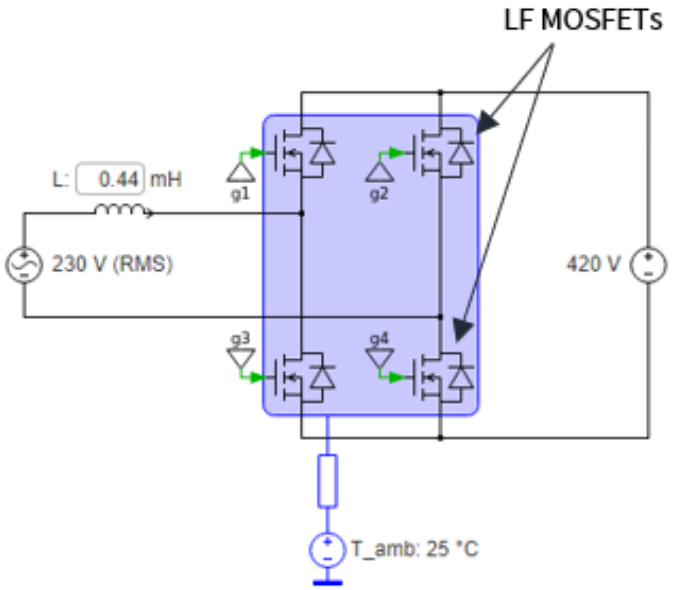


Figure 9: Totem-Pole Converter - LF MOSFETs Topology

The Totem-Pole converter with Low Frequency (LF) MOSFETs employs two High Frequency MOSFETs and two Low Frequency (LF) MOSFETs. This topology does not use any rectifier diodes. The conduction losses incurred in the LF MOSFETs are significantly lower compared to rectifier diodes. Therefore, this is the most efficient topology. However, more gate drivers required here can add to the size and cost of the converter.

Summary

Table 3 summarizes the details of the three topologies in consideration. The devices used are listed in this table and a comparison of the efficiencies is made.

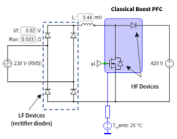
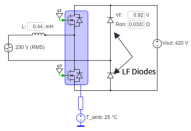
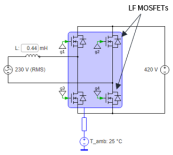
Topology	Classical Boost	Totem-Pole Converter – LF Diodes	Totem-Pole Converter – LF MOSFETs
Circuit Diagram			
MOSFET (HF)	C3M0045065J1	C3M0045065J1	C3M0045065J1
MOSFET - LF	-	-	C3M0015065D
Diodes - HF	C6D20065D	-	-
Rectifier Diode Specs	Vf = 0.92 V, Ron = 0.033 Ω	Vf = 0.92 V, Ron = 0.033 Ω	-
Efficiency (SpeedFit)	98.46 %	98.97 %	99.39 %

Table 3: Comparison between topologies: Classical Boost, Totem-Pole Converter- LF Diodes, Totem-Pole Converter- LF MOSFETs

Note: The peak efficiency (>99%) stated in the reference design for the Totem-Pole Converter – LF MOSFETs includes the losses in the auxiliary power supply and other components of the converter, whereas the efficiency stated above only includes the losses in the power semiconductors.

SpeedFit Simulator 2.0 allows the user to compare different topologies and designs for their applications. It provides the user flexibility to select the optimal SiC MOSFETs and SiC Schottky diodes, and to configure the specifications of low-frequency silicon diodes to help estimate a realistic value of the efficiency of the converter. The System and Device Overview tables, as shown in Figures 6 - 8, on the Simulation tab summarize the losses in the different components like HF MOSFETs, LF MOSFETs, and SiC/Si Rectifier Diodes to conveniently analyze the losses in each device separately and optimize the design.