Silicon Carbide TOLL MOSFETs Enable High Efficiency and High Power Density in 3.6kW Totem-Pole PFC

Yuequan Hu
Manager, Industry Power Applications
Wolfspeed
CONTENTS

1  Introduction and Specifications
2  Topology Selection
3  Power Components and Key Magnetics Selection
4  PCB Layout Considerations
5  Experimental Results
Introduction and Specifications
PFC circuit is a critical stage for power factor correction and low total harmonic distortion

**Where they are used:** Servers, Data centers, Telecom base station, Mining Power, etc.

**Trends:**
- High efficiency for 80 PLUS® Platinum/Titanium, OCP3.0, High efficiency 5G for Carbon-Neutral
- High power density
- Lower system cost
Main changes in Generation 2 from Generation 1

- UPS is decentralized: Load sharing and variability across supplies is not required
- Each unit operates at full load
- High efficiency at full load is critical and required
- AC/DC output changed from 12V to 48VDC (efficiency improved by 1%)
> 99% PFC peak efficiency is required for 80 PLUS Titanium applications

### Typical Efficiency of Server Power Titanium

<table>
<thead>
<tr>
<th>Load(%)</th>
<th>PFC</th>
<th>DC/DC</th>
<th>Unit Eff</th>
</tr>
</thead>
<tbody>
<tr>
<td>0%</td>
<td>91.18%</td>
<td>94.62%</td>
<td>94.90%</td>
</tr>
<tr>
<td>20%</td>
<td>94.90%</td>
<td>96.20%</td>
<td>97.12%</td>
</tr>
<tr>
<td>40%</td>
<td>99.05%</td>
<td>96.20%</td>
<td>96.20%</td>
</tr>
</tbody>
</table>

### 80 Plus test type

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Output/Load</th>
<th>115V non-redundant</th>
<th>115V Industrial</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Star 3.0</td>
<td>multi</td>
<td>93%</td>
<td>90%</td>
</tr>
<tr>
<td></td>
<td>single ≤ 500W</td>
<td>83%</td>
<td>90%</td>
</tr>
<tr>
<td></td>
<td>single &gt; 1000W</td>
<td>83%</td>
<td>90%</td>
</tr>
<tr>
<td></td>
<td>single &gt; 3000W</td>
<td>83%</td>
<td>90%</td>
</tr>
</tbody>
</table>

### 80 Plus Platinum

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Output/Load</th>
<th>115V non-redundant</th>
<th>115V Industrial</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lot 9 (1-Mar -2020)</td>
<td>multi</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td></td>
<td>single</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>Lot 9 (1-Jan -2023)</td>
<td>multi</td>
<td>90%</td>
<td>94%</td>
</tr>
<tr>
<td></td>
<td>single</td>
<td>90%</td>
<td>94%</td>
</tr>
</tbody>
</table>

1. PF not defined under same load as 80 PLUS
2. 100% Load efficiency is 90%, not 91%

https://www.unicomengineering.com/blog/eu-lot-9-update/
OCP3.0 EFFICIENCY CRITERIA

• OCP (Open Compute Project) is an open-design architecture aiming to redesign everything from the data center down to the server to improve energy efficiency, power management, and ease of serviceability.

• Server/datacenter platforms supporting OCP 3.0 are targeting:

  ➢ Power levels > 3kW (with output 48V)
  ➢ High Efficiency (PFC Efficiency Target = ~99%)
  ➢ Small Form Factor
  ➢ Thermally-Efficient Components
  ➢ Lower Cooling Costs
## TYPICAL SPEC OF OCP3.0 RECTIFIER

- Input voltage range: 180V-305VAC rms 50Hz/60Hz
- Output power: 3kW
- Output voltage: 48V DC
- Efficiency: 97.5% pk / **96.5%** at 30%-100% load
- Holdup time: 20 ms
- Operating temperature range: 0 – 55°C

❖ >98.5 efficiency for PFC and around 98% efficiency for DC/DC required at full load
❖ >99% efficiency for PFC and >98.5% efficiency for DC/DC required at half load
❖ To meet these requirements (high efficiency and high power density), selection of circuit topology and power components very critical
High efficiency ➢ How to achieve high power density and low profile (overall height: 40mm)?

High power density/Low profile ➢ How to achieve high efficiency and meet thermal requirement?

Thermal management ➢ How to achieve good EMI performance with compact design?

EMI
### SPECIFICATION OF REFERENCE DESIGN

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage $V_{IN}$</td>
<td>180-265 VAC RMS, 230V nominal</td>
<td>Power derating needed for low line</td>
</tr>
<tr>
<td>Output Voltage $V_{OUT}$</td>
<td>420 VDC max.</td>
<td></td>
</tr>
<tr>
<td>Output Power $P_{OUT}$</td>
<td>3.6 kW max.</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency $f_s$</td>
<td>60kHz</td>
<td></td>
</tr>
<tr>
<td>Peak Efficiency $\eta$</td>
<td>99%</td>
<td>With AUX PSU</td>
</tr>
<tr>
<td>Silicon Carbide MOSFET</td>
<td>*C3M0045065L – HF leg</td>
<td>TOLL package for HF Leg</td>
</tr>
<tr>
<td></td>
<td>C3M0015065D – LF leg</td>
<td>LF can use Si/SiC MOSFET</td>
</tr>
<tr>
<td>Form Factor (W x H x L)</td>
<td>73mm x 40mm x 220mm</td>
<td>Power density: 92W/in$^3$</td>
</tr>
<tr>
<td>Operating Ambient Temperature $T_a$</td>
<td>-40°C to +45°C</td>
<td>Forced air cooling</td>
</tr>
</tbody>
</table>

*Coming Soon*
Topology Selection
TARGET PFC TOPOLOGIES OF SERVER SMPS

Traditional PFC Boost

- Appropriate for low power server SMPS targeting lower 80 PLUS efficiency standards (e.g., Silver, Gold)
- Low VF, high reverse blocking voltage and zero reverse recovery of Wolfspeed C6D 650V Schottky enable high efficiency and high-power density

Bridgeless Totem-Pole PFC

- For HF leg, Si-based MOSFET cannot be used due to slow reverse recovery of body diode
- Low Rds(on) over Temp., robust body diode and lower switching losses of Wolfspeed C3M 650V Silicon Carbide MOSFET enable high efficiency and high-power density
- 80 PLUS Titanium efficiency standards can be achieved
WOLFSPEED 3RD GENERATION 650 V SILICON CARBIDE MOSFET TECHNOLOGY

Wolfspeed’s 650 V Silicon Carbide MOSFETs offer the lowest conduction and switching losses in the industry for users who need smaller, lighter, and highly efficient power conversion in their products.

Design benefits include:
- Low Rds(on) Over Temperature
- Low Parasitic Capacitance
- Fast body with ultra low Qrr

Compared with silicon, our 650 V Silicon Carbide MOSFETs enable:
- 75% lower switching losses
- ½ the conduction losses
- 3x higher power density
### BLOCK DIAGRAM- HIGH EFFICIENCY DESIGN

- **C3M0045065L**
  - TOLL package  C3M™ 650V Silicon Carbide Power MOSFET
- **C3M0015065D**
  - TO-247 package  C3M™ 650V Silicon Carbide Power MOSFET
- **UCC5350**
  - 5A, High Voltage, Isolated Gate Driver with Internal Miller Clamp
- **Si8233BB**
  - 4A, 2.5kV Isolated Dual Channel gate Driver
- **TMS320F280049C**
  - C2000 real-time microcontroller MCU with digital control algorithms
- **MAX13256**
  - 36V H-Bridge Transformer Driver for Isolated Supplies

- Daughter cards for high power density and flexibility
- Low-cost low-profile discrete power supply instead of high-cost off-the-shelf ones

*Coming soon*
DSP offers digital control with powerful computing capability

Flexible control methods can be implemented
Power Components Selection and Daughter Card Design
WOLFSPEED 650 V SILICON CARBIDE POWER MOSFET IN A TOLL (TO LEAD-LESS) PACKAGE

- Low lead inductance enables lower switching losses
- Larger back metal tab enables lower junction temperature
- Ideal for higher switching frequency applications
- 25% smaller footprint as compared to the standard TO-263-7L Package
- Minimum Creepage = 3.15 mm (D-S)
- Ease of automated assembly
- Ideal for ~400VDC applications

Coming Soon!

New TOLL (TO-Leadless) Package
TOLL VS. D2PAK (TO-263-7) QUICK COMPARISONS

- ~ 25% Footprint Reduction
- ~ 50% Height Reduction
- Low Source Inductance
- High Frequency Operation

Drain Tab Area:
- TOLL tab area ~56.3 mm²
- D2Pak-7L tab area ~52.8 mm²

Package Height:
- TOLL Height = 2.20 mm
- D2Pak Height = 4.30 mm

Creepage Distance:
- TOLL 3.5 mm
  (Enough for 650 V Rating)
- D2Pak-7L 7 mm
**SYSTEM LEVEL THERMAL PERFORMANCE OF TOLL VS TO-263-7L PACKAGE**

<table>
<thead>
<tr>
<th>Thermal Performance</th>
<th>Package</th>
<th>TOLL</th>
<th>TO-263-7L</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$T_{j_{\text{max}}}$(°C)</td>
<td>152</td>
<td>175</td>
</tr>
</tbody>
</table>

TOLL Package require less thermal management, granting cost, space, and weight benefits to the application.

**Power – 28 W**

**Convection 5000 W/m²K**
## PRODUCT PORTFOLIO

### Wolfspeed 650V SiC MOSFET

R\(_{\text{DS(on)}}\) = 45 m\(\Omega\), 60 m\(\Omega\), and 120 m\(\Omega\)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Qual.</th>
<th>(V_{BR})</th>
<th>(R_{\text{DS(on)}})</th>
<th>(I_D)</th>
<th>Samples</th>
<th>Package options</th>
</tr>
</thead>
<tbody>
<tr>
<td>C3M0045065L</td>
<td>Industrial</td>
<td>650V</td>
<td>45m(\Omega)</td>
<td>50A</td>
<td>Now</td>
<td>TOLL</td>
</tr>
<tr>
<td>C3M0060065L</td>
<td>Industrial</td>
<td>650V</td>
<td>60m(\Omega)</td>
<td>36A</td>
<td>Now</td>
<td>TOLL</td>
</tr>
<tr>
<td>C3M0120065L</td>
<td>Industrial</td>
<td>650V</td>
<td>120m(\Omega)</td>
<td>23A</td>
<td>Now</td>
<td>TOLL</td>
</tr>
</tbody>
</table>

**Coming Soon!**
HIGH-FREQUENCY HALF-BRIDGE DAUGHTER CARD (30MMX45MMX15MM)

Option A

Adhesive(TIA520R) as TIM for assembling heatsink
- Larger size of heatsink
- One heatsink for HS and LS MOSFET heat dissipation, good to balance the temperature of two MOSFETs
- Additional thermal impedance

- Daughter card for high-frequency leg
- Fully utilize vertical space of power supply
- Increase power density (not taking too much PCB area)
- Easy assembly with double-sided edge connectors
- Quick evaluation of Wolfspeed’s Silicon Carbide MOSFETs
HIGH-FREQUENCY HALF-BRIDGE DAUGHTER CARD (30MMX45MMX15MM)

Daughter Card for High-Frequency Leg
✓ Fully utilize vertical space of power supply
✓ Increase power density (not taking too much valuable PCB area)
✓ Easy assembly with double-sided edge connectors
✓ Quick evaluation of Wolfspeed’s Silicon Carbide MOSFETs

Option B
Directly solder the copper heatsink to PCB
• No additional thermal impedance for TIM between PCB and heatsink
• Separate heatsink for HS and LS MOSFET may cause temperature difference
• The heatsink connected to drain pad of MOSFET (live)
• Difficult to handle high power because of size constraint
THERMAL VIAS FOR HEAT TRANSFER

Via spacing: 0.8mm
Via size: 0.4mm with 2.4mil (60µm) copper plating thickness

- Standard PCB manufacture process
- Cost effective

<table>
<thead>
<tr>
<th>Thermal Impedance</th>
<th>Soldering Heatsink</th>
<th>Adhesive TIM</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\theta,JC}$</td>
<td>0.7</td>
<td>0.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta,solder}$</td>
<td>0.015</td>
<td>0.015</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta,PCB}$</td>
<td>0.45</td>
<td>0.45</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta,TIM}$</td>
<td>0.03</td>
<td>0.52</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta,HA}$</td>
<td>5.3</td>
<td>3.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{\theta, total}$</td>
<td>6.5</td>
<td>5.09</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
High Frequency Half-Bridge Power Stage and Gate Drive Circuit

- **UCC5350MC** as gate driver
  - Active miller clamp
  - 5A sink and source current
  - 100V/nS minimum CMTI
- Separate Rg_on and Rg_off to control ON and OFF speed conveniently
GATE DRIVE BIAS CIRCUITS

HF HS Gate Bias

HF/LF LS Gate Bias

LF HS Gate Bias

- +15V/-3V gate power supply voltage
- Separate gate drive power supply for high-side and low-side MOSFETs
- Small surface mount transformer with high frequency enables compact design of daughter card
Key Magnetics Selection
## Parameters and Performance Comparison – PFC Choke

<table>
<thead>
<tr>
<th></th>
<th>KH106-060A</th>
<th>KAM106-060A</th>
<th>NPC106060</th>
<th>NPA106060</th>
<th>NPN-LH106060</th>
</tr>
</thead>
<tbody>
<tr>
<td>Permeability</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>60</td>
</tr>
<tr>
<td>Pv(100mT @50kHz)</td>
<td>300kW/m³</td>
<td>200kW/m³</td>
<td>150kW/m³</td>
<td>150kW/m³</td>
<td>200kW/m³</td>
</tr>
<tr>
<td>DC Bias (@100 Oe)</td>
<td>80%</td>
<td>68%</td>
<td>70%</td>
<td>55%</td>
<td>85%</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>&lt;200kHz</td>
<td>&lt;200kHz</td>
<td>&lt;200kHz</td>
<td>&lt;300kHz</td>
<td>&lt;200kHz</td>
</tr>
<tr>
<td>Vendor</td>
<td>KDM</td>
<td>KDM</td>
<td>POCO</td>
<td>POCO</td>
<td>POCO</td>
</tr>
</tbody>
</table>

- Trade-off between core loss and DC bias
- NPN-LH material selected for its low core loss and best DC bias
- DC bias capability and loss data of POCO can be seen at [http://pocomagnetic.com/html/2020/03/02/202003021053158007732711.html](http://pocomagnetic.com/html/2020/03/02/202003021053158007732711.html)
**TRANSFORMER FOR GATE BIAS VOLTAGES**

Gate drive bias PS with discrete parts

- Low profile (6.35mm vs. 12.5mm, lower height ≤ 4mm achievable)
- Good for airflow
- SM facilitates automated assembly

Off-the-shelf gate drive bias PS

- Tall (12.5mm)
- Great impact on airflow and thermal
- Not suitable for SM/automated assembly
PCB Layout Considerations
HIGH DV/DT NODE AND HIGH DI/DT LOOP

- Keep the sensitive signals far away from the high dv/dt, di/dt trace/nodes
- Keep the sensitive signals far away from the high magnetic field such as PFC inductor.
- Place ceramic or film caps as close as possible to minimize the high frequency di/dt loop.
- Proper PCB layout of the power components to minimize the high frequency di/dt loop.
PARASITIC CAPS OF PCB

\[ C = \frac{\varepsilon_r S}{4\pi kd} \]

\[ \frac{1}{4\pi k} = 8.85 \times 10^{-12} \text{ F/m} \]

\[ \varepsilon_r \text{ of FR4 } \rightarrow 4.3 \]

\[ d = 0.0001 \text{ m} \]

For 1 cm \(^2\) PCB trace overlap:

\[ C = 4.3 \times 0.01 \times 0.01 \times 8.85 \times 10^{-12} / 0.0001 = 38 \text{ pF} \]

\[ P_c = 0.5 \times C \times f \times V^2 = 0.22 \text{ W for 440Vbus hard switching @60 kHz} \]

- Minimize overlapping of traces which can generate undesired power losses
COMPONENTS PLACEMENT FOR MAIN BOARD

- Cooling Fan
- EMI filter and inrush current limit
- Keep output away from input
- Keep control board away from PFC choke
- HF daughter card and LF bridge
- Aux PS and control board

Output Cap 1
Output Cap 2
VDC
COMPONENTS PLACEMENT ON HF DAUGHTER CARD

- Separate gate drive, bias PS from power loop/traces to avoid overlap
- Place the gate drivers near MOSFETs
- No overlap between Drain and Source traces, Drain and Gate to reduce the parasitic capacitance coupling
- Place ceramic caps as close as possible to minimize the high di/dt loop
Experimental results
WOLFSPEED 3.6KW TOTEM-POLE PFC WITH SILICON CARBIDE

Control card with TI DSP
Daughter card with SiC MOSFETs C3M0045065L

Dimension: 220mmX73mmX40mm

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage $V_{IN}$</td>
<td>180-265 VAC RMS, 230V nominal</td>
<td>Power derating needed for low line</td>
</tr>
<tr>
<td>Output Voltage $V_{OUT}$</td>
<td>420 VDC max.</td>
<td></td>
</tr>
<tr>
<td>Output Power $P_{OUT}$</td>
<td>3.6 kW max.</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency $f_s$</td>
<td>60kHz</td>
<td></td>
</tr>
<tr>
<td>Peak Efficiency $\eta$</td>
<td>99%</td>
<td></td>
</tr>
<tr>
<td>Silicon Carbide MOSFET</td>
<td>C3M0045065L – HF leg</td>
<td>TOLL package for HF Leg</td>
</tr>
<tr>
<td></td>
<td>C3M0015065D – LF leg</td>
<td></td>
</tr>
<tr>
<td>Form Factor (W x H x L)</td>
<td>73mm x 40mm x 220mm</td>
<td>Power density: 92W/in$^3$</td>
</tr>
<tr>
<td>Operating Ambient Temperature $T_a$</td>
<td>-40°C to +45°C</td>
<td>Forced air cooling</td>
</tr>
</tbody>
</table>
Over 99% efficiency achieved at half load even with Aux PS
POWER FACTOR AND THD AT 230V INPUT

At nominal input 230V
- PF > 0.96 at 10% load
- PF > 0.99 at half load
- PF > 0.995 at full load

At nominal input 230V
- THD < 10% load
- THD < 4% at half load
- THD < 2% at full load
CAPTURED WAVEFORMS

Test Condition: Vin=230V/50Hz, Vo = 400V, full load

\[ v_{in} \]: Input voltage [500V/div]
\[ i_{in} \]: Input current [20A/div]
\[ i_L \]: Inductor current [20A/div]
CAPTURED SWITCHING WAVEFORMS

Test Condition: Vin=230V/50Hz, Vo = 400V, full load

Gate drive signals within specified limits
## THERMAL RESULT (adhesive as TIM)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>180Vac Input 400Vdc output 3600W</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High side MOSFET</td>
<td>13.38</td>
<td>82.5</td>
<td>94.27</td>
<td>175</td>
<td>135</td>
<td>Pass</td>
</tr>
<tr>
<td>Low side MOSFET</td>
<td>13.38</td>
<td>85</td>
<td>96.77</td>
<td>175</td>
<td>135</td>
<td>Pass</td>
</tr>
</tbody>
</table>

| **230Vac Input 400Vdc output 3600W (adhesive as TIM)** |                               |                        |                              |                               |                          |          |
| High side MOSFET         | 8.24                          | 63.5                   | 70.75                        | 175                           | 135                      | Pass     |
| Low side MOSFET          | 8.24                          | 62                     | 69.25                        | 175                           | 135                      | Pass     |

**Balanced thermal**
### THERMAL RESULT (soldered copper heatsink)

<table>
<thead>
<tr>
<th></th>
<th>Calculated Power loss (Watts)</th>
<th>Measured Case Temp (°C)</th>
<th>Calculated Junction Temp (°C)</th>
<th>Max. Junction Temperature (°C)</th>
<th>Derating Requirement (°C)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>180Vac Input 400Vdc output 3300W</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High side MOSFET</td>
<td>13.38</td>
<td>108</td>
<td>117.57</td>
<td>175</td>
<td>135</td>
<td>Pass</td>
</tr>
<tr>
<td>Low side MOSFET</td>
<td>13.38</td>
<td>95.6</td>
<td>105.17</td>
<td>175</td>
<td>135</td>
<td>Pass</td>
</tr>
<tr>
<td><strong>230Vac Input 400Vdc output 3600W (soldered copper heatsink)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High side MOSFET</td>
<td>8.24</td>
<td>83.5</td>
<td>90.75</td>
<td>175</td>
<td>135</td>
<td>Pass</td>
</tr>
<tr>
<td>Low side MOSFET</td>
<td>8.24</td>
<td>67</td>
<td>74.25</td>
<td>175</td>
<td>135</td>
<td>Pass</td>
</tr>
</tbody>
</table>

**Unbalanced thermal**
SUMMARY

- 80 PLUS Platinum/Titanium efficiency standards require new topologies and advanced power devices to be used for server and data center power supplies.

- A 3.6kW high-efficiency high-power-density Totem-pole PFC with Wolfspeed 650V SiC TOLL devices designed and tested to meet 80 Plus efficiency and OCP form factor requirements.

- A peak efficiency of over 99% at half load and an efficiency of over 98.5% at full load achieved even with Aux PS.

- TOLL package enabled small form factor PCB design with an ease in thermal management.

- Thermal vias with high-performance adhesive proved to be a cost-effective thermal solution.

- Design challenges and general design guidelines introduced in this work.

- Wolfspeed 650V SiC Power MOSFETs in TOLL package has opened the door to high-efficient and high-power-density power supplies.