

This version (15 May 2020 22:22) was **approved** by Eileen.
The Previously approved version (15 May 2020 22:21) is available.

Quick Start Guide for Testing the AD9213/9217 ADC Evaluation Board Using the ADS8-V1EBZ FPGA-Based Capture Board

Typical Setup

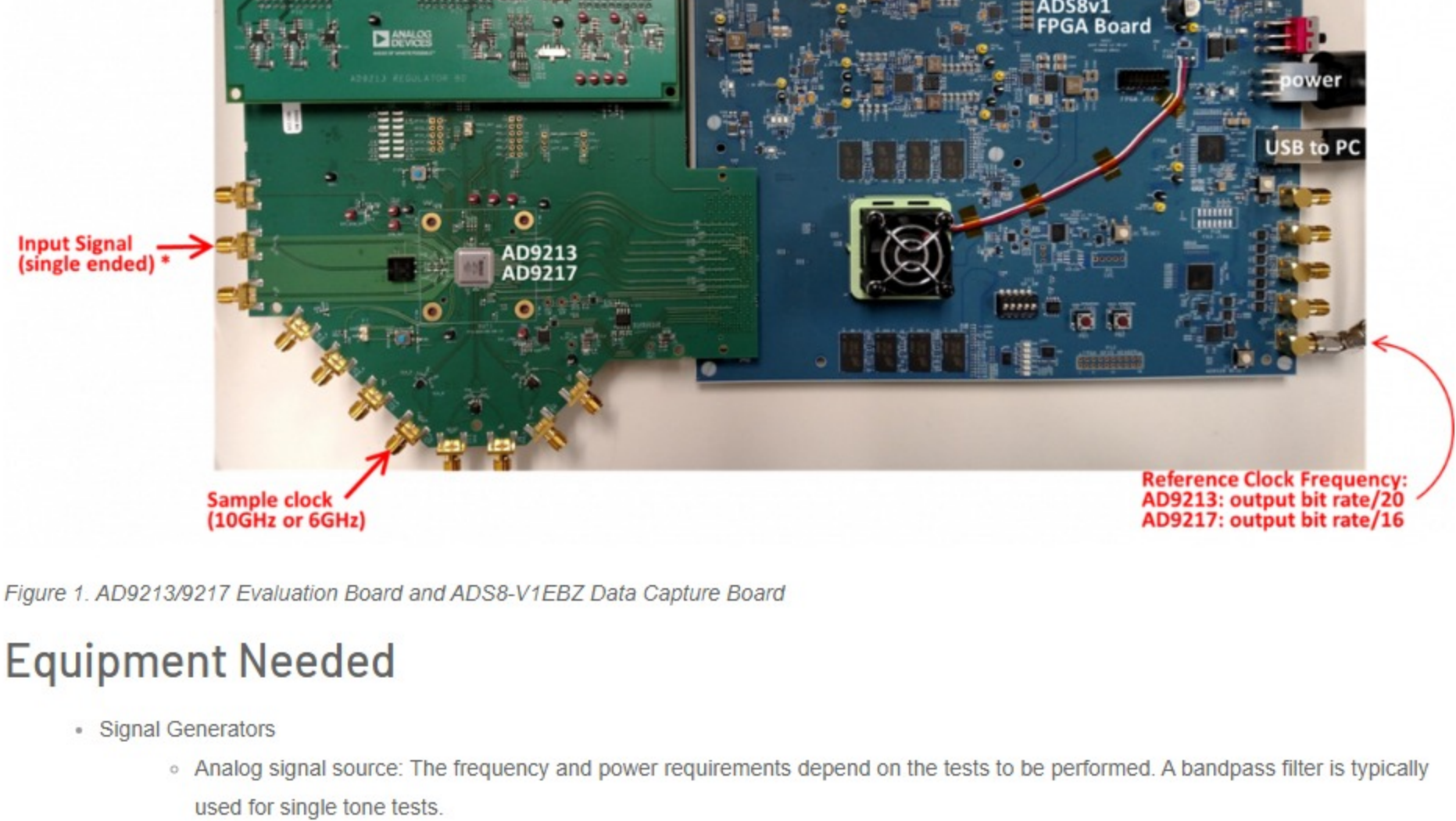


Figure 1. AD9213/9217 Evaluation Board and ADS8-V1EBZ Data Capture Board

Equipment Needed

- Signal Generators
 - Analog signal source: The frequency and power requirements depend on the tests to be performed. A bandpass filter is typically used for single tone tests.
 - Analog clock source: The clock signal generator should have very low phase-noise and be capable of supplying a 10GHz clock signal (or 6 GHz clock signal for the 6Gsp/s speed grade of AD9213) at approximately 10dBm.
 - Reference clock source: For AD9213-10GEBZ with 16 output lanes (at 10Gsp/s), the frequency of REFCLK is 625MHz. For AD9213-6EBZ configured for 8 output lanes (at 6Gsp/s), the frequency of REFCLK is 750MHz. For AD9213, the frequency of REFCLK is the digital output lane rate divided by 20. For AD9217, the frequency of REFCLK is the sample rate divided by 16, which is the same as digital output data rate divided by 16.
- PC running Windows®
- USB port and cable to connect to a PC
- AD9213/9217 Evaluation Board
- AD9213/9217 Regulator Board (supplies power to the ADC Board)
- ADS8-V1EBZ FPGA Based Data Capture Board with a power supply

Helpful Documents

- AD9213 Data Sheet
- ACE Manual: http://swdownloads.analog.com/ACE/ACE_User_Manual_rev3.pdf

Software Needed

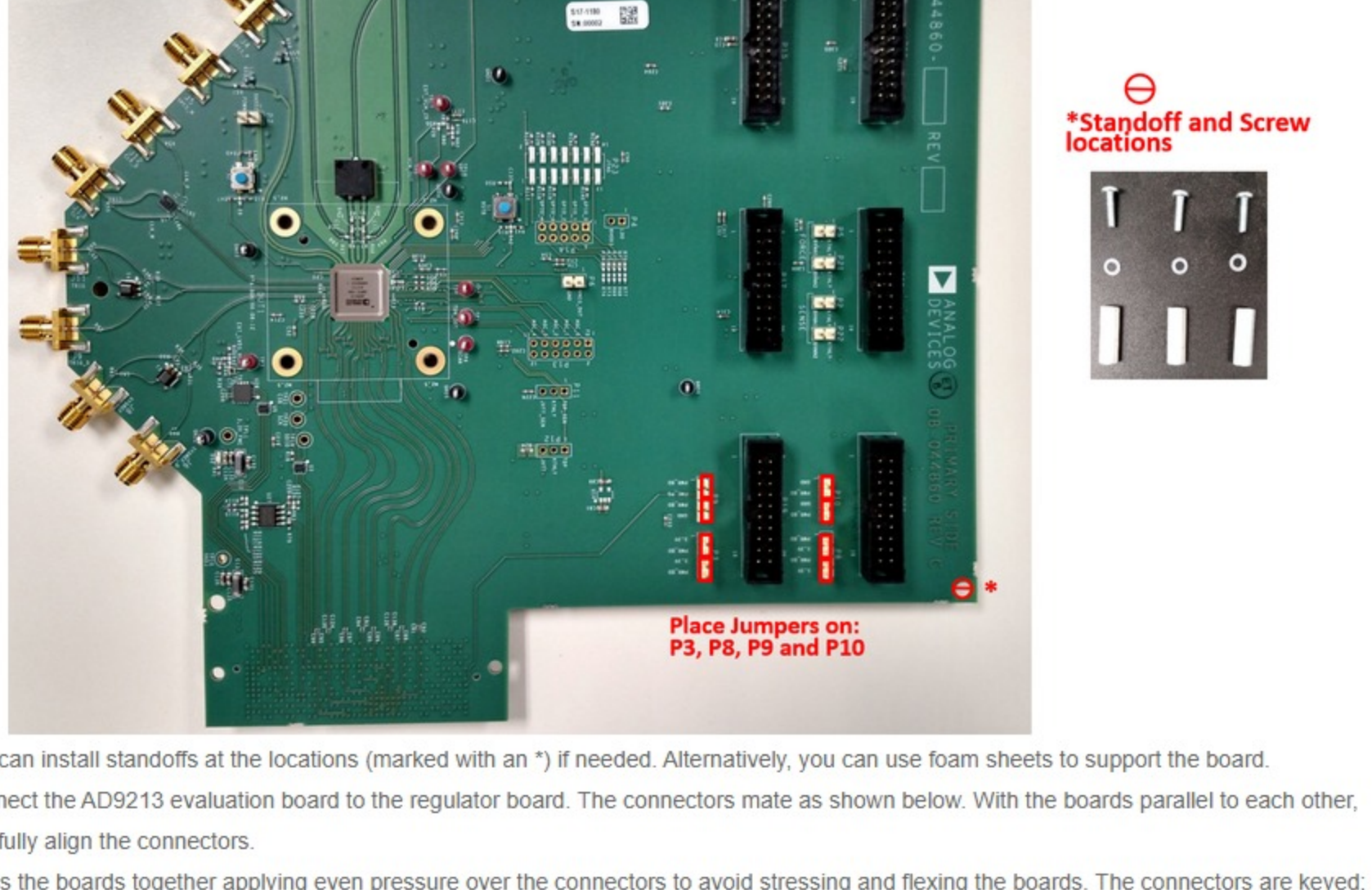
- Analysis Control Evaluation (ACE) software: available at <http://www.analog.com/en/design-center/evaluation-hardware-and-software/ace-software.html>
- ACE <https://wiki.analog.com/resources/tools-software/ace>

Board Design and Integration Files

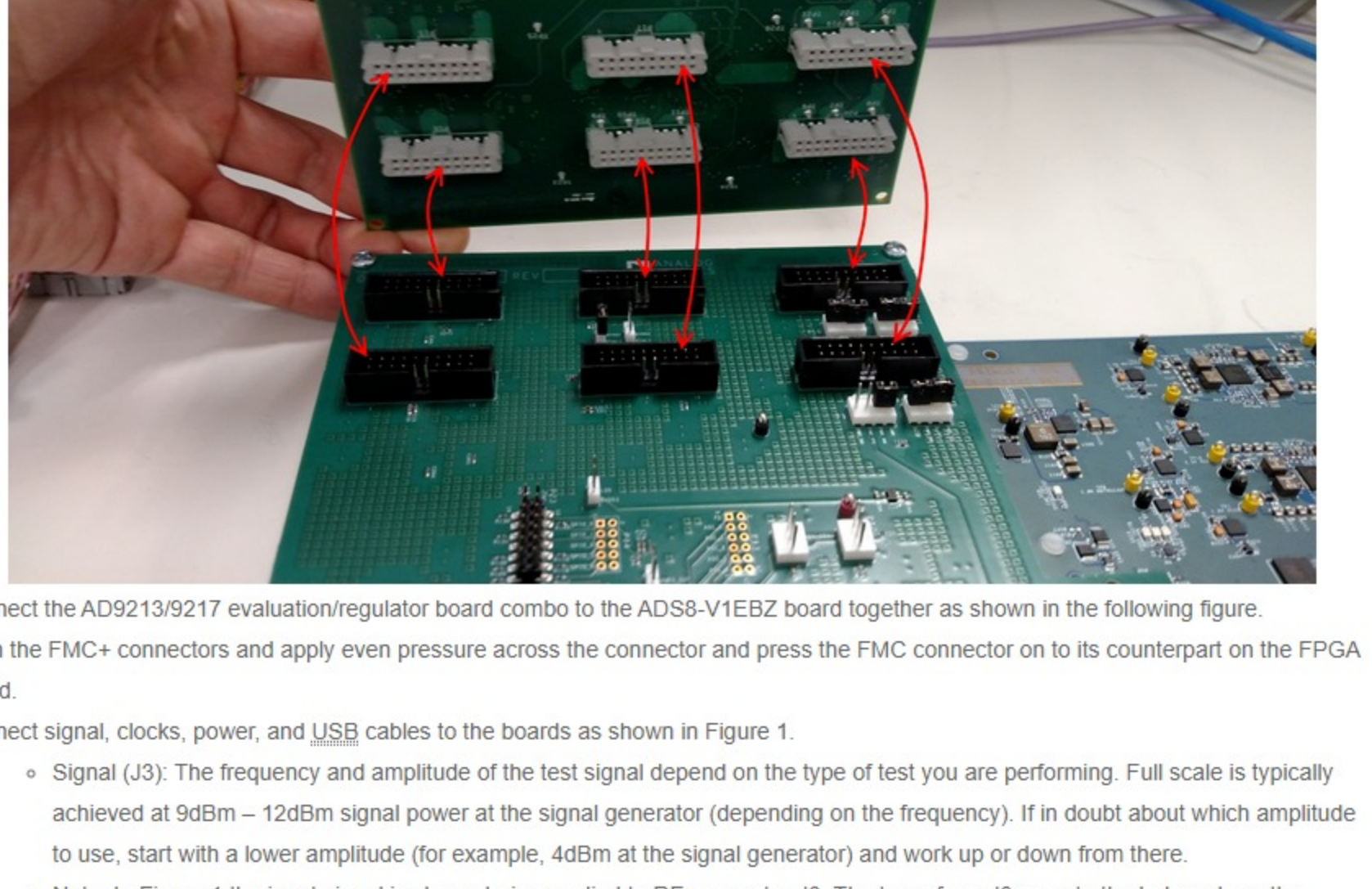
- Schematics for ADC board and regulator board
- Gerber Layout files for ADC board
- Gerber Layout files for regulator board
- Bill of materials for ADC board
- Bill of Materials for regulator board

Testing

- Install the ACE software. The installer is located at <http://www.analog.com/en/design-center/evaluation-hardware-and-software/ace-software.html>. The Start page appears after you complete the installation and open ACE. The Start page displays released plugins. Ensure that the AD9213/9217 plugin appears in the pre-installed list of released plugins.
- If the AD9213/9217 plugin does not appear in the pre-installed list, it is also available here: <https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/EVAL-AD9213.html#web-related-software>
- Close ACE.
- Install jumpers on P3, P6, P9, P10 as shown below.



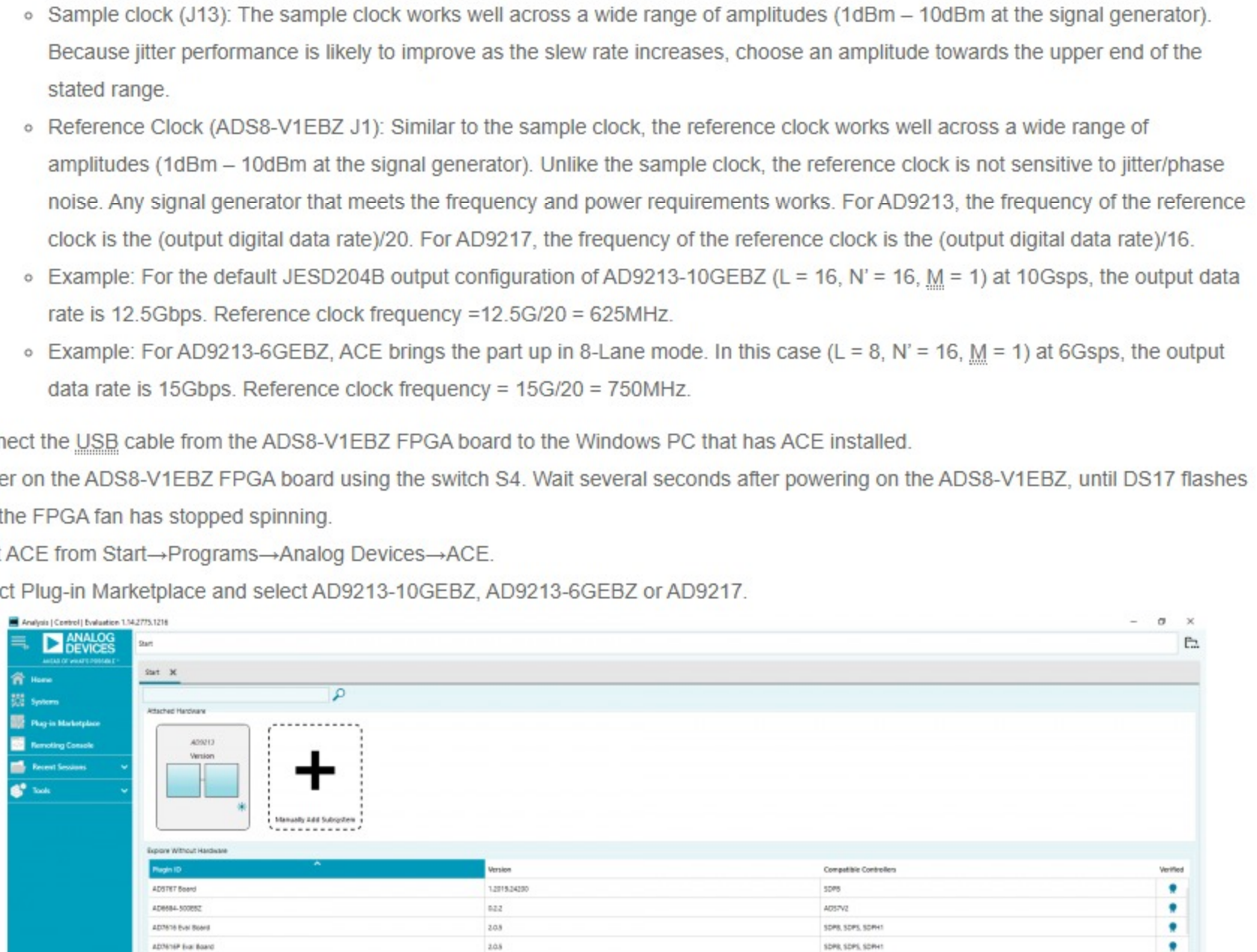
- You can install standoffs at the locations (marked with an *) if needed. Alternatively, you can use foam sheets to support the board.
- Connect the AD9213/9217 evaluation board to the regulator board. The connectors mate as shown below. With the boards parallel to each other, carefully align the connectors.
- Press the boards together applying even pressure over the connectors to avoid stressing and flexing the boards. The connectors are keyed, therefore, you cannot insert the board with the incorrect orientation.



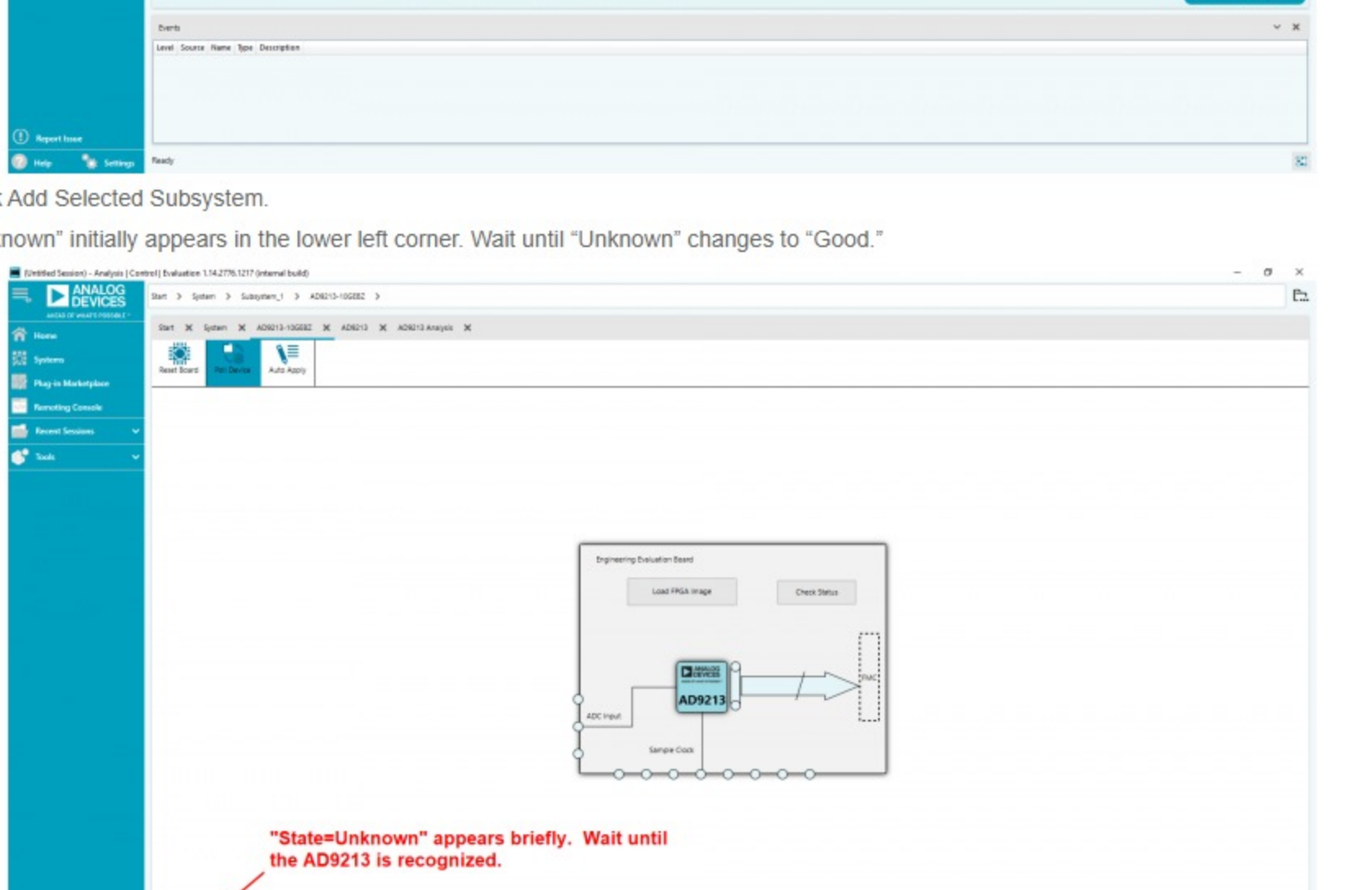
- Connect signal, clocks, power, and USB cables to the boards as shown in Figure 1.
- Signal (J3): The frequency and amplitude of the test signal depend on the type of test you are performing. Full scale is typically achieved at 9dBm – 12dBm signal power at the signal generator (depending on the frequency). If in doubt about which amplitude to use, start with a lower amplitude (for example, 4dBm at the signal generator) and work up or down from there.
- Note: In Figure 1 the input signal is shown being applied to RF connector J3. The trace from J3 goes to the balun where the single-ended signal is converted to differential. On some board revisions the trace to the balun comes from RF connector J2. In these cases, the input signal must be applied to J2.

- Sample clock (J13): The sample clock works well across a wide range of amplitudes (1dBm – 10dBm at the signal generator). Because jitter performance is likely to improve as the slew rate increases, choose an amplitude towards the upper end of the stated range.
- Reference clock (ADS8-V1EBZ J1): Similar to the sample clock, the reference clock works well across a wide range of amplitudes (1dBm – 10dBm at the signal generator). Unlike the sample clock, the reference clock is not sensitive to jitter/phase noise. Any signal generator that meets the frequency and power requirements works. For AD9213, the frequency of the reference clock is the (output digital data rate)/20. For AD9217, the frequency of the reference clock is the (output digital data rate)/16.
- Example: For the default JESD204B output configuration AD9213-10GEBZ (L = 16, N = 16, M = 1) at 10Gsp/s, the output data rate is 12.5Gsp/s. Reference clock frequency = 12.5G/20 = 625MHz.
- Example: For AD9213-6GEBZ, ACE brings the part up in 8-Lane mode. In this case (L = 8, N = 16, M = 1) at 6Gsp/s, the output data rate is 15Gsp/s. Reference clock frequency = 15G/20 = 750MHz.

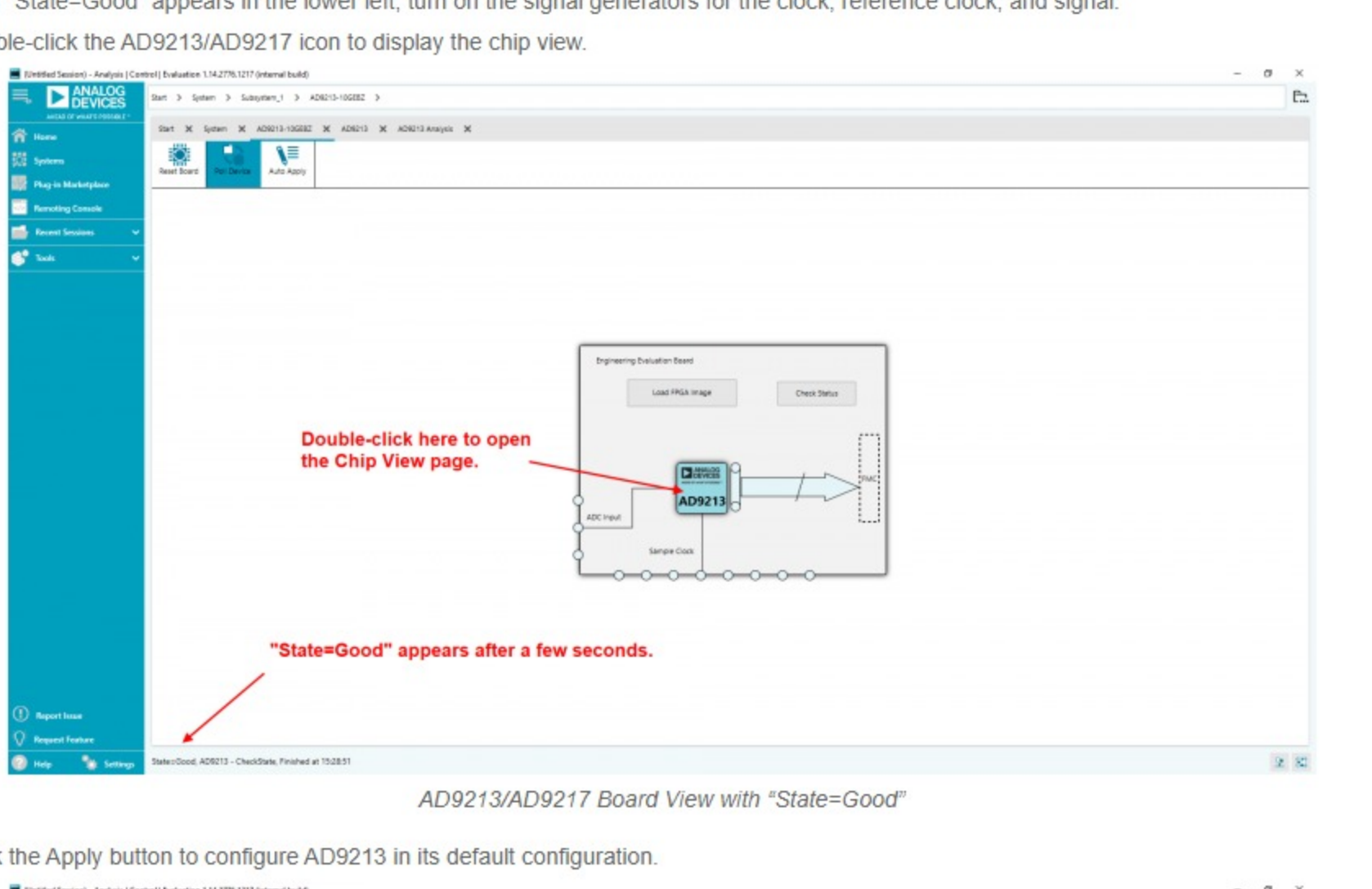
- Connect the USB cable from the ADS8-V1EBZ FPGA board to the Windows PC that has ACE installed.
- Power on the ADS8-V1EBZ FPGA board using the switch S4. Wait several seconds after powering on the ADS8-V1EBZ, until DS17 flashes and the FPGA fan has stopped spinning.
- Start ACE from Start—Programs—Analog Devices—ACE.
- Select Plug-in Marketplace and select AD9213-10GEBZ, AD9213-6GEBZ or AD9217.



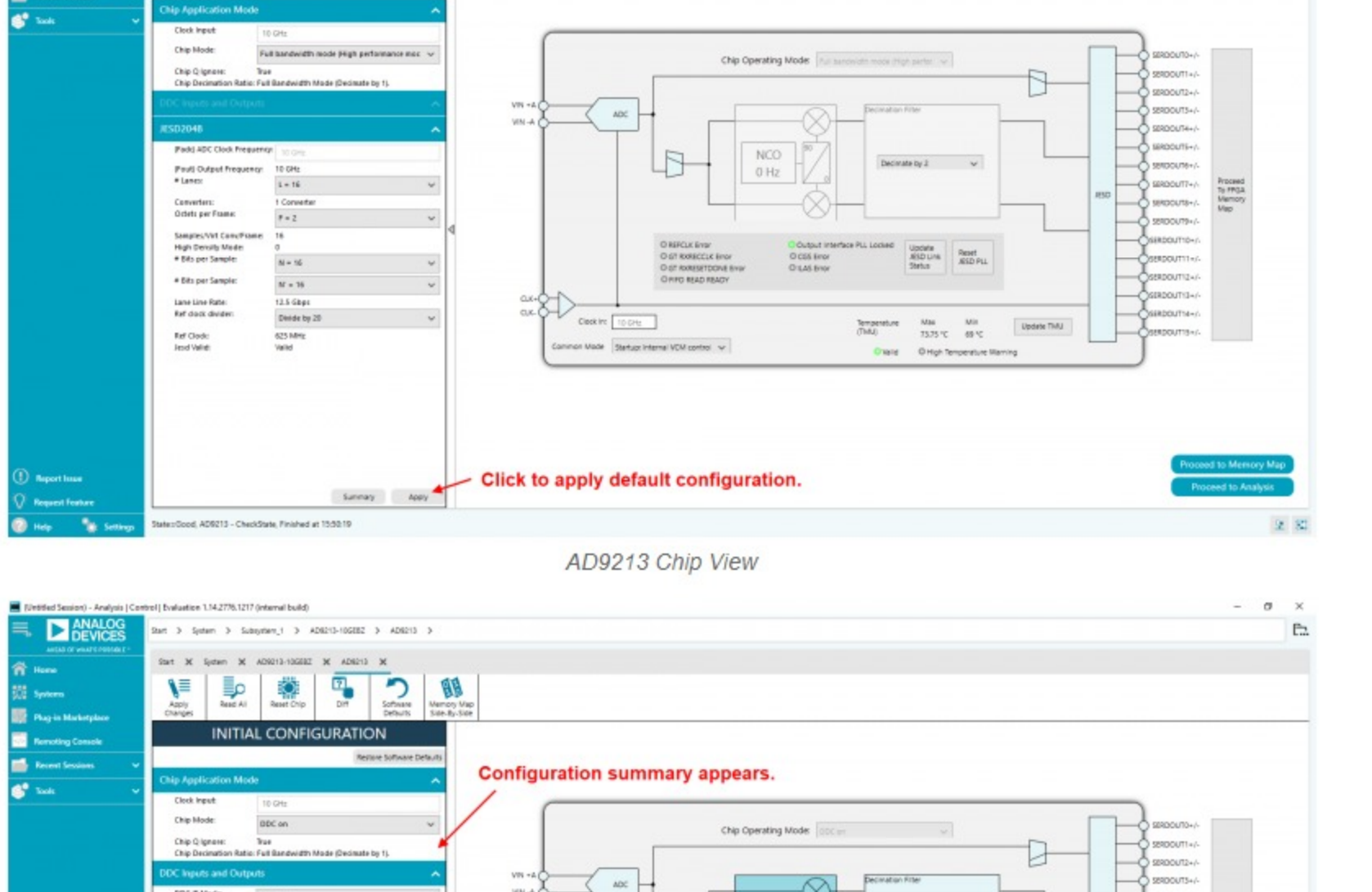
- Click Add Selected Subsystem.
- 'Unknown' initially appears in the lower left corner. Wait until 'Unknown' changes to 'Good.'



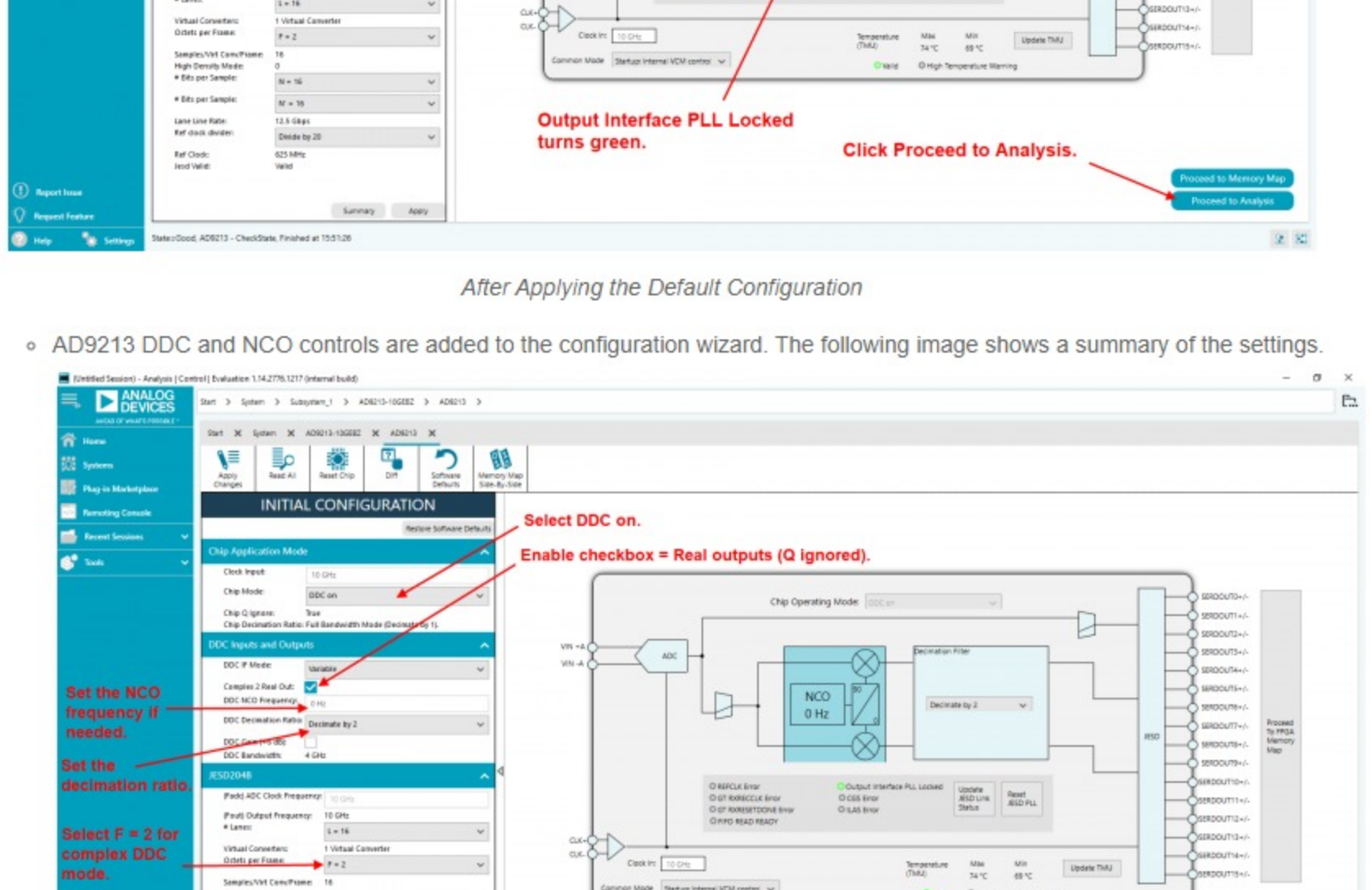
- Click the Apply button to configure AD9213 in its default configuration.



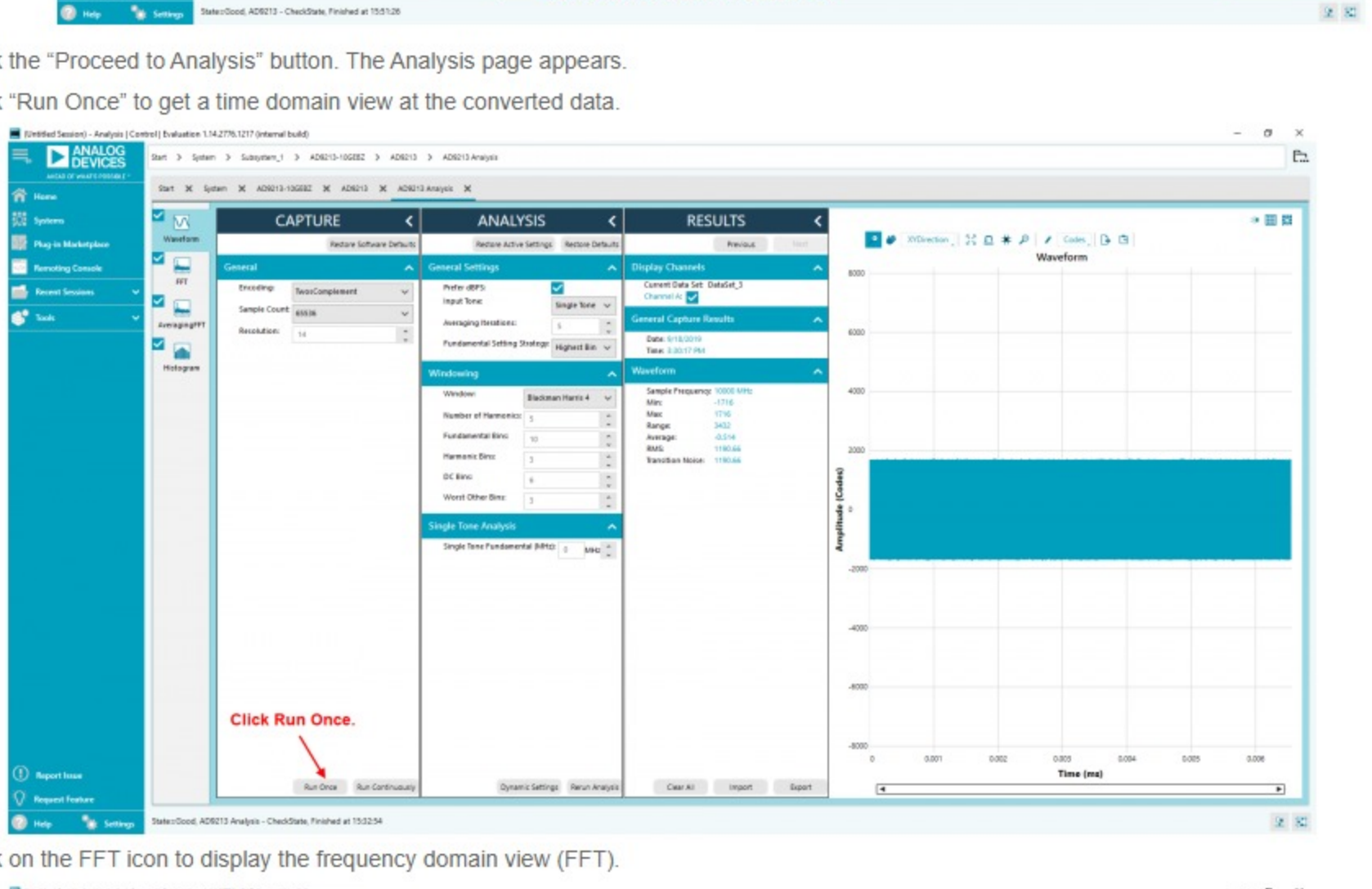
- AD9213 DDC and NCO controls are added to the configuration wizard. The following image shows a summary of the settings.



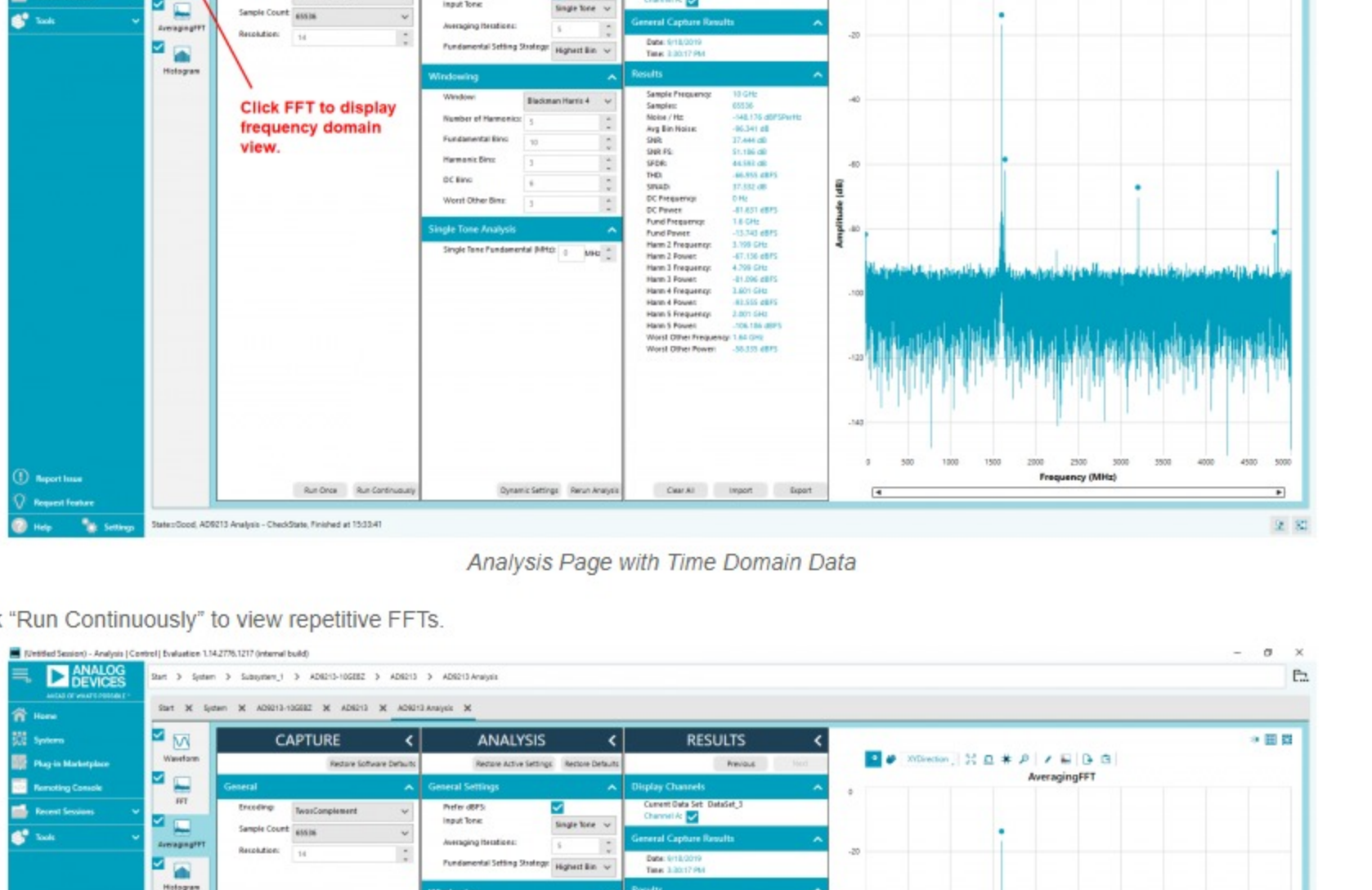
- Click the 'Proceed to Analysis' button. The Analysis page appears.



- Click the 'Run Once' button to get a time domain view at the converted data.



- Click the 'Run Continuously' button to view repetitive FFTs.



Notes

- If the ACE startup procedure does not proceed as described or expected (assuming you properly setup the hardware):
 - Close the ACE software.
 - Power down the ADS8-V1EBZ using switch S4 (you might need to repeat this step several times).
- If after repeated attempts the ACE startup procedure is not successful:
 - Check that the jumpers are placed on the AD9213/9217 evaluation board as shown in step 4.
 - Check that all signal generators are on and at the correct frequencies and power levels.
 - Check that 3.3V appears at TPS on the Regulator Board.