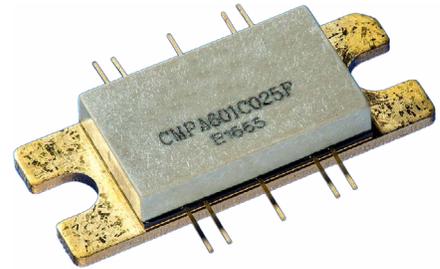


# CMPA601C025F

25 W, 6.0 - 12.0 GHz, GaN MMIC, Power Amplifier

## Description

The CMPA601C025F is a gallium nitride (GaN) High Electron Mobility Transistor (HEMT) based monolithic microwave integrated circuit (MMIC) on a Silicon Carbide (SiC) substrate, using a 0.25µm gate length fabrication process. The semiconductor offers 25 Watts of power from 6 to 12 GHz of instantaneous bandwidth. The GaN HEMT MMIC is housed in a thermally-enhanced, 10-lead 25 mm x 9.9 mm metal/ceramic flanged package. It offers high gain and superior efficiency in a small footprint package at 50 ohms.



PN: CMPA601C025F  
Package Type: 440213

## Typical Performance Over 6.0 - 12 GHz ( $T_c = 25^\circ\text{C}$ )

Parameter	6.0 GHz	7.5 GHz	9.0 GHz	10.5 GHz	12.0 GHz	Units
Small Signal Gain	35	34	34	37	31	dB
$P_{OUT}$ @ $P_{IN} = 22$ dBm	34	51	49	45.9	36.5	W
Power Gain @ $P_{IN} = 22$ dBm	23	25	25	25	23.5	dB
PAE @ $P_{IN} = 22$ dBm	21	36	35	33	27	%

Note: All data CW

### Features

- 34 dB Small Signal Gain
- 40 W Typical  $P_{SAT}$
- Operation up to 28 V
- High Breakdown Voltage
- High Temperature Operation
- Size 0.172 x 0.239 x 0.004 inches

### Applications

- Jamming Amplifiers
- Test Equipment Amplifiers
- Broadband Amplifiers



### Absolute Maximum Ratings (not simultaneous) at 25°C

Parameter	Symbol	Rating	Units	Conditions
Drain-Source Voltage	$V_{DSS}$	84	$V_{DC}$	25°C
Gate-Source Voltage	$V_{GS}$	-10, +2		
Storage Temperature	$T_{STG}$	-40, +150	°C	
Operating Junction Temperature	$T_J$	225		
Maximum Forward Gate Current	$I_{GMAX}$	23	mA	25°C
Soldering Temperature <sup>1</sup>	$T_{STG}$	245	°C	
Screw Torque	$\tau$	40	in-oz	
Thermal Resistance, Junction to Case <sup>2</sup>	$R_{\theta JC}$	0.85	°C/W	85°C @ $P_{DISS} = 116W$
Case Operating Temperature <sup>2</sup>	$T_C$	-40, +150	°C	

Notes:

<sup>1</sup> Refer to the Application Note on soldering<sup>2</sup> See also, the Power Dissipation De-rating Curve on page 5

### Electrical Characteristics (Frequency = 6.0 GHz to 12.0 GHz unless otherwise stated; $T_C = 25^\circ C$ )

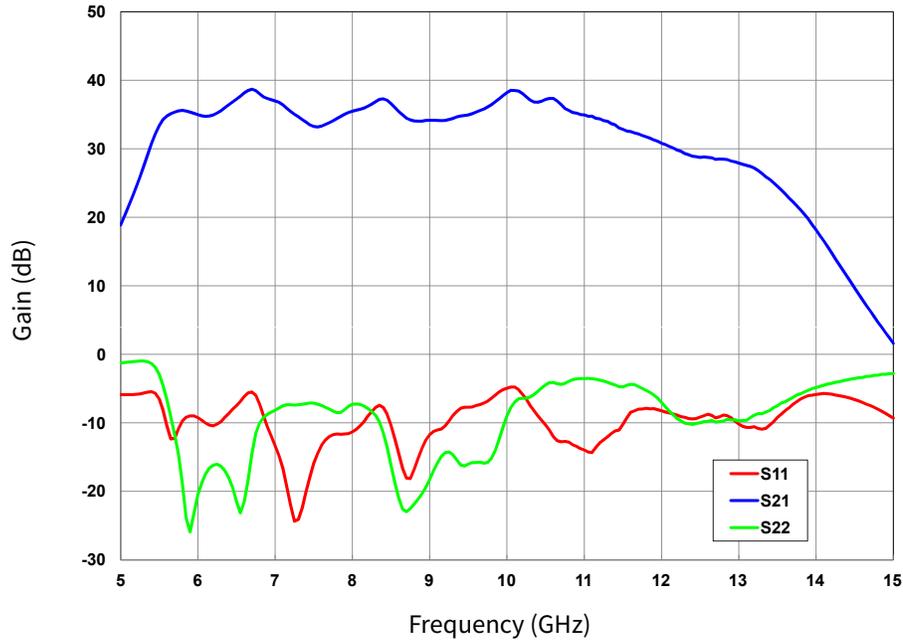
Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>DC Characteristics<sup>1,2</sup></b>						
Gate Threshold	$V_{TH}$	-3.8	-2.8	-2.3	V	$V_{DS} = 10 V, I_D = 23 mA$
Saturated Drain Current	$I_{DS}$	10.6	13.0		A	$V_{DS} = 6 V, I_{GS} = 2 V$
Drain-Source Breakdown Voltage	$V_{BD}$	84	100	—	V	$V_{GS} = -8 V, I_{DS} = 23 mA$
<b>RF Characteristics<sup>3</sup></b>						
Small Signal Gain at 6.0 - 10.5 GHz	S21	28	31	—	dB	$V_{DD} = 28 V, I_{DQ} = 2 A, P_{IN} = -30 dBm$
Small Signal Gain at 10.5 - 12 GHz		25	28	—		
Output Power at 6 GHz <sup>3,4</sup>	$P_{OUT1}$	45.5	47.2	—	dBm	$V_{DD} = 28 V, I_{DQ} = 2 A, P_{IN} = 22 dBm$
Output Power at 9.5 GHz <sup>3,4</sup>	$P_{OUT2}$	45.5	47.1	—		
Output Power at 12 GHz <sup>3,4</sup>	$P_{OUT3}$	43.0	44.8	—		
Power Added Efficiency at 6 GHz <sup>3,4</sup>	$PAE_1$	23	33.2	—	%	
Power Added Efficiency at 9.5 GHz <sup>3,4</sup>	$PAE_2$	26	32.3	—		
Power Added Efficiency at 12 GHz <sup>3,4</sup>	$PAE_3$	15.5	26.5	—		
Input Return Loss	S11	—	-5	—	dB	$V_{DD} = 28 V, I_{DQ} = 2 A, P_{IN} = -30 dBm$
Output Return Loss	S22	—		—		
Output Mismatch Stress	VSWR	—	—	5:1	Ψ	No damage at all phase angles, $V_{DD} = 28 V, I_{DQ} = 2 A, P_{IN} = 22 dBm$

Notes:

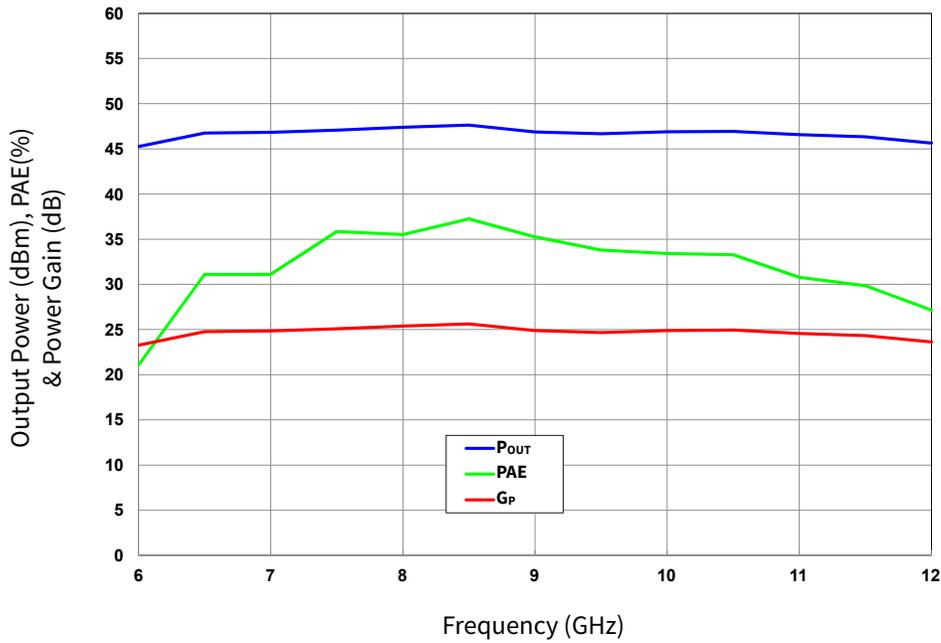
<sup>1</sup> Measured on-wafer prior to packaging<sup>2</sup> Scaled from PCM data<sup>3</sup> Measured in CMPA601C025F-AMP with 12.4 GHz low pass filter<sup>4</sup> Fixture loss de-embedded using the following offsets. The offset is subtracted from the input offset value and added to the output offset value.

- a) 6.0 GHz - 0.13 dB
- b) 9.50 GHz - 0.26 dB
- c) 12.0 GHz - 0.35 dB

**CMPA601C025F Typical Performance**

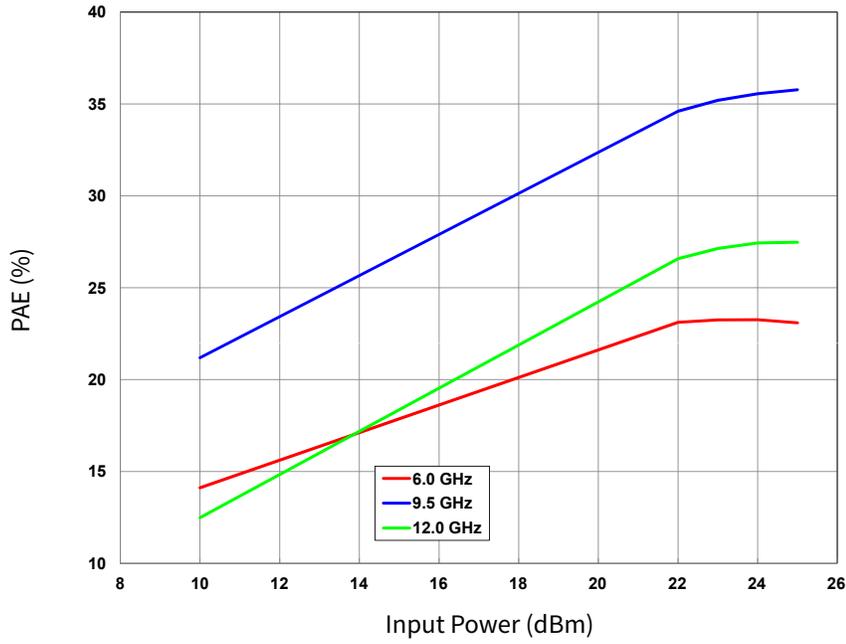


**Figure 1.** Small Signal S-Parameters vs. Frequency  
 $V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 2.0\text{ A}$ ,  $P_{IN} = -30\text{ dBm}$

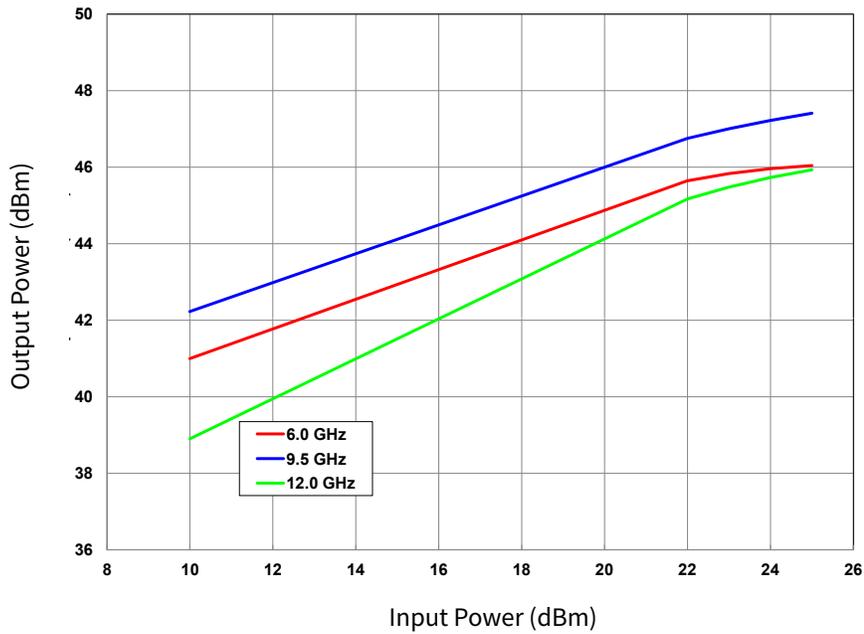


**Figure 2.** Output Power, Gain and Power Added Efficiency vs. Input Power  
 $V_{DD} = 28\text{ V}$ ,  $I_{DQ} = 2.0\text{ A}$ ,  $P_{IN} = 22\text{ dBm}$

**CMPA601C025F Typical Performance**

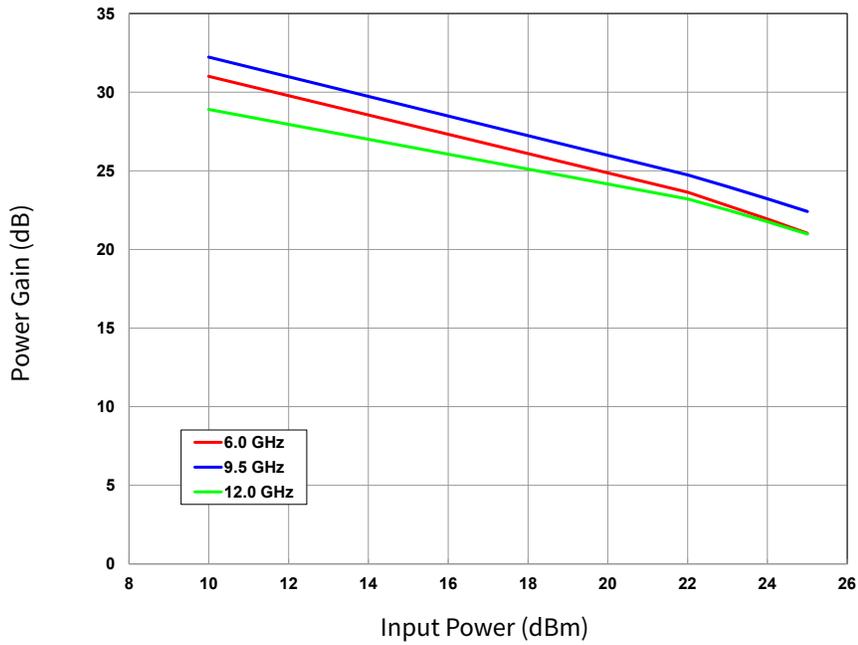


**Figure 3.** Power Added Efficiency vs. Input Power  
 $V_{DD} = 28\text{ V}, I_{DQ} = 2.0\text{ A}$

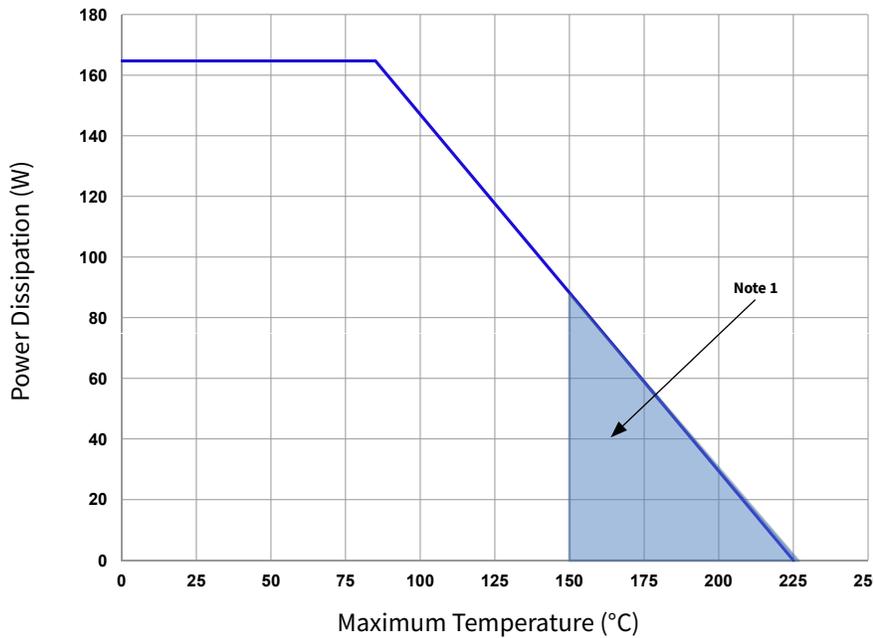


**Figure 4.** Output Power vs. Input Power  
 $V_{DD} = 28\text{ V}, I_{DQ} = 2.0\text{ A}$

**CMPA601C025F Typical Performance**



**Figure 5. Gain vs Input Power**  
 $V_{DD} = 28\text{ V}, I_{DQ} = 2.0\text{ A}$



**Figure 6. Power Dissipation Derating Curve**

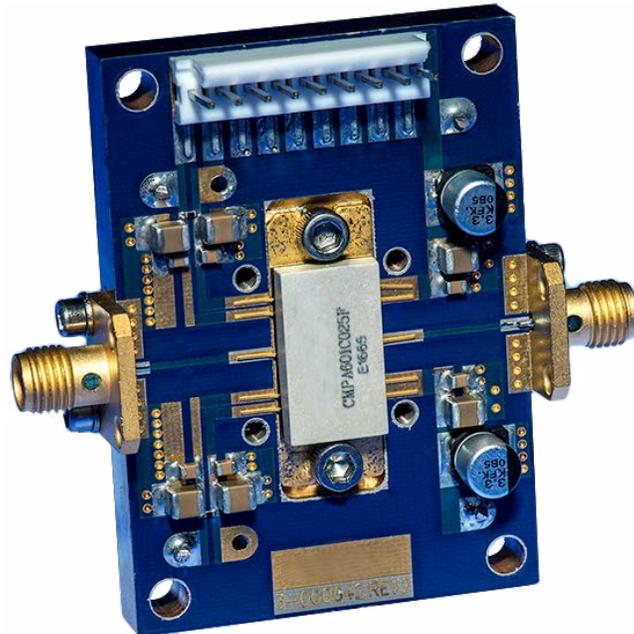
Notes:

<sup>1</sup> Area exceeds Maximum Case Operating Temperature (See Page 2)

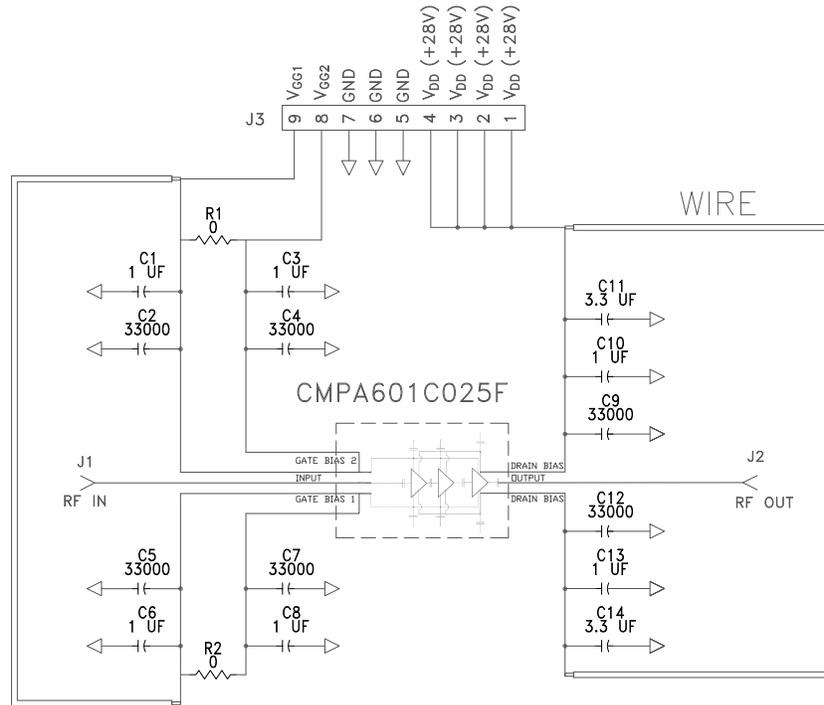
**CMPA601C025F-AMP Demonstration Amplifier Circuit Bill of Materials**

Designator	Description	Qty
C2, C4, C5, C7, C9, C12	CAP, 33000pF, 0805, 100V, X7R	6
C1, C3, C6, C8, C10, C13	CAP, 1.0μF, 100V, 10%, X7R, 1210	6
C11, C14	CAP ELECT 3.3μF 80V FK SMD	2
R1, R2	RES 0.0 OHM 1/16W 0402 SMD	2
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
W1	WIRE, BLACK, 22 AWG ~ 1.50"	1
W2	WIRE, BLACK, 22 AWG ~ 1.75"	1
Q1	CMPA601C025F	1

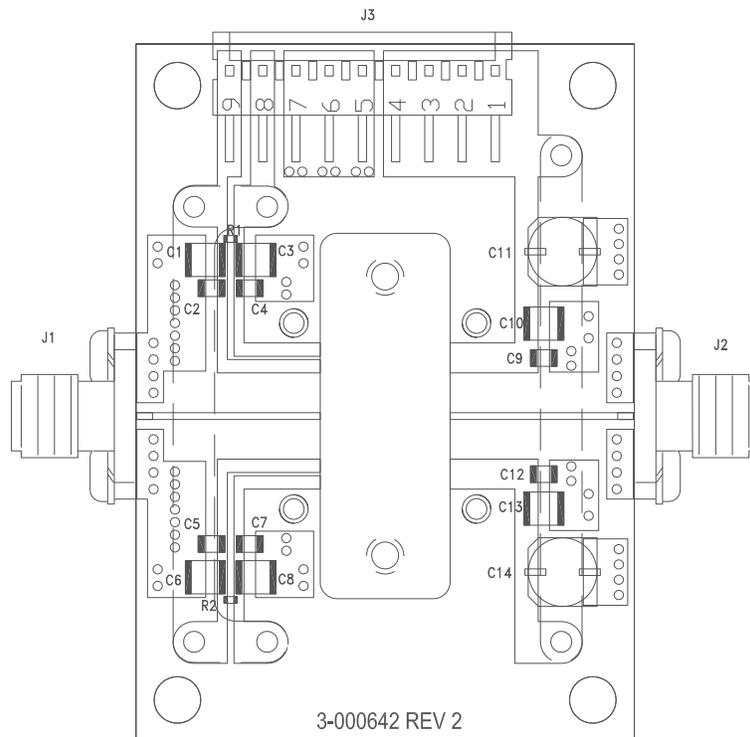
**CMPA601C025F-AMP Demonstration Amplifier Circuit**



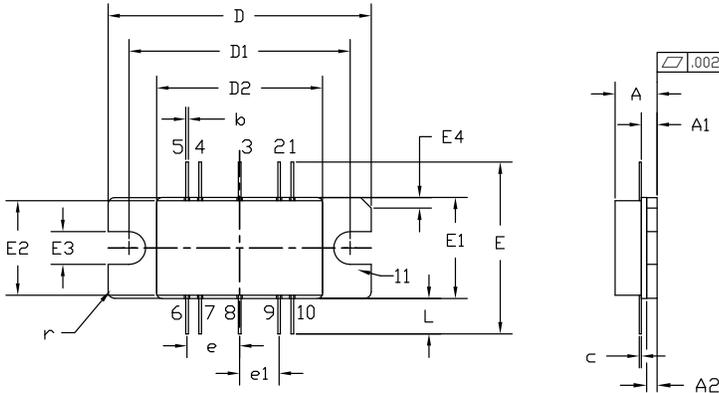
### CMP601C025F-AMP Demonstration Amplifier Circuit Schematic



### CMPA601C025F-AMP Demonstration Amplifier Circuit Outline



**Product Dimensions CMPA601C025F**



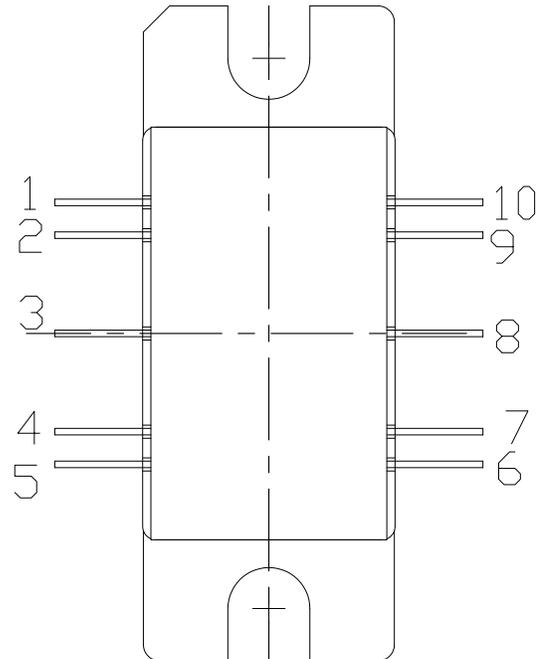
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1994.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.

DIM	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.155	0.175	3.94	4.45	
A1	0.055	0.065	1.40	1.65	
A2	0.035	0.045	0.89	1.14	
b	0.01	TYP	0.254	TYP	10x
c	0.007	0.009	0.18	0.23	
D	0.995	1.005	25.27	25.53	
D1	0.835	0.845	21.21	21.46	
D2	0.623	0.637	15.82	16.18	
E	0.653	TYP	16.59	TYP	
E1	0.380	0.390	9.65	9.91	
E2	0.355	0.365	9.02	9.27	
E3	0.120	0.130	3.05	3.30	
E4	0.035	0.045	0.89	1.14	45° CHAMFER
e	0.200	TYP	5.08	TYP	4x
e1	0.150	TYP	3.81	TYP	4x
L	0.115	0.155	2.92	3.94	10x
r	0.025	TYP	.635	TYP	3x

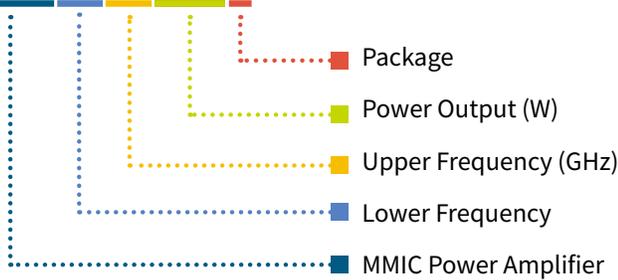
- PIN 1: GATE BIAS 6: DRAIN BIAS  
 2: GATE BIAS 7: DRAIN BIAS  
 3: RF IN 8: RF OUT  
 4: GATE BIAS 9: DRAIN BIAS  
 5: GATE BIAS 10: DRAIN BIAS  
 11: SOURCE

Pin Number	Qty
1	Gate Bias for Stage 1, 2 & 3
2	Gate Bias for Stage 1, 2 & 3
3	RF <sub>IN</sub>
4	Gate Bias for Stage 1, 2 & 3
5	Gate Bias for Stage 1, 2 & 3
6	Drain Bias
7	Drain Bias
8	RF <sub>OUT</sub>
9	Drain Bias
10	Drain Bias



**Part Number System**

**CMPA601C025F**



**Table 1.**

Parameter	Value	Units
Lower Frequency	6.0	GHz
Upper Frequency <sup>1</sup>	12.0	GHz
Power Output	25	W
Package	Flanged	—

Note:  
<sup>1</sup> Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

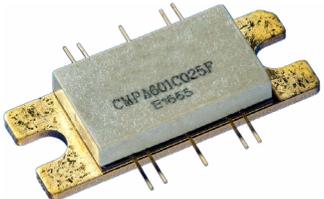
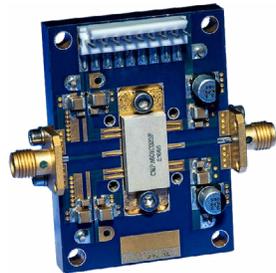
**Table 2.**

Character Code	Code Value
A	0
B	1
C	2
D	3
E	4
F	5
G	6
H	7
J	8
K	9
Examples:	1A = 10.0 GHz 2H = 27.0 GHz

**Electrostatic Discharge (ESD) Classifications**

Parameter	Symbol	Class	Classification Level	Test Methodology
Human Body Model	HBM	1A	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	C3	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

**Product Ordering Information**

Order Number	Description	Unit of Measure	Image
CMPA601C025F	GaN HEMT	Each	
CMPA601C025F-AMP	Test board with GaN HEMT installed	Each	

## Notes & Disclaimer

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