QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1525
12/14 BIT, 25 TO 125 MSPS QUAD ADC

LTC2175-14, LTC2175-12, LTC2174-14, LTC2174-12, LTC2173-14, LTC2173-12, LTC2172-14, LTC2172-12, LTC2171-14, LTC2171-12, LTC2170-14, LTC2170-12

DESCRIPTION

Demonstration circuit 1525 supports a family of 14/12 BIT 125 MSPS ADCs. Each assembly features one of the following devices: LTC2175-14, LTC2175-12, LTC2174-14, LTC2174-12, LTC2173-14, LTC2173-12, LTC2172-14, LTC2172-12, LTC2171-14, LTC2171-12, LTC2170-14, LTC2170-12 high speed, quad ADCs.

The versions of the 1525A demo board are listed in Table 1. Depending on the required resolution and sample rate, the DC1525 is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5 MHz to 140MHz. Refer to the datasheet for proper input networks for different input frequencies.

Design files for this circuit board are available. Call the LTC factory.

Table 1. DC1525 Variants

DC1525 VARIANTS	ADC PART NUMBER	RESOLUTION*	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1525A-A	LTC2175-14	14-BIT	125 Msps	5MHz-140MHz
1525A-B	LTC2174-14	14-BIT	105 Msps	5MHz-140MHz
1525A-C	LTC2173-14	14-BIT	80 Msps	5MHz-140MHz
1525A-D	LTC2172-14	14-BIT	65 Msps	5MHz-140MHz
1525A-E	LTC2171-14	14-BIT	40 Msps	5MHz-140MHz
1525A-F	LTC2170-14	14-BIT	25 Msps	5MHz-140MHz
1525A-G	LTC2175-12	12-BIT	125 Msps	5MHz-140MHz
1525A-H	LTC2174-12	12-BIT	105 Msps	5MHz-140MHz
1525A-I	LTC2173-12	12-BIT	80 Msps	5MHz-140MHz
1525A-J	LTC2172-12	12-BIT	65 Msps	5MHz-140MHz
1525A-K	LTC2171-12	12-BIT	40 Msps	5MHz-140MHz
1525A-L	LTC2170-12	12-BIT	25 Msps	5MHz-140MHz

Table 2. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage – DC1525A	Depending on sampling rate and the A/D converter provided, this supply must provide up to 500mA.	Optimized for 3V [3V ⇔6.0V min/max]
Analog input range	Depending on SENSE Pin Voltage	1 V_{PP} to 2V_{PP}
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (differential)	Nominal Logic levels (100Ω load, 3.5mA Mode)	350mV/1.25V common mode
	Minimum Logic levels (100Ω load, 3.5mA Mode)	247mV/1.25V common mode
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Encode Clock Level	Single ended Encode Mode (ENC- tied to GND)	0-3.6V
Encode Clock Level	Differential Encode Mode (ENC- not tied to GND)	0.2V-3.6V
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 1525 is easy to set up to evaluate the performance of the LTC2175 A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

SETUP

If a DC1371 “PStache” Data Acquisition and Collection System was supplied with the DC1525 demonstration circuit, follow the DC1371 Quick Start Guide to install the required software and for connecting the DC1371 to the DC1525 and to a PC running Windows 2000 or XP.

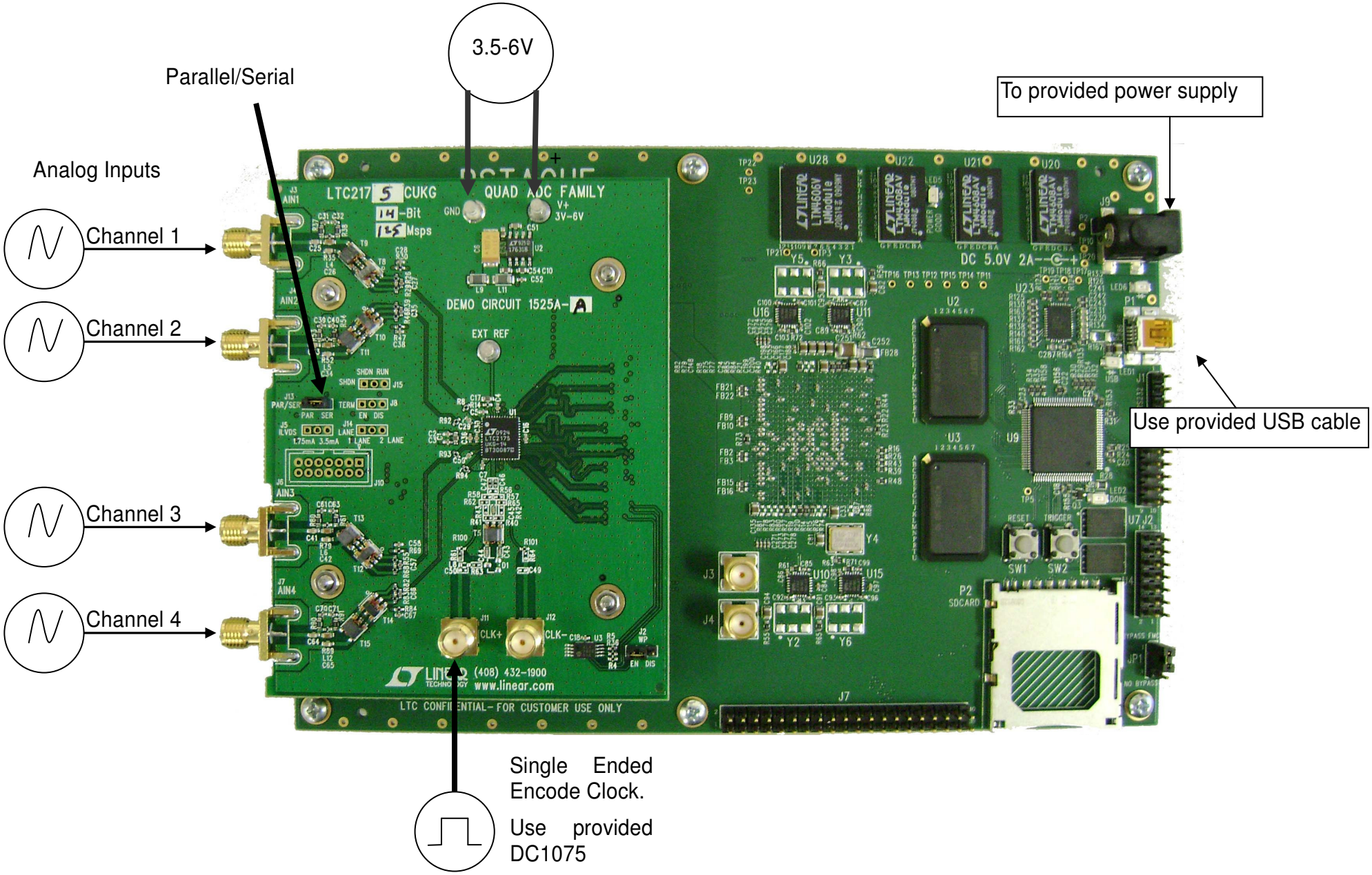


Figure 1. DC1525 Setup (zoom for detail)

DC1525 DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC1525 demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1)

J13: PAR/SER : Selects Parallel or Serial programming mode. (Default - Serial)

Optional Jumpers:
J8: Term: Enables/ Disable optional output termination. (Default - Removed)

J5: ILVDS: Selects either 1.75mA or 3.5mA of output current for the LVDS drivers. (Default – Removed)

J14: LANE: Selects either 1 lane or 2 lane output modes (Default – Removed) NOTE: The DC1371 does not support 1 lane operation.

J15: SHDN: Enables and disables the LTC2175. (Default - Removed)

J2: WP: Enable/Disables write protect for the EEPROM. (Default – Removed)

Note: optional jumper should be left open to ensure proper serial configuration.

APPLYING POWER AND SIGNALS TO THE DC1525 DEMONSTRATION CIRCUIT

The DC1371 is used to acquire data from the DC1525, the DC1371 must FIRST be connected to a powered USB port and have =5V applied power BEFORE applying +3.6V to +6.0V across the pins marked “V+” and “GND” on the DC1525. DC1525 requires 3.6V for proper operation.

Regulators on the board produce the voltages required for the ADC. The DC1525 demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC1525 should not be removed, or connected to the DC1371 while power is applied.

ANALOG INPUT NETWORK

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 140 MHz, refer to the LTC2175 datasheet for a proper input network. Other input networks may be more appropriate for input frequencies less that 5MHz.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final ampli-

fier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Apply the analog input signal of interest to the SMA connectors on the DC1525 demonstration circuit board marked “J3 AIN1”, “J4 AIN2”, “J6 AIN3”, “J7 AIN4”. These inputs correspond with channels 1-4 of the ADC respectively. These inputs are capacitive coupled to Balun transformers ETC1-1-13.

ENCODE CLOCK

NOTE: Apply an encode clock to the SMA connector on the DC1525 demonstration circuit board marked “J11 CLK+”. As a default the DC1525 is populated to have a single ended input.

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075A that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2175.

Using band pass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1525 a band pass filter used for the clock should be used prior to the DC1075A. Datasheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used for both the Clock input and the Analog input.

DIGITAL OUTPUTS

Data outputs. data clock, and frame clock signals are available on J1 of the DC1525. This connector follows the VITA-57/FMC standard, but all signals should be verified when using an FMC carrier card other than the DC1371.

SOFTWARE

The DC1371A is controlled by the PScope System Software provided or downloaded from the Linear Technology website at http://www.linear.com/software/.

To start the data collection software if “PScope.exe”, is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1525 demonstration circuit is properly connected to the DC1371, PSCOPE should automatically detect the DC1525, and configure itself accordingly.

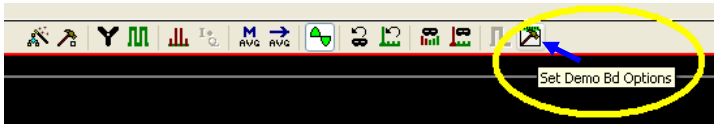
If everything is hooked up properly, powered and a suitable convert clock is present, clicking the “Collect” button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371A Quick Start Guide and in the online help available within the PScope program itself.

SERIAL PROGRAMMING

PScope has the ability to program the DC1525 board serially through the DC1371. There are several options available in the LTC2175 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the "Set Demo Bd Options" icon on the PScope toolbar (Figure 3).

Figure 3: PScope Toolbar



This will bring up the menu shown in figure 4.

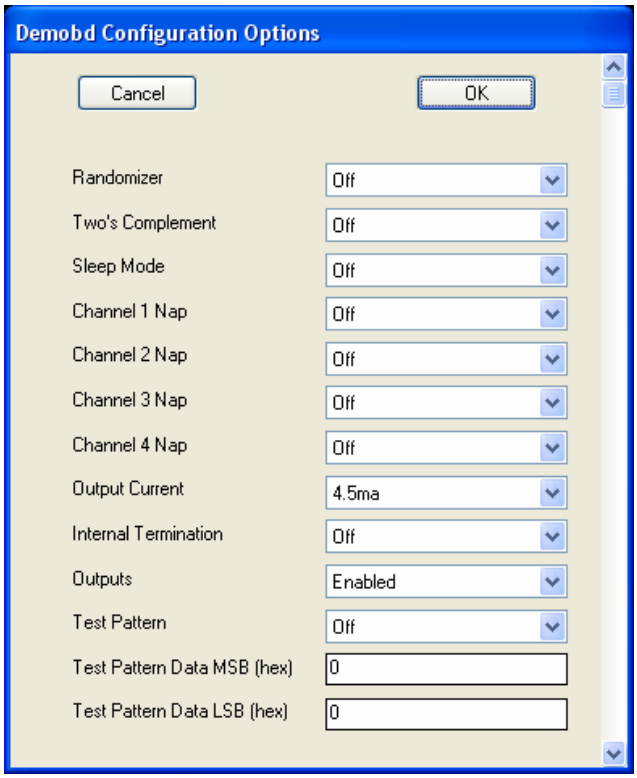


Figure 4: Demobd Configuration Options.

This menu allows any of the options available for the LTC2175 family to be programmed serially. The LTC2175 family has the following options:

Randomizer – Enables Data Output Randomizer

- Off (Default) – Disables data output randomizer

- On – Enables data output randomizer

Two's complement – Enables two's complement mode

- Off (Default) – Selects offset binary mode

- On – Selects two's complement mode

Sleep Mode– Selects between normal operation, sleep mode:

- Off (Default) – Entire ADC is powered, and active

- On – The entire ADC is powered down.

Channel 1 Nap- Selects between normal operation and putting channel 1 in nap mode.

-Off (Default) – Channel one is active

- On – Channel one is in nap mode

Channel 2 Nap- Selects between normal operation and putting channel 2 in nap mode.

-Off (Default) – Channel two is active

- On – Channel two is in nap mode

Channel 3 Nap- Selects between normal operation and putting channel 3 in nap mode.

-Off (Default) – Channel three is active

- On – Channel three is in nap mode

Channel 4 Nap- Selects between normal operation and putting channel 4 in nap mode.

-Off (Default) – Channel four is active

- On – Channel four is in nap mode

Output Current – Selects the LVDS output drive current

- 1.75mA (Default) - LVDS output driver current

- 2.1mA - LVDS output driver current

- 2.5mA - LVDS output driver current

- 3.0mA - LVDS output driver current

- 3.5mA - LVDS output driver current

- 4.0mA - LVDS output driver current

- 4.5mA - LVDS output driver current

Internal Termination – Enables LVDS internal termination

- Off (Default) – Disables internal termination

- On – Enables internal termination

Outputs – Enables Digital Outputs

- Enabled (Default) – Enables digital outputs

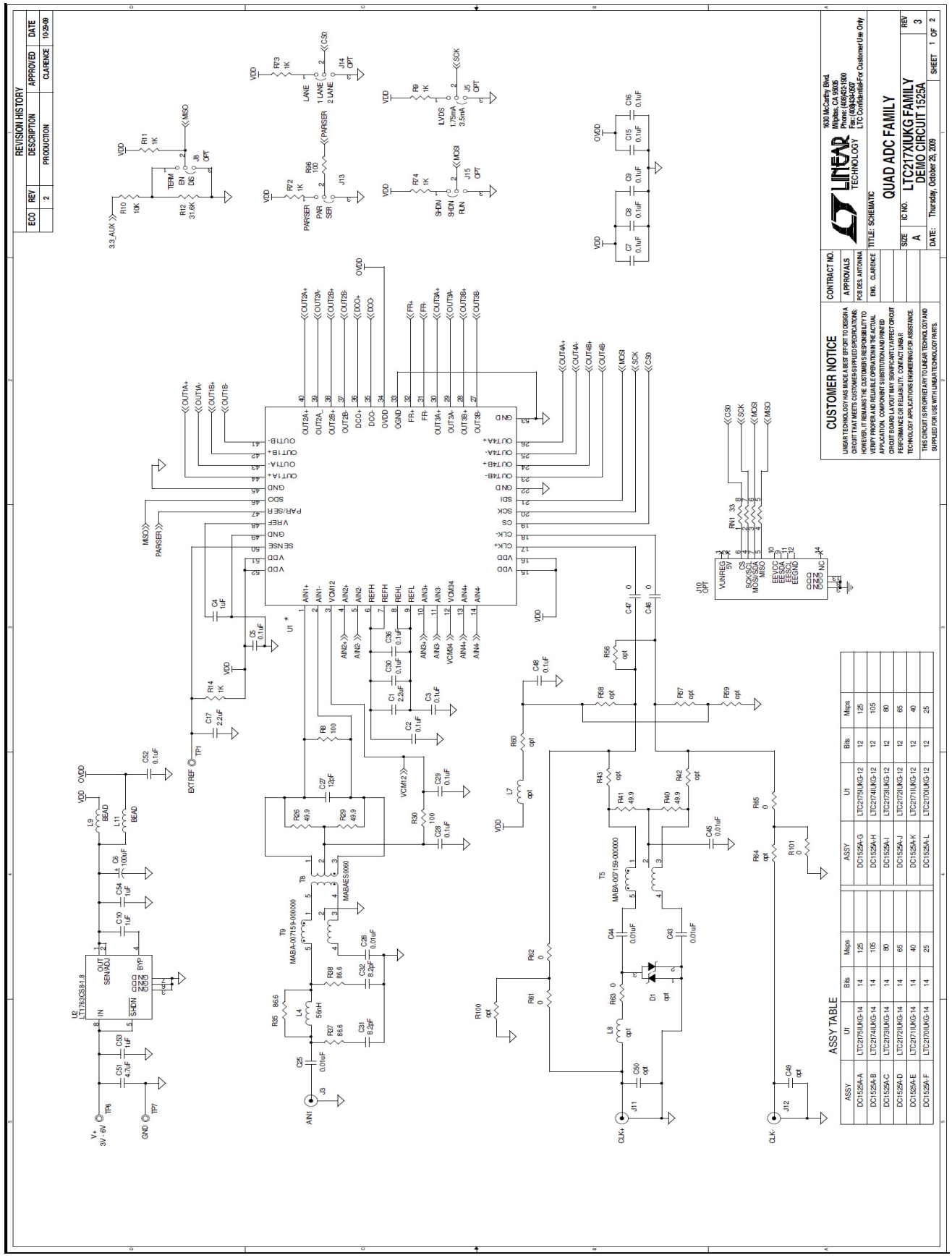
- Disabled – Disables digital outputs

Test Pattern – Selects Digital output test patterns. The desired test pattern can be entered into the text boxes provided.

-Off(default) – ADC input data is displayed

-On – Test pattern is displayed.

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1525 demo board.


REVISION HISTORY
ECO REV DESCRIPTION APPROVED DATE
2 PRODUCTION CLARENCE 10-29-09
CUSTOMER NOTICE
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.
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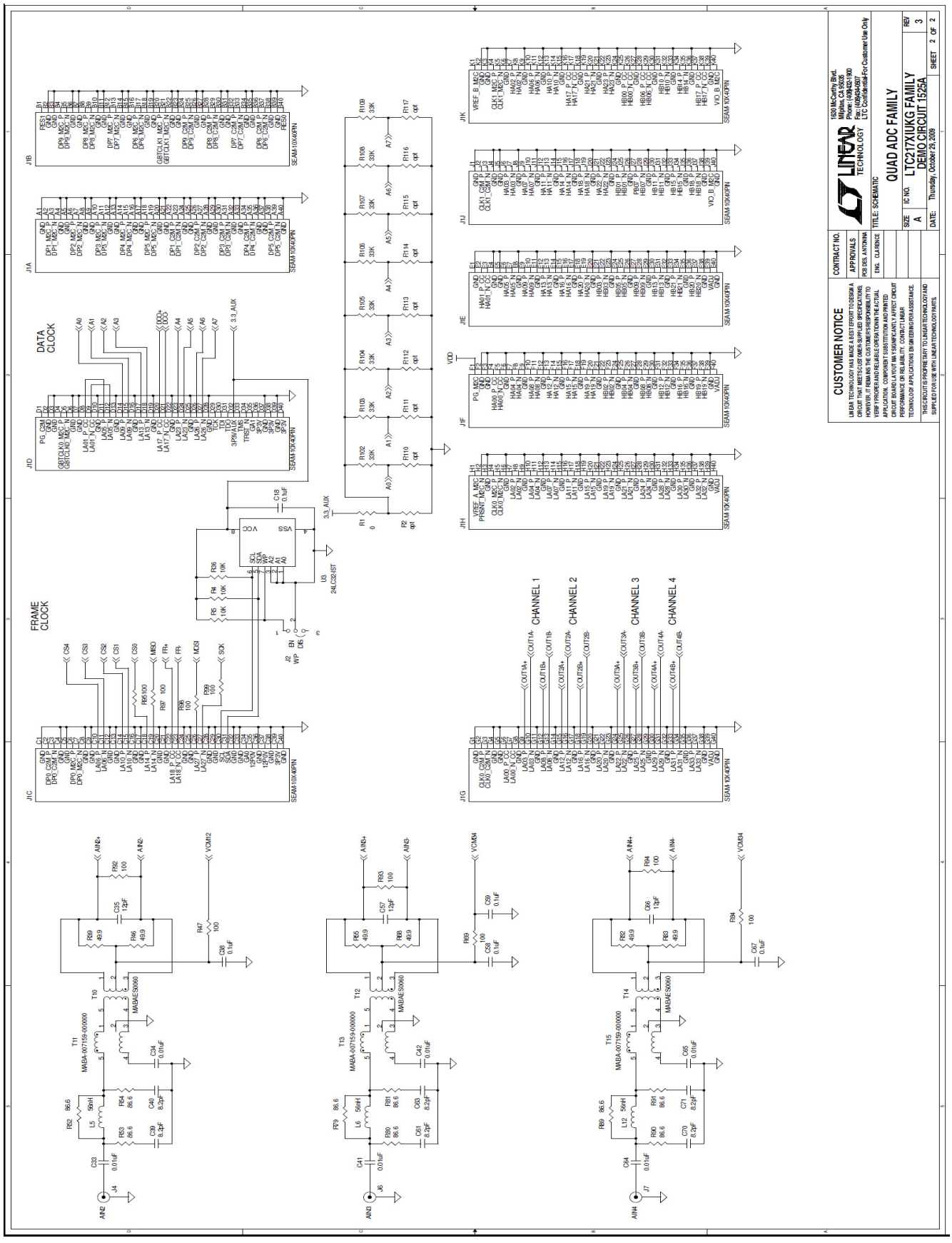
LTC Confidential-For Customer Use Only
TITLE: SCHEMATIC
QUAD ADC FAMILY
SIZE A
IC NO. LTC2171XIUKG FAMILY
DEMO CIRCUIT 1525A
REV 3
DATE: Thursday, October 29, 2009
SHEET 1 OF 2
ASSY TABLE
ASSY U1 Bits Msps
DC1525A-A LTC2175IUKG-14 14 125
DC1525A-B LTC2174IUKG-14 14 105
DC1525A-C LTC2173IUKG-14 14 80
DC1525A-D LTC2172IUKG-14 14 65
DC1525A-E LTC2171IUKG-14 14 40
DC1525A-F LTC2170IUKG-14 14 25
ASSY U1 Bits Msps
DC1525A-G LTC2175IUKG-12 12 125
DC1525A-H LTC2174IUKG-12 12 105
DC1525A-I LTC2173IUKG-12 12 80
DC1525A-J LTC2172IUKG-12 12 65
DC1525A-K LTC2171IUKG-12 12 40
DC1525A-L LTC2170IUKG-12 12 25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FRAME CLOCK
CHANNEL 1
CHANNEL 2
CHANNEL 3
CHANNEL 4
SEAM-10X40PIN
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24LC02BST
AIN1
AIN2
AIN3
AIN4
VCM12
VCM34