LTC4278

DESCRIPTION

Demonstration circuit 1561A is a high-power supply featuring the LTC®4278. This board is a Type 2 (IEEE 802.3at) compliant, high power Power-over-Ethernet (PoE), Powered Device (PD). The DC1561 also features a wide auxiliary input voltage range of 9V to 57V. The demonstration board can connect to a Type 2 Power Sourcing Equipment (PSE) device, such as the DC1567.

The LTC4278 provides IEEE802.3at standard (PoE+) PD interfacing and power supply control. When the PD fully powers the PD interface passes power from the PSE to the switcher through an internal, low resistance, high power MOSFET. The highly integrated LTC4278 con-

trols a high-power, small-sized power supply that utilizes a highly-efficient isolated flyback topology with synchronous rectification. The DC1561A outputs 5V at 4.5A.

DC1561A also demonstrates the use of an auxiliary wall adapter for nominal 12Vdc, 24Vac/dc, or 48Vdc systems. When present, the auxiliary supply is the dominant supply over PoE to provide power.

Design files for this circuit board are available. Call the LTC factory.

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Table 1. Performance Summary $(T_A = 25 ^{\circ}C)$

PARAMETER	CONDITION	VALUE
PoE Input Voltage (V _{PORT})	At RJ-45 Jack (J1)	37V – 57V
Auxiliary Input Voltage (VAUX)	From AUX+ to AUX- terminals	9V – 57V
Output Voltage (V _{OUT})	Typical	5V
Output Current (I _{OUT})	Over 9V to 57V input voltage	4.5A (max)
Output Voltage Ripple (typ)	Over 9V to 57V input voltage, I _{OUT} = 4.5A	30mV _{P-P} (typ)
Output Regulation	PoE Input Voltage, I _{OUT} = 0A to 4.5A	±0.4% (typ)
	Auxiliary Input Voltage, I _{OUT} = 0A to 4.5A	±1.1% (typ)
Output Voltage Response to Load Step (typ)	Load Step = 2.25A to 4.5A, 48V Input Voltage	±500mV (±10%) (typ)
	Settling Time (within 1% of V _{OUT})	< 150us (typ)
Switching Frequency		250kHz (typ)
Efficiency	V _{AUX} = 24V, I _{OUT} = 4.5A (includes diode D12)	89% (typ)

OPERATING PRINCIPLES

A compatible high power PSE board, such as the DC1567, connects to the DC1561A at the RJ45 connector J1 (see the schematic in Figure 12). As required by IEEE802.3at, the DC1561A

uses a diode bridge across the data pairs and signal pairs. Schottky diodes (D2-9) are used at the input to improve efficiency over standard diode bridges. The LTC4278 provides the PoE



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required 25k signature resistance and classification up to class 4 (25.5W). When the PD is powered and voltage reaches above the PoE "On Voltage", the LTC4278 switches the port voltage over to the power supply controller through its internal MOSFET. This voltage allows the zener and NPN-based linear regulator (R9/D17/Q3) to power up the bias pin, V_{CC}, of the power supply controller. The IC begins a controlled soft-start of the output. As the output voltage rises, bias power takes over by the bias supply made up of T1's bias winding and D11 since it reverse biases the linear regulator's (Q3) base to emitter junction.

When the soft-start period is over, the output voltage regulates by observing the pulses across the bias winding during the flyback time.

The Primary Gate drive (PG) and Synchronous Gate (SG) drive Pulse Width Modulates (PWM) in order to keep the output voltage constant. The synchronous gate drive signal transmits to the secondary via the small signal transformer, T2. The output of T2 drives a discrete gate drive buffer, R22 and Q6/7 to achieve fast gate transition times, hence higher efficiency.

The two-stage input filter, C5, L2, and C6 and output filter, C1/3, L1, and C9 are the reasons that this PoE flyback supply has exceptionally low differential mode conducted emissions. A common mode filter consisting of a common mode choke (L3) and common mode capacitor (C34) yields low common mode emissions out of the power supply.

QUICK START PROCEDURE

Demonstration circuit 1561A is easy to set up to evaluate the performance of the LTC4278 in a PoE+ PD application. Refer to Figure 1 for proper equipment setup and follow the procedure below:

- 1. Place test equipment (voltmeter, ammeter, and electronic load) across output.
- 2. Input supplies:
 - a. Connect a PoE+ capable PSE, like the DC1567, with an Ethernet cable to the RJ45 connector, J1. See Figure 1.
 - b. Or, connect a 37V to 57V capable power supply ("Power Supply" in Figure 1) across VPORT P and VPORT N.
 - c. Or, if evaluating the auxiliary power supply capability, connect a 9V to 57V @ 4A capable

power supply across AUX+ to AUX- ("Auxiliary Supply" in Figure 1).

- 3. Check for the proper output voltage of 5V.
- 4. Once the proper output voltage is confirmed, adjust the output's load current within the operating range and observe the output voltage regulation, output ripple voltage, efficiency, and other parameters.

NOTE: When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output (or input) voltage ripple by touching the probe tip and probe ground directly across the +VOUT and -VOUT (or VPORT_P and VPORT_N) terminals. See Figure 2 for proper scope probe technique.



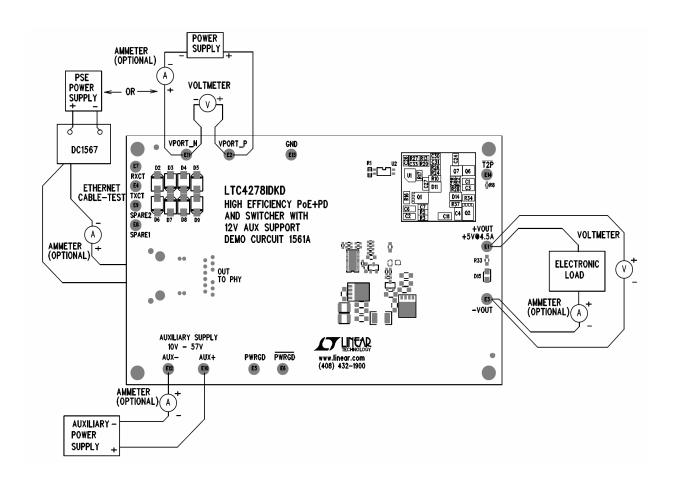


Figure 1. Proper Measurement Equipment Setup

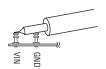


Figure 2. Measuring Input or Output Ripple



MEASURED DATA

Figures 3 through 11 are measured data for a typical DC1561A. Figure 12 is the schematic and Figure 13 is the bill of materials.

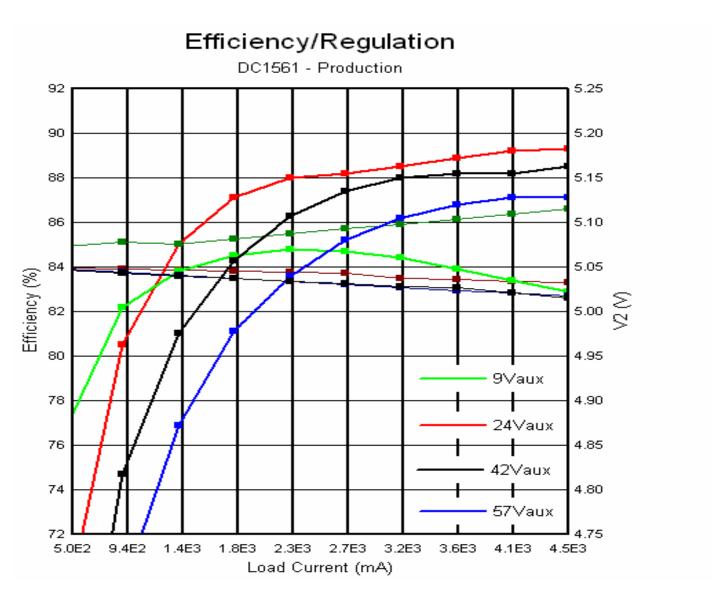


Figure 3. Efficiency and Regulation (including OR'ing diode, D12)



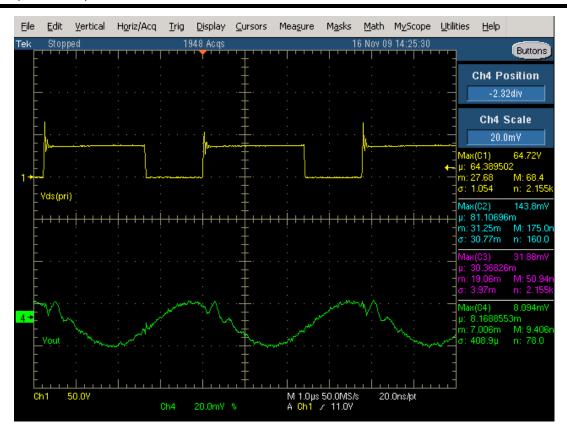


Figure 4. Output Ripple (24Vaux, 4.5A)

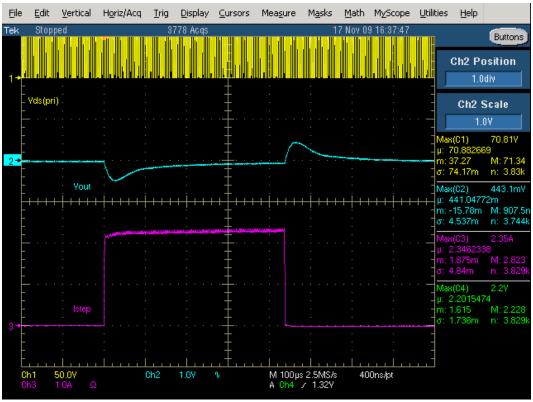


Figure 5. Load Transient Response (57Vport, 2.25A to 4.5A to 2.25A)



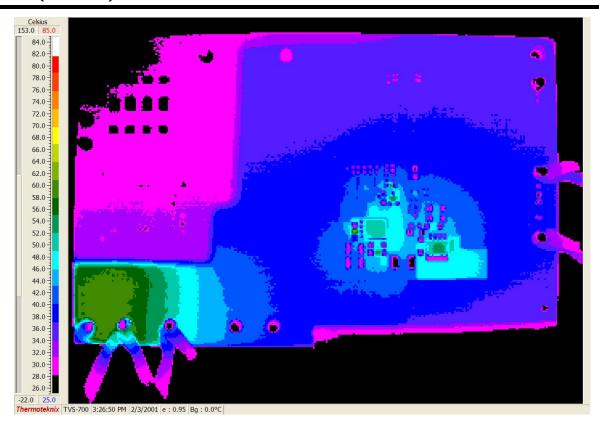


Figure 6. Temp Data (9Vaux, 4.5A, Top)

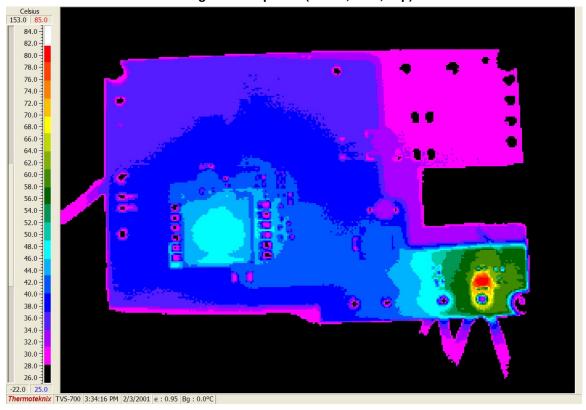


Figure 7. Temp Data (9Vaux, 4.5A, Bottom)



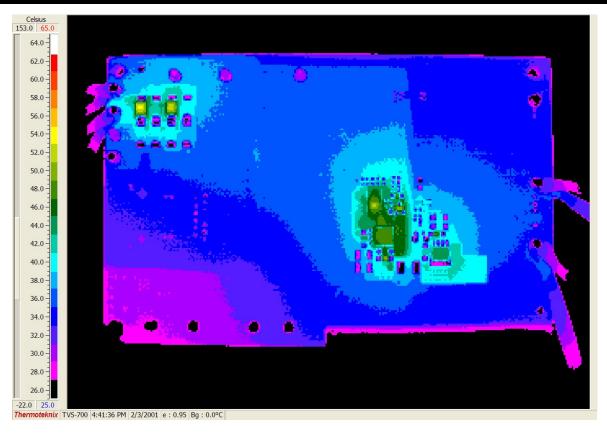


Figure 8. Temp Data (37Vport, 4.5A, Top)



Figure 9. Temp Data (37Vport, 4.5A, Bottom)



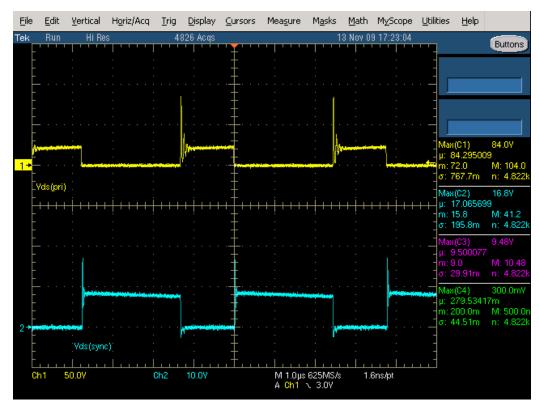


Figure 10. Stresses (9Vaux, 4.5A)

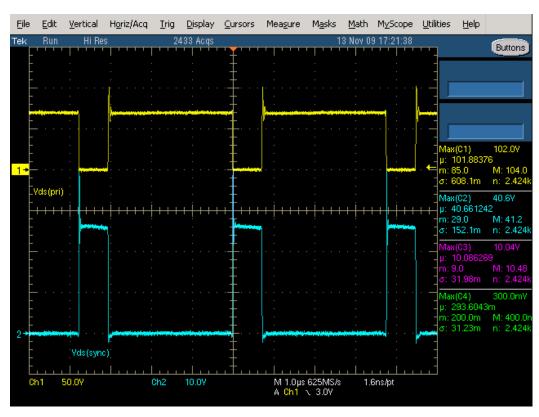


Figure 11. Stresses (57Vaux, 4.5A)



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