DEMO MANUAL DC1763A

LTC2195, LTC2194, LTC2193, LTC2192, LTC2191, LTC2190
16-Bit, 25Msps to 125Msps Dual ADCs

DESCRIPTION

Demonstration circuit 1763A supports a family of 16-Bit 25Msps to 125Msps ADCs. Each assembly features one of the following devices: LTC®2195, LTC2194, LTC2193, LTC2192, LTC2191, LTC2190 high speed, dual ADCs.

The versions of the 1763A demo board are listed in Table 1. Depending on the required resolution and sample rate, the DC1763A is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 140MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo

Table 1. DC1763A Variants

DC1763A VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1763A-A	LTC2195	16-Bit	125Msps	5MHz to 140MHz
1763A-B	LTC2194	16-Bit	105Msps	5MHz to 140MHz
1763A-C	LTC2193	16-Bit	80Msps	5MHz to 140MHz
1763A-D	LTC2192	16-Bit	65Msps	5MHz to 140MHz
1763A-E	LTC2191	16-Bit	40Msps	5MHz to 140MHz
1763A-F	LTC2190	16-Bit	25Msps	5MHz to 140MHz

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage – DC1763A	Depending on Sampling Rate and the A/D Converter Provided, this Supply Must Provide up to 500mA.	3	3.6	6	V
Analog Input Range	Depending on SENSE Pin Voltage	1		2	V_{P-P}
Logic Input Voltages	Minimum Logic High Maximum Logic Low		1.3 0.6		V V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode) Common Mode Minimum Logic Levels (100Ω Load, 3.5mA Mode) Common Mode		350 1.25 247 1.25		mV V mV V
Sampling Frequency (Convert Clock Frequency)	See Table 1				
Encode Clock Level	Single-Ended Encode Mode (ENC^- Tied to GND) Differential Encode Mode (ENC^- Not Tied to GND)	0 0.2		3.6 3.6	V V
Resolution	See Table 1				
Input Frequency Range	See Table 1				
SFDR	See Applicable Data Sheet				
SNR	See Applicable Data Sheet				

QUICK START PROCEDURE

Demonstration circuit 1763A is easy to set up to evaluate the performance of the LTC2195 A/D converter family. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

Setup

If a DC1371 PStache Data Acquisition and Collection System was supplied with the DC1763A demonstration circuit, follow the DC1371 Quick Start Guide to install the required software and for connecting the DC1371 to the DC1763A and to a PC.

DC1763A Demonstration Circuit Board Jumpers

The DC1763A demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1)

J1 PAR/SER: Selects parallel or serial programming mode. (default: serial)

Optional Jumpers:

J8 Term: Enables/Disables optional output termination. (default: removed)

J5 ILVDS: Selects either 1.75mA or 3.5mA of output current for the LVDS drivers. (default: removed)

J14 LANE: Selects either 1-lane or 2-lane output modes (default: removed) NOTE: The DC1371 does not support 1-lane operation.

J15 SHDN: Enables and disables the LTC2195. (default: removed)

J2 WP: Enable/Disables write protect for the EEPROM. (default: removed)

Note: optional jumper should be left open to ensure proper serial configuration.

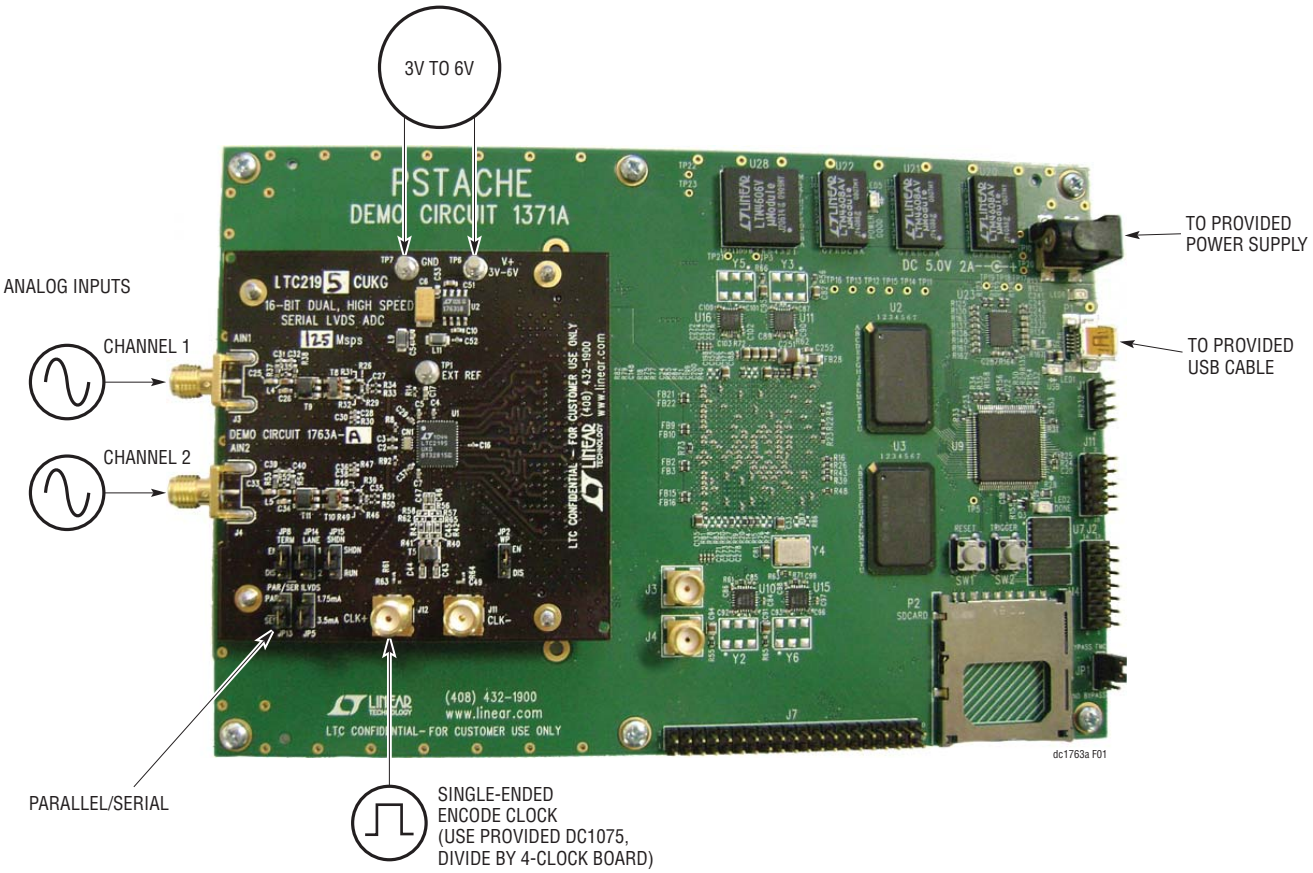


Figure 1. Demo Board Setup

QUICK START PROCEDURE

Applying Power and Signals to the DC1763A Demonstration Circuit

If a DC1371 is used to acquire data from the DC1763A, the DC1371 must FIRST be connected to a powered USB port and have 5V applied power BEFORE applying 3.6V to 6V across the pins marked V^+ and GND on the DC1763A. DC1763A requires 3.6V for proper operation.

Regulators on the board produce the voltages required for the ADC. The DC1763A demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC1763A should not be removed, or connected to the DC1371 while power is applied.

Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 140MHz, refer to the LTC2195 data sheet for a proper input network. Other input networks may be more appropriate for input frequencies less that 5MHz.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Apply the analog input signal of interest to the SMA connectors on the DC1763A demonstration circuit board marked J3 AIN1 and J4 AIN2. These inputs correspond with channels one and two of the ADC respectively. These inputs are capacitively coupled to balun transformers ETC1-1-13 (lead free part number MABA007159-000000).

Encode Clock

NOTE: Apply an encode clock to the SMA connector on the DC1763A demonstration circuit board marked J11 CLK^+. As a default the DC1763A is populated to have a single-ended input.

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator a squaring circuit can be used. Linear Technology also provides demo board DC1075 that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2195. Using band pass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1763A a band pass filter used for the clock should be used prior to the DC1075. Data sheet FFT plots are taken with 10-pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used for both the clock input and the analog input.

Digital Outputs

The data outputs, data clock, and frame clock signals are available on J1 of the DC1763A. This connector follows the VITA-57/FMC standard, but all signals should be verified when using an FMC carrier card other than the DC1371.

Software

The DC1371 is controlled by the PScope™ System Software provided or downloaded from the Linear Technology website at http://www.linear.com/software/.

To start the data collection software if PScope.exe, is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

QUICK START PROCEDURE

If the DC1763A demonstration circuit is properly connected to the DC1371, PScope should automatically detect the DC1763A, and configure itself accordingly. If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371 Quick Start Guide and in the online help available within the PScope program itself.

Serial Programming

PScope has the ability to program the DC1763A board serially through the DC1371. There are several options available in the LTC2195 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 2).

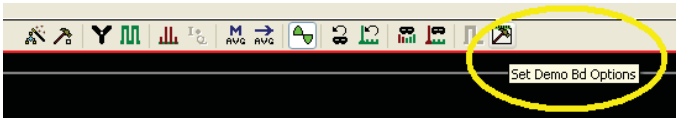


Figure 2. PScope Toolbar

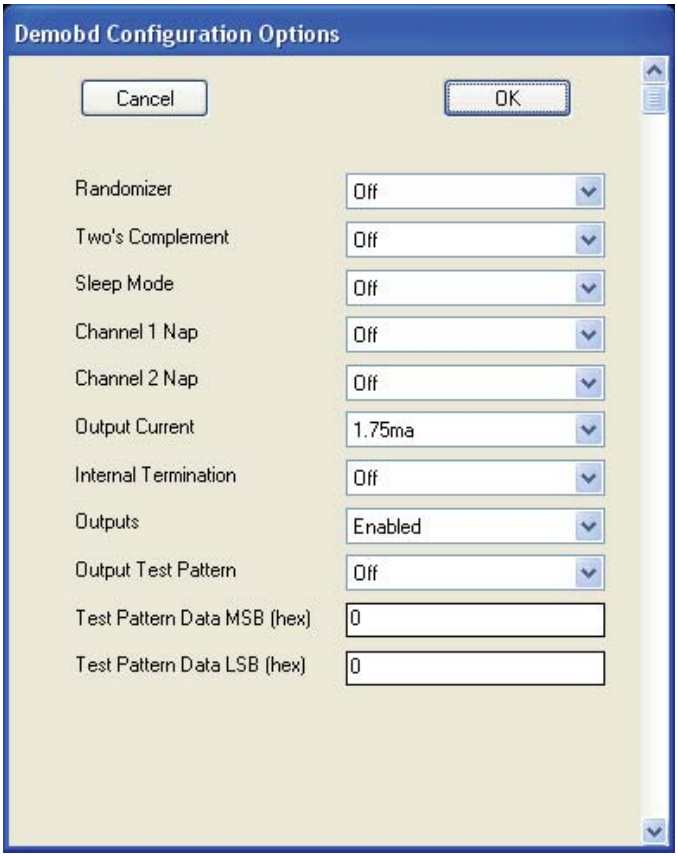


Figure 3. Demobd Configuration Options

This will bring up the menu shown in Figure 3.

This menu allows any of the options available for the LTC2195 family to be programmed serially. The LTC2195 family has the following options:

Randomizer: Enables data output randomizer

- Off (Default): Disables data output randomizer
- On: Enables data output randomizer

Two's Complement: Enables two's complement mode

- Off (Default): Selects offset binary mode
- On: Selects two's complement mode

Sleep Mode: Selects between normal operation, sleep mode:

- Off (Default): Entire ADC is powered, and active
- On: The entire ADC is powered down.

QUICK START PROCEDURE

Channel 1 Nap: Selects between normal operation and putting channel 1 in nap mode.

- Off (Default): Channel one is active
- On: Channel one is in nap mode

Channel 2 Nap: Selects between normal operation and putting channel 2 in nap mode.

- Off (Default): Channel two is active
- On: Channel two is in nap mode

Output Current: Selects the LVDS output drive current

- 1.75mA (Default): LVDS output driver current
- 2.1mA: LVDS output driver current
- 2.5mA: LVDS output driver current
- 3.0mA: LVDS output driver current
- 3.5mA: LVDS output driver current
- 4.0mA: LVDS output driver current
- 4.5mA: LVDS output driver current

Internal Termination: Enables LVDS internal termination

- Off (Default): Disables internal termination
- On: Enables internal termination

Outputs: Enables digital outputs

- Enabled (Default): Enables digital outputs
- Disabled: Disables digital outputs

Test Pattern: Selects digital output test patterns. The desired test pattern can be entered into the text boxes provided.

- Off(default): ADC input data is displayed
- On: Test pattern is displayed.

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1763A demo board.

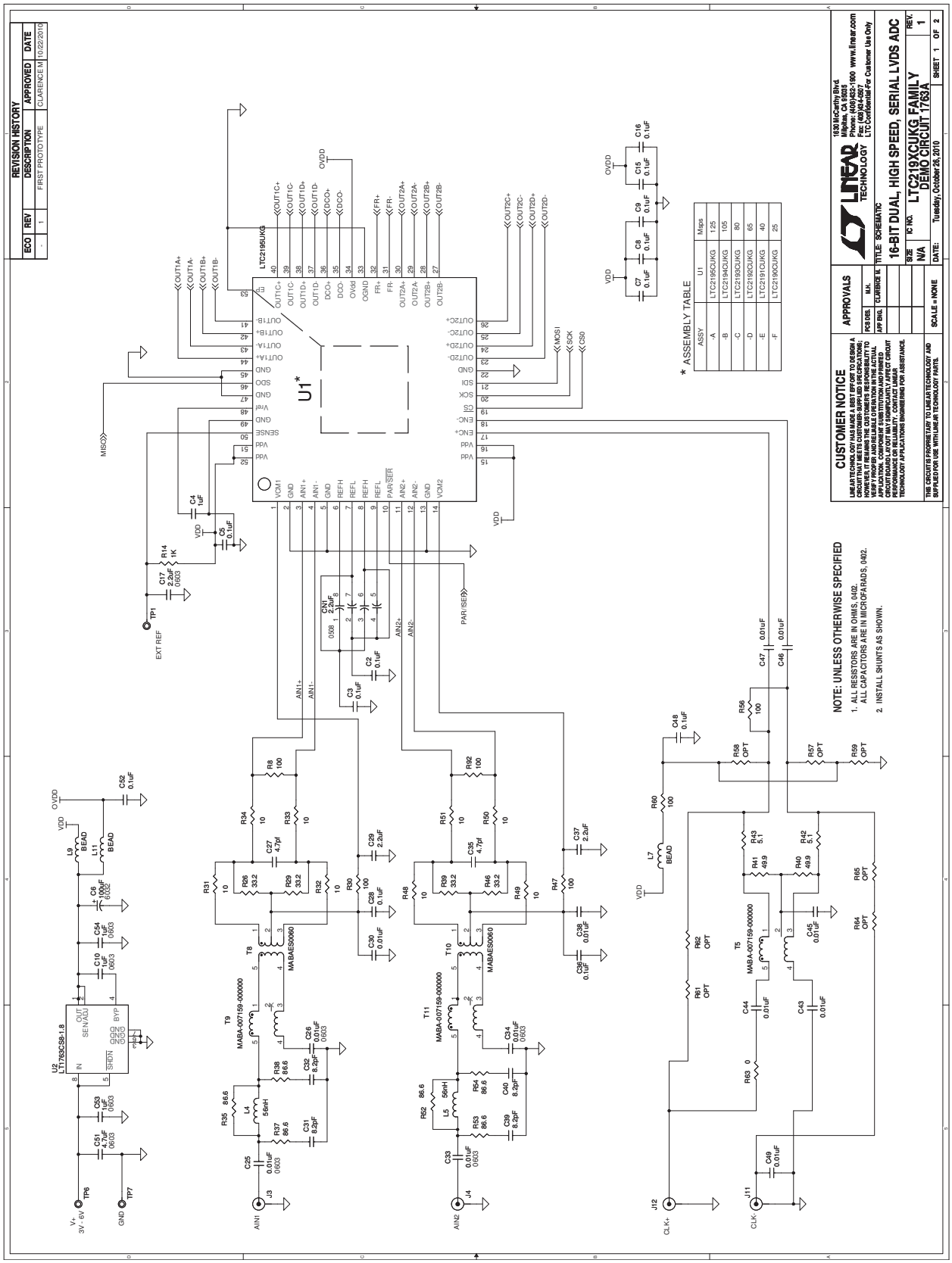
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CN1	Capacitor, Array, 0508, 2.2µF, 20%, 4V, X5R	AVX, W2L14D225MAT1A
2	13	C2, C3, C5, C7, C8, C9, C15, C16, C18, C28, C36, C48, C52	Capacitor, X5R, 0.1µF, 10V, 10%, 0402	AVX, 0402ZD104KAT2A
3	1	C4	Capacitor, X5R, 1µF, 10V, 10%, 0402	AVX, 0402ZD105KAT2A
4	1	C6	Capacitor, Tantalum, 100µF, 16V, 10%, 6032	AVX, TPSC107K016R0200
5	3	C10, C53, C54	Capacitor, X7R, 1µF, 10V, 10%, 0603	AVX, 0603ZC105KAT2A
6	1	C17	Capacitor, X5R, 2.2µF, 10V, 20%, 0603	AVX, 0603ZD225MAT2A
7	4	C25, C26, C33, C34	Capacitor, X7R, 0.01µF, 50V, 10%, 0603	AVX, 06035C103KAT2A
8	2	C27, C35	Capacitor, COG, 4.7pF, 50V, 5%, 0402	AVX, 04025A4R7JAT2A
9	2	C29, C37	Capacitor, X5R, 2.2µF, 6.3V, 20%, 0402	AVX, 04026D225MAT2A
10	7	C30, C38, C43-C47	Capacitor, X7R, 0.01µF, 16V, 10%, 0402	AVX, 0402YC103KAT2A
11	4	C31, C32, C39, C40	Capacitor, COG, 8.2pF, 50v, 5%, 0402	AVX, 04025A8R2JAT2A
12	1	C49	Capacitor, X7R, 0.01µF, 25V, 10%, 0402	AVX, 04023C103KAT2A
13	1	C51	Capacitor, X5R, 4.7µF, 6.3V, 20%, 0603	AVX, 06036D475MAT2A
14	1	J1	BGA Connector, 40 × 10	Samtec, SEAM-40-02.0-S-10-2-A
15	6	JP2, JP5, JP8, JP13, JP14, JP15	Header, 3-Pin, 0.079, Single Row	Samtec, TMM-103-02-L-S
16	2	J3, J4	Connector, SMA 50Ω, Edge-Launch	E. F. Johnson, 142-0701-851
17	2	J11, J12	Connector, SMA Jack, Straight, Thru-Hole	Amphenol Connex, 132134
18	2	L4, L5	Inductor, 56nH, 0603	Murata, LQP18MN56NG02D
19	1	L7	Ferrite Bead, 0603	Murata, BLM18BB470SN1D
20	2	L9, L11	Ferrite Bead, 1206	Murata, BLM31PG330SN1L
21	2	R1, R63	Resistor, Chip, 0Ω 0402	Yageo, RC0402FR-070RL
22	0	R2, R57-R59, R61, R62, R64, R65	OPT, Resistor, Chip, 0402	
23	12	R4, R5, R10, R36, R102-R109	Resistor, Chip, 10k, 1/16W, 5%, 0402	Yageo, RC0402JR-0710KL
24	2	R8, R92	Resistor, Chip, 100Ω, 1/16W, 1%, 0402	Yageo, RC0402FR-07100RL
25	6	R9, R11, R14, R72, R73, R74	Resistor, Chip, 1k, 1/16W, 5%, 0402	Yageo, RC0402JR-071KL
26	1	R12	Resistor, Chip, 31.6k, 1/16W, 1%, 0402	Yageo, RC0402FR-0731K6L
27	4	R26, R29, R39, R46	Resistor, Chip, 33.2Ω, 1/16W, 1%, 0402	Yageo, RC0402FR-0733R2L
28	9	R30, R47, R56, R60, R95-R99	Resistor, Chip, 100Ω, 1/16W, 5%, 0402	Yageo, RC0402JR-07100RL
29	8	R31, R32, R33, R34, R48-R51	Resistor, Chip, 10.0Ω, 1/16W, 1%, 0402	Yageo, RC0402FR-0710RL
30	2	R35, R52	Resistor, Chip, 86.6Ω, 1/16W, 1%, 0402	Yageo, RC0402FR-0786R6L

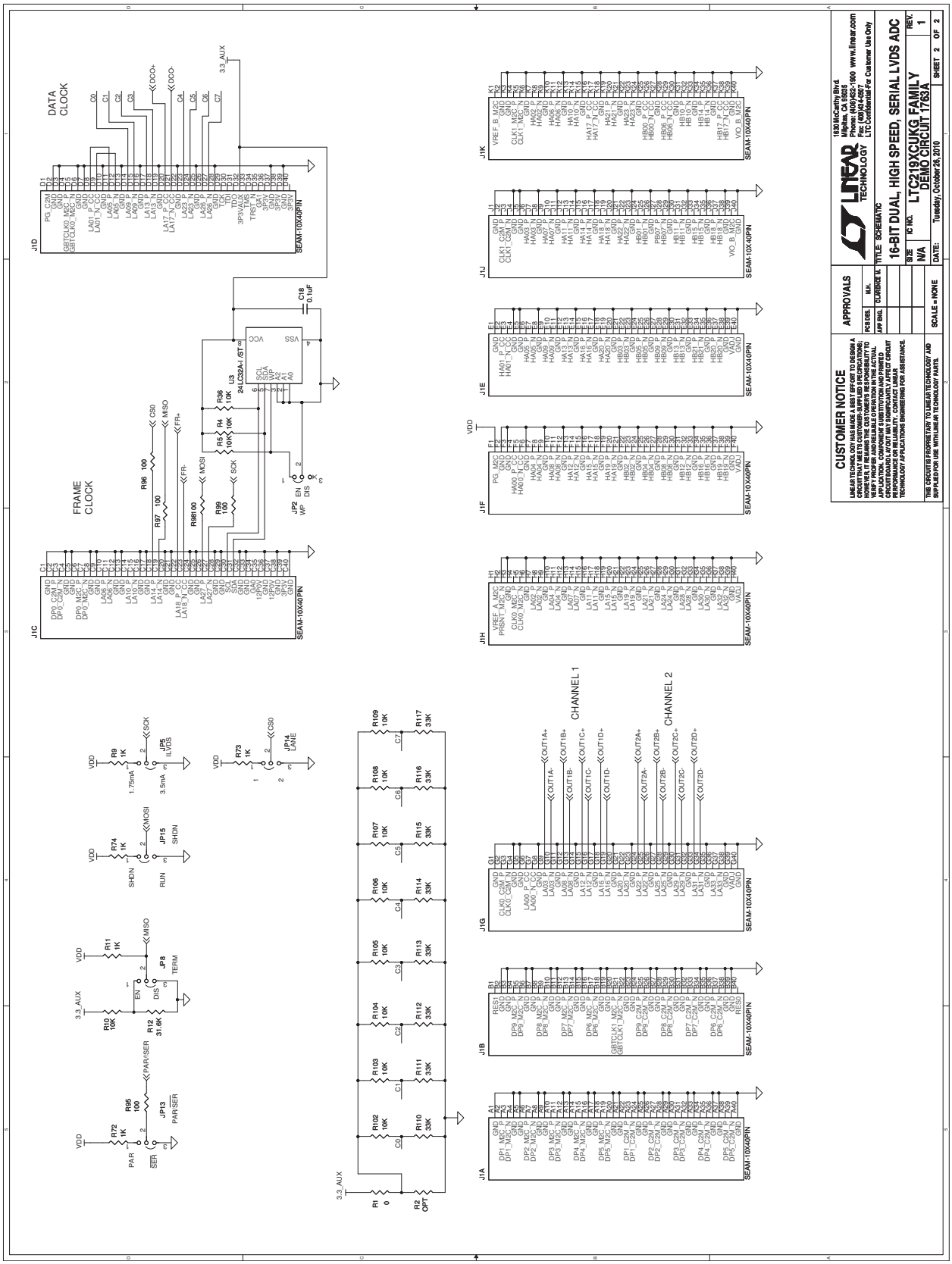
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
31	4	R37, R38, R53, R54	Resistor, Chip, 86.6Ω, 1/16W, 1%, 0603	Yageo, RC0603FR-0786R6L
32	2	R40, R41	Resistor, Chip, 49.9Ω, 1/16W, 1%, 0402	Yageo, RC0402FR-0749R9L
33	2	R42, R43	Resistor, Chip, 5.1Ω, 1/16W, 1%, 0402	Yageo, RC0402FR-075R1L
34	8	R110-R117	Resistor, Chip, 33k, 1/16W, 1%, 0402	Yageo, RC0402FR-0733KL
35	3	TP1, TP6, TP7	Testpoint, Turret, .094, PBF	Mill-Max, 2501-2-00-80-00-00-07-0
36	3	T5, T9, T11	Transformer, RF~SMT~1:1 Balun	Macom, MABA-007159-000000
37	2	T8, T10	Transformer, Flux-Coupled Balun	Macom, MABAES0060
38	1	U2	IC, LT1763CS8-1.8 SO8	Linear Technology, LT1763CS8-1.8#PBF
39	1	U3	IC, EEPROM 32KBIT 400khz 8TSSOP	Microchip, 24LC32A-I/ST
40	6	XJ2, XJ5, XJ8, XJ13, XJ14, XJ15	Shunt, 0.079" Center	Samtec, 2SN-BK-G
41	2		Stencil (Top & Bottom)	Stencil 1763A

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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