# LTC2207, LTC2206, LTC2205, LTC2204, LTC2203, LTC2202

## DESCRIPTION

Demonstration circuit 919 supports members of a family of 16/14 BIT 130 MSPS ADCs. Each assembly features one of the following devices: LTC2207, LTC2206, LTC2205, LTC2204, LTC2203, or LTC2202 high speed, high dynamic range ADCs.

Other members of this family include the LTC2208/LTC2208-14 16/14-Bit 130Msps ADC with LVDS outputs. These 9x9mm QFN devices are supported by Demonstration circuit 854 (CMOS outputs only) or by Demonstration circuit 996 (LVDS outputs).

Several versions of the 919A demo board supporting a single ended clock input, specifically targeted for use with the 25Msps LTC2203 and 10Msps LTC2202 A/D converters, are listed in Table 1. LTC2204, LTC2205, LTC2206 and LTC2207 have differential clock inputs but use a single ended clock input for evaluation with the DC input on the DC919 board. Depending on the required sample rate and input frequency, the DC919 is supplied with the appropriate ADC and with an optimized input circuit. The circuitry on the analog inputs is optimized for analog input frequencies from DC to 70MHz or from 1MHz to 70MHz if using the transformer coupled input. For higher input frequencies, contact the factory for support.

**Design files for this circuit board are available. Call the LTC factory.**

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**Table 1. DC919A Variants**

| DC919 VARIANTS | ADC PART NUMBER | RESOLUTION* | MAXIMUM SAMPLE RATE | INPUT FREQUENCY |
|---|---|---|---|---|
| 919A-A | LTC2207 | 16-Bit | 105Msps | DC - 70MHz |
| 919A-B | LTC2206 | 16-Bit | 80Msps | DC - 70MHz |
| 919A-C | LTC2205 | 16-Bit | 65Msps | DC - 70MHz |
| 919A-D | LTC2204 | 16-Bit | 40Msps | DC -70MHz |
| 919A-E | LTC2203 | 16-Bit | 25Msps | DC - 70MHz |
| 919A-F | LTC2202 | 16-Bit | 10Msps | DC - 70MHz |

**Table 2. Performance Summary (T$_A$ = 25°C)**

| PARAMETER | CONDITION | VALUE |
|---|---|---|
| Supply Voltage | Depending on sampling rate and the A/D converter provided, this supply must provide up to 500mA. | Optimized for 3.3V [3.15V ⇔3.45V min/max] |
| Analog input range | Depending on PGA Pin Voltage | 1.5V$_{PP}$ to 2.25V$_{PP}$ |
| Logic Input Voltages | Minimum Logic High | 2.4V |
| | Maximum Logic Low | 0.8V |
| Logic Output Voltage (74VCX245 output buffer, V$_{cc}$ = 2.5V) | Minimum Logic High @ -1.6mA | 2.3V (33Ω Series terminations) |
| | Maximum Logic Low @ 1.6mA | 0.7V (33Ω Series terminations) |
| Sampling Frequency (Convert Clock Frequency) | See Table 1 | |
| Convert Clock Level | 50 Ω Source Impedance, AC coupled or ground referenced (Convert Clock input is capacitor coupled on board and terminated with 50Ω.) | 2V$_{P-P}$ ⇔2.5V$_{P-P}$ Sine Wave or Square wave |
| Resolution | See Table 1 | |
| Input frequency range | See Table 1 | |
| SFDR | See Applicable Data Sheet | |
| SNR | See Applicable Data Sheet | |

# QUICK START PROCEDURE

Demonstration circuit 919 is easy to set up to evaluate the performance of the LTC2207, LTC2206, LTC2205, LTC2204, LTC2203, or LTC2202 A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

### SETUP

If a DC718 QuickDAACS Data Analysis and Collection System was supplied with the DC919 demonstration circuit, follow the DC718 Quick Start Guide to install the required software and for connecting the DC718 to the DC919 and to a PC running Windows98, 2000 or XP.
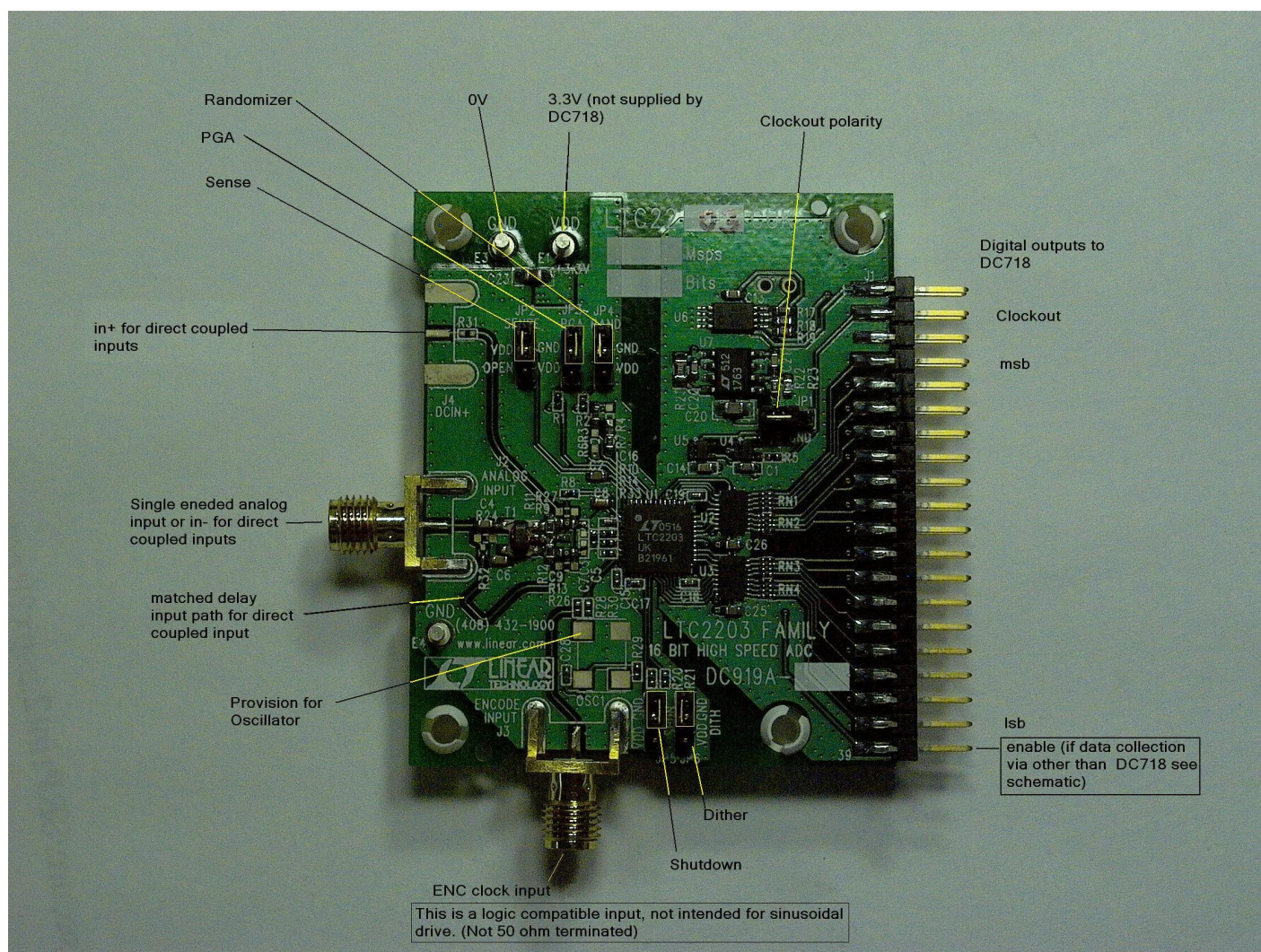
**Figure 1. DC919 Setup (zoom in for detail)**

## DC919 DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC919 demonstration circuit board should have the following jumper settings as default: (as per figure 1)

JP1: Output clock polarity: GND
JP2: SENSE: VDD, (Internal reference)
JP3: PGA:   GND    2.25V range
JP4: RAND: GND    Not randomized
JP5: SHDN: GND    Not Shutdown
JP6: DITH:   GND    No internal dithering

## APPLYING POWER AND SIGNALS TO THE DC919 DEMONSTRATION CIRCUIT

If a DC718 is used to acquire data from the DC919, the DC718 must FIRST be connected to a powered USB port or provided an external 6-9V BEFORE applying +3.3V across the pins marked "+3.3V" and "PWR GND" on the DC919. The DC919 demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC718 data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an un-powered hub in which case it must be supplied an external 6-9V on turrets G7(+) and G1(-) or the adjacent 2.1mm power jack.

## ENCODE CLOCK

**NOTE: This is a logic compatible input, contrary to the majority of Linear technology ADC demo boards. It is not terminated with 50Ω.**

Apply an encode clock to the SMA connector on the DC919 demonstration circuit board marked "J3 ENCODE INPUT".

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter source. A low jitter 3.3V oscillator with direct connection through a barrel is recommended.

If using a sinusoidal generator, the amplitude should be as large as possible, up to $3V_{P-P}$ or 13dBm, filtered and terminated with a 50Ω thru-terminator. If a generator with 50Ω output impedance is connected via a cable, it is recommended that a thru-terminator be used. However, below 15 MHz, it is recommended that a square wave drive be used.

If a sinusoidal ground referenced signal, or an AC coupled signal is used, 1.5V-1.7V DC bias must be introduced via a bias tee.

DC919 has provision for a popular surface mount oscillator form and some population options to select this as the clock source. (Please see schematic.)

If only sinusoidal or clipped sinusoid signal sources are available as the clock source for scenarios involving sampling rates less than 15-20Msps, it is recommended that a divide by 4 or divide by 8 be used. If the converter is to be used at very low sampling rates approaching the minimum, a higher divide ratio may be required. This is especially important if under-sampling.

If you want to use these converters at less than the minimum sampling rate, it is recommended that you run the ADC above the minimum rate, and decimate. If over-sampling low frequencies, the use of a sinusoid is potentially acceptable, but it must be very clean or the low dVdT will result in a great sensitivity to wideband noise in the clock driver. .

The use of a divider may require a band-pass filter prior to the divider in order to achieve best SNR as the divider can exaggerate phase noise if it is sensitive to GHz frequencies. Contact Linear technology for recommendations or in some cases, available clock sources or dividers.

Most generators require filtering or they will compromise both the SNR and the SFDR of the ADCs.

Generally datasheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics,

non-harmonically related spurs and broad band noise. Low phase noise Agilent 8644B generators are used with TTE band pass filters for both the Clock input and the Analog input. In the case of the LTC2203/2 we use a divide by 4.

This demo board is, populated by default for the dc input path. There is a transformer mounted at T1, but C4, C6, R9 and R13 are not populated. If a single ended AC input is required, the DC input paths must be disconnected by removing R26,27,31 & 32, and the above components installed.

If the transformer input is required, C4 & C6 should be 0.1uF X5R 0402, R9 and R13 should be 10 ohm 0402 resistors.

Note that this transformer (ETC1-1T) is poor below 1 MHz.

Reduced amplitude signals can be applied to 300 KHz. Applications below 300 KHz must be driven directly via DC inputs.

As there are a significant number of these boards that are customized, please confirm the population of your board. The schematic below shows the default population, the photograph shows the population of a transformer coupled version. This board may also be populated with LTC2204-2207 for DC drive applications, in which case, R33 is a 0.1uF capacitor.

Apply the analog input signal of interest to the SMA connector on the DC919 demonstration circuit board marked "J2 ANALOG INPUT". These inputs are capacitive coupled to a Flux coupled transformers ETC1-1T. In some cases, where these devices are to be used in under-sampling scenarios, this transformer should be replaced with an ETC1-1-13 Balun.

The DC919 can be modified for direct DC drive from a suitable differential signal source.

This may be done by yourself or at special request when you order the demo board.

If the DC input paths are populated with low value (5.1 ohm) resistors at both ends of these transmission lines, you must provide a reasonably well balanced differential drive with 1.25V common mode.

The spacing of these SMA connectors (0.8") allows them to be mated directly with demo boards for devices such as the LT1993, LT1994, LT5514 and others.

It is not recommended to drive this ADC in a single ended fashion into a single DC input.

An internally generated conversion clock output is available on pin 3 of J1 and the data samples are available on Pins 7-37 of J1 which can be collected via a logic analyzer, cabled to a development system through a SHORT 2 to 4 inch long 40-pin ribbon cable or collected by the DC718 QuickEval-II Data Acquisition Board using the *PScope System Software* provided or down loaded from the Linear Technology website at http://www.linear.com/software/. If a DC718 was provided, follow the DC718 Quick Start Guide and the instructions below.

If data is to be collected by a logic analyzer, pin 40 must be strapped to OVDD or 2.5V.

(Please see schematic.)

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

Configure PScope for the appropriate variant of the DC919 demonstration circuit by selecting the correct A/D Converter as installed on the DC919. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select device, either LTC2202, LTC2203 or any of the pin-compatible 14-Bit and 16-Bit parts up to LTC2207. Select the part in the Device List and PScope will automatically blank the last two LSBs when using a DC919 supplied with a 14-Bit part. If you are operating with a

version of PScope that does not include these parts in the device menu, you may manually configure as:

User configure

16-Bit (or 14-Bit if using -14 versions)

Alignment: Left-16

Bipolar (2's complement)

Positive clock edge

Type: CMOS

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for *PScope* is available in the DC718 Quick Start Guide and in the online help available within the *PScope* program itself.

## ANALOG INPUT NETWORK

For optimal distortion and noise performance the RC network on the analog inputs should be optimized for different analog input frequencies. At this point in time, the circuit in Fig. 3 for input frequencies below 70MHz. For input frequencies from 70MHz to 140MHz, the circuit in Fig. 2 is used. These two input networks cover a broad bandwidth and are not optimized for operation at a specific input frequency.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

Narrow band high Q filters may produce poor SNR results with Dither enabled. 10% band-pass would be preferred over 5% band-pass on the analog input. The filters should be located close to the inputs to avoid reflections from impedance disconti-

nuities at the driven end of a long transmission line. Most filters do not present 50 ohms outside the pass-band.

In cases with long transmission lines, 3-10dB pads may be required to obtain low distortion.

If your generator cannot deliver full scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

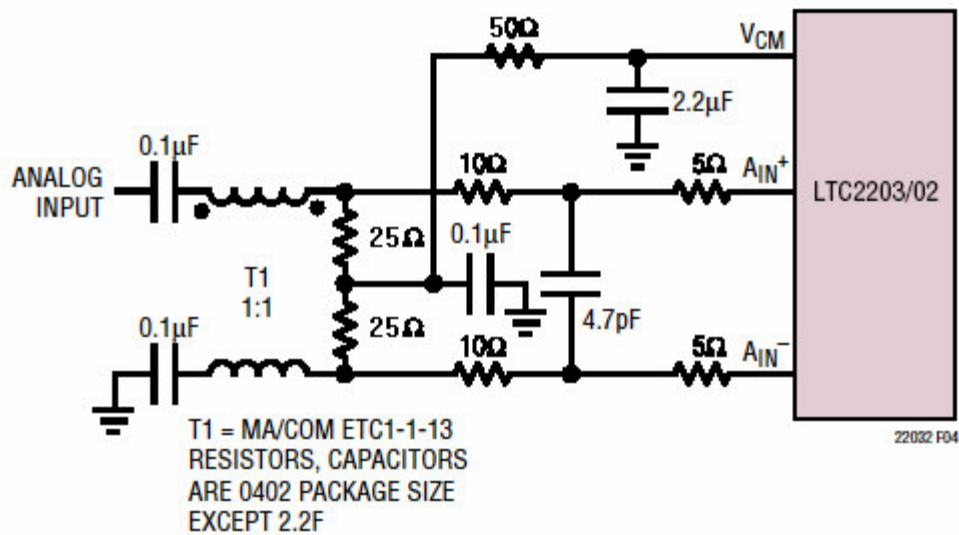For advice on drive circuits or for input frequencies greater than 70MHz contact the factory for support.

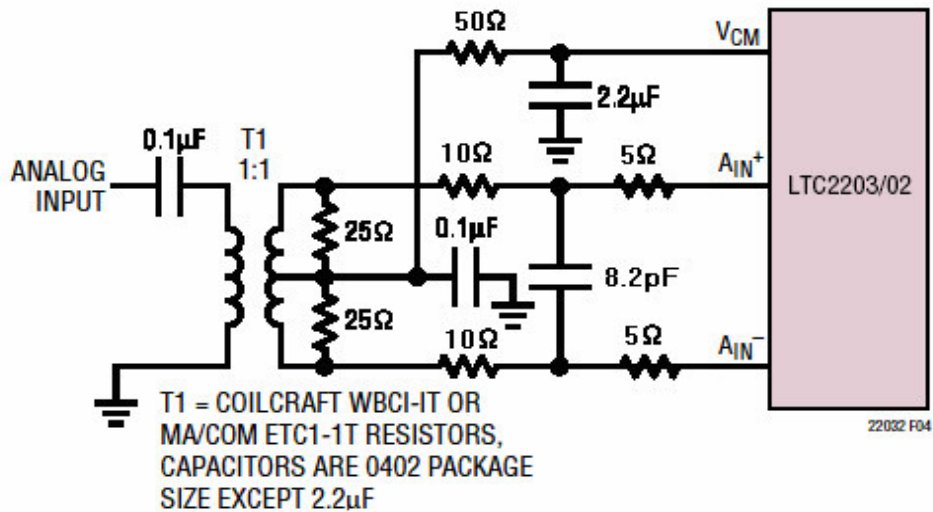**Figure 2.   Analog Front End Circuit For 70MHz+ (1 of 2)**



**Figure 3.   Analog Front End Circuit For 1MHz < $A_{IN}$ < 70MHz (1 of 2)**

For input frequencies less than 5MHz, or greater than 150MHz, other input networks may be more appropriate. Please consult the factory for suggestions on drivers and networks if your signal sources extend outside these ranges, or if you experience difficulties driving these suggested networks.

**VERSION TABLE**

| Assembly Type | U1 | R33 | INPUT FREQUENCY | Bits | Msps |
|---|---|---|---|---|---|
| DC919A-A | LTC2207CUK | 0.01uF | DC < Ain < 70MHz | 16 | 105 |
| DC919A-B | LTC2206CUK | 0.01uF | DC < Ain < 70MHz | 16 | 80 |
| DC919A-C | LTC2205CUK | 0.01uF | DC < Ain < 70MHz | 16 | 65 |
| DC919A-D | LTC2204CUK | 0.01uF | DC < Ain < 70MHz | 16 | 40 |
| DC919A-E | LTC2208CUK | 0 OHM | DC < Ain < 70MHz | 16 | 25 |
| DC919A-F | LTC2202CUK | 0 OHM | DC < Ain < 70MHz | 16 | 10 |

LTC2203 FAMILY
16 BIT HIGH SPEED ADC
DWG NO. DC919A