GaN HEMT Bias Sequencing and Temperature Compensation Circuit

INTRODUCTION

This application note outlines a bias sequencing circuit that can be used in conjunction with Wolfspeed RF GaN HEMT devices. Under normal operation all Wolfspeed GaN RF devices require a negative gate voltage and positive drain voltage for operation, with the gate voltage having to be applied first to prevent failure.

The bias sequencing circuit presented here uses a single DC power supply for both the gate and drain. The circuit topology prevents any failures by not applying drain voltage until a negative gate voltage is ready and DC input voltage is higher than 16V to prevent low voltage issues. The quiescent current (Idq) of the device is adjusted using a potentiometer and the gate bias temperature compensation circuit can be enabled/disabled as needed.

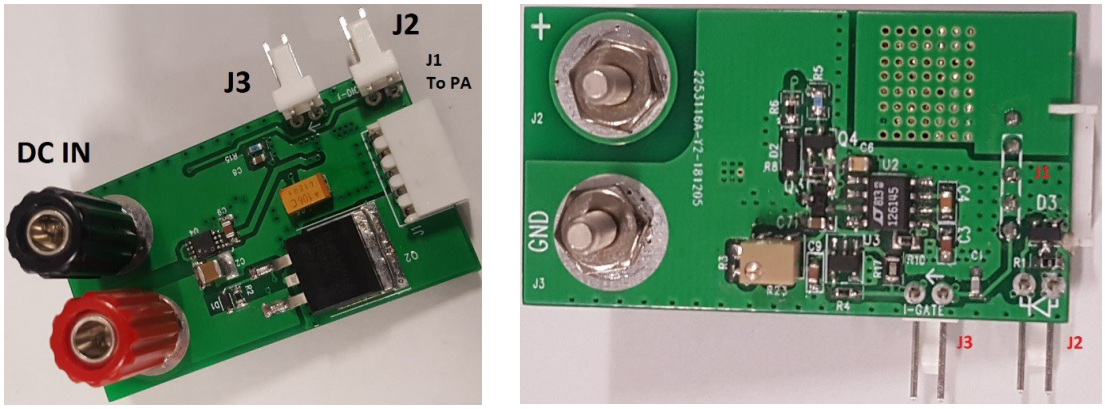

Figure 1. GaN Device Biasing Control Board

CIRCUIT OPERATION

Figure 1 shows an image of the board and Figure 2 shows an image of the circuit block diagram. The input to the circuit is a single DC power (DC IN, 20V to 50V) and the optional board temperature sensing line to J2 (which can be shorted to disable temperature compensation). J3 is for gate current measurement which must be shorted if no measurement is required (shorted by default). Drain DC, gate biasing voltage and ground are connected by J1 to a Wolfspeed application fixture.

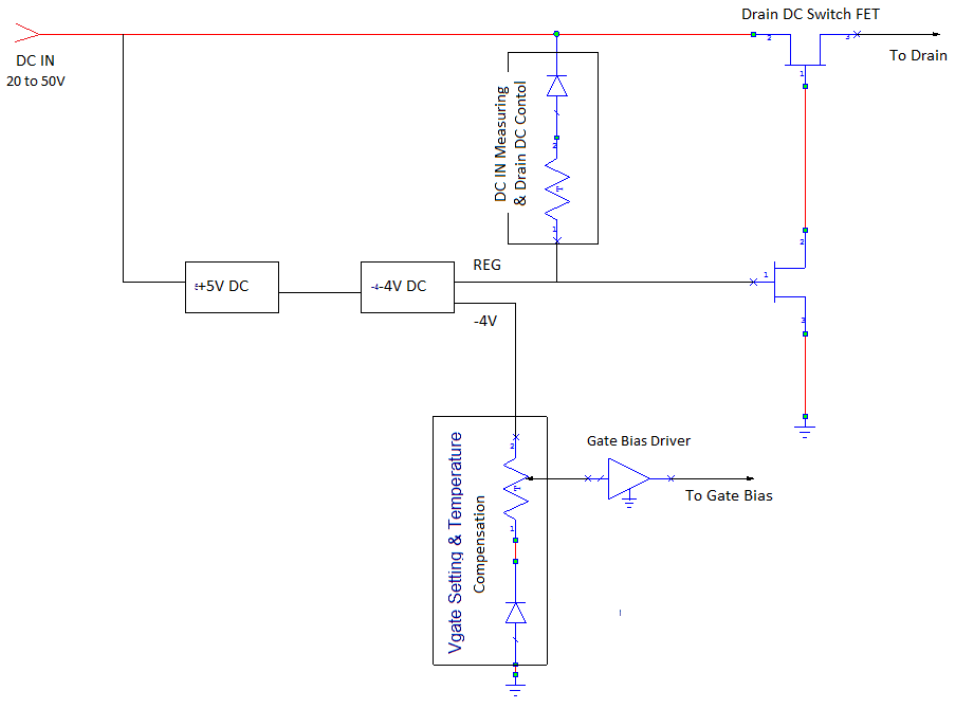

Figure 2. GaN Biasing Control Board Block Diagram

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The drain DC switching control circuit shown in Figure 3 uses a high voltage, low turn-on resistance P-channel power FET (Q2) to control the DC power applied to the drain of the GaN device. A 60V wide DC input low drop regulator (U4) with 100mA current capability regulates the DC input to positive 5V that connects to the switch capacitor regulated voltage inverter's (U2) DC input. The inverter provides a -4.5V with 15mA current capability DC supply for the gate of the GaN RF transistor and a Negative Ready REG signal output for the drain DC power control. When the negative voltage is not ready (within 5% of the set value of -4.5V), U2 REG pin is high, Q3 will be turned on, preventing Q2 from turning on and causing the device to fail. Similarly, if the DC input voltage is lower than 16V (determined by the Zener voltage of D2 and Q4 threshold) Q2 will remain off to prevent any possible low voltage oscillations.

The inverter's negative output is connected to the gate biasing setting and temperature compensation circuit for setting the GaN gate bias voltage for temperature compensation capability. This voltage is led to an operational amplifier (U3) to drive the GaN transistor's gate biasing circuit.

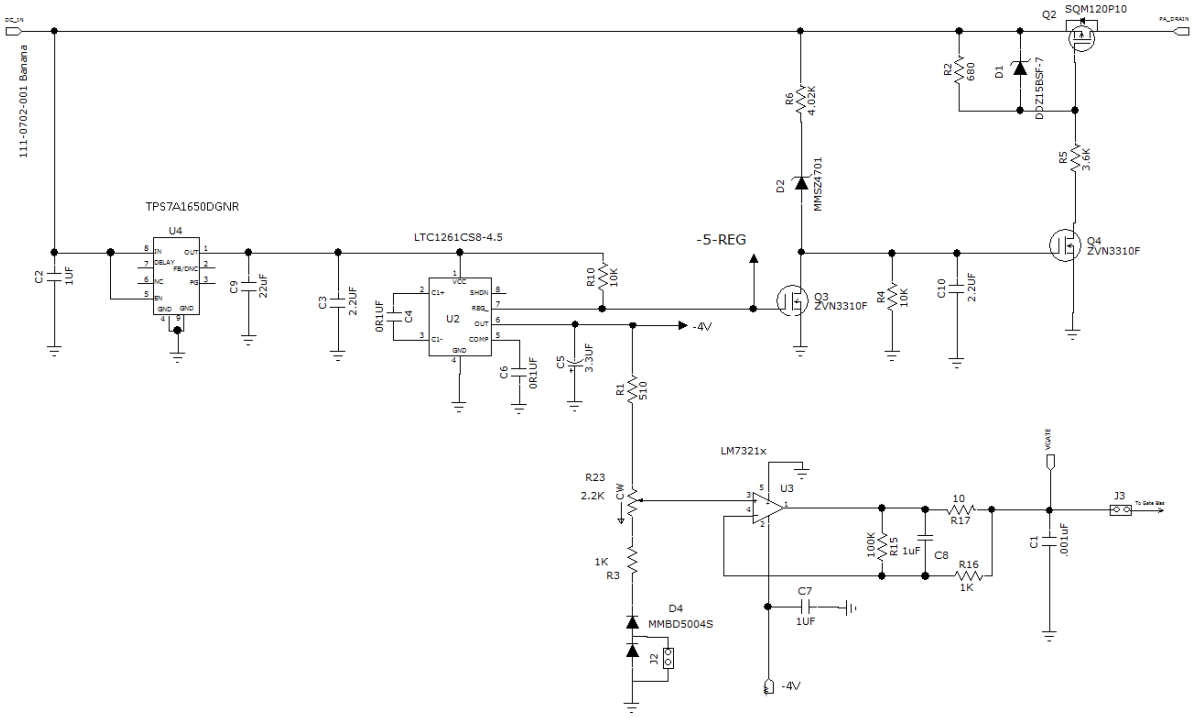

Figure 3. Whole GaN Biasing Sequence and Temperature Compensation Circuit

GaN HEMT Bias Sequencing and Temperature Compensation Circuit

Table 1. Bill of Materials

DESIGNATOR	DESCRIPTION	QTY
C1	CAPACITOR, 0603, 0.001uF,10%	1
C4, C6	CAPACITOR, 0805, 0R1UF, 50V, 20%	2
C5	CAPACITOR, 10%, SMT3216, 10uF, 16V Tantum	1
C2	CAPACITOR, 0805 100V 10% X7R 1UF	1
C3	CAPACITOR, 0603,2.2UF, 25V, 20%	1
C7 ,C8, C9	CAPACITOR, SMT0603,1UF, 25V, 20%	3
D1	ZENER SOD-323 DDZ15BSF-7 3% 15V	1
D2	SMT-ZENER-MMSZ4701	1
D3	DIODE, MMBD5004S-SOT-23	1
Q3, Q4	ZVN3310F-SOT-23	2
Q2	FET-P-SMT-SQM120P10-D2PAK	1
U3	LM7321MF/NOPB-SOT23-5	1
U2	SO-8, LTC1261CS8-4.5	1
U4	TPS7A1650DGNR 60V INPUT, 5V output	1
R1	RESISTOR, 0603-ROHS, 0 OHM,5%	1
R3	RESISTOR, 0603, 1K-1%	1
R5	RESISTOR, 0805, 3.6 K, 1%	1
R8	RESISTOR 0603 .1W 22.1K, 1%	1
R10	RESISTOR, 0603, 4.7K, 1%	1
R2	RESISTOR, 0805, 680 OHM,1%	1
R6	RESISTOR, 0805, 4.03 K, 1%	1
R15	RESISTOR, 0603,100K, 1%	1
R4	RESISTOR, 0603 .1W, 845 OHM, 1%	1
R16	RESISTOR, 0603, 1K,1%	1
R17	RESISTO, 0805, 10 OHM,1%	1
R23	SMT, POT, 2K-1/4W, 3224W-1-202E Bourns	1
J2, J3	2 pin male 77311-118-02LF, Amphenol ICC (FCI)	2
J1	MOLEX 38001335, 5 Position Receptacle Connector 0.100” (2.54mm) Board Edge, Through Hole, Right Angle	1
JDC +	111-0702-001, CONN BIND POST KNURLED RED	1
JDC GNDw	111-0703-001, CONN BIND POST KNURLED BLACK	1

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Table 2. Bias Control Boards

PART NUMBER	DESCRIPTION
CGB5P-CEN	Gate Biasing Assy, GaN, 5 PIN
CGB9P-CEN	Gate Biasing Assy, GaN, 9 PIN (Pin 5 gate control)
CGB9P-SIDE	Gate Biasing Assy, GaN, 9 PIN (Pin 1&2 gate control)