Evaluating the ADRF5048, Silicon SP4T Switch, Nonreflective, 100 MHz to 45 GHz

FEATURES

- Full featured evaluation board for the ADRF5048
- Simple connection to test equipment
- Thru line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5048 is a SP4T, nonreflective switch manufactured in the silicon process.

This user guide describes the ADRF5048-EVALZ evaluation board, which was designed to simply evaluate the features and performance of the ADRF5048. A photograph of the evaluation board is shown in Figure 1.

Note that the ADRF5048 IC is populated on the ADRF5042 bare evaluation board. However, the whole assembly is the ADRF5048-EVALZ.

The ADRF5048 data sheet provides full specifications for the ADRF5048. Consult the ADRF5048 data sheet in conjunction with this user guide when using the ADRF5048-EVALZ.

ADRF5048-EVALZ EVALUATION BOARD PHOTOGRAPH

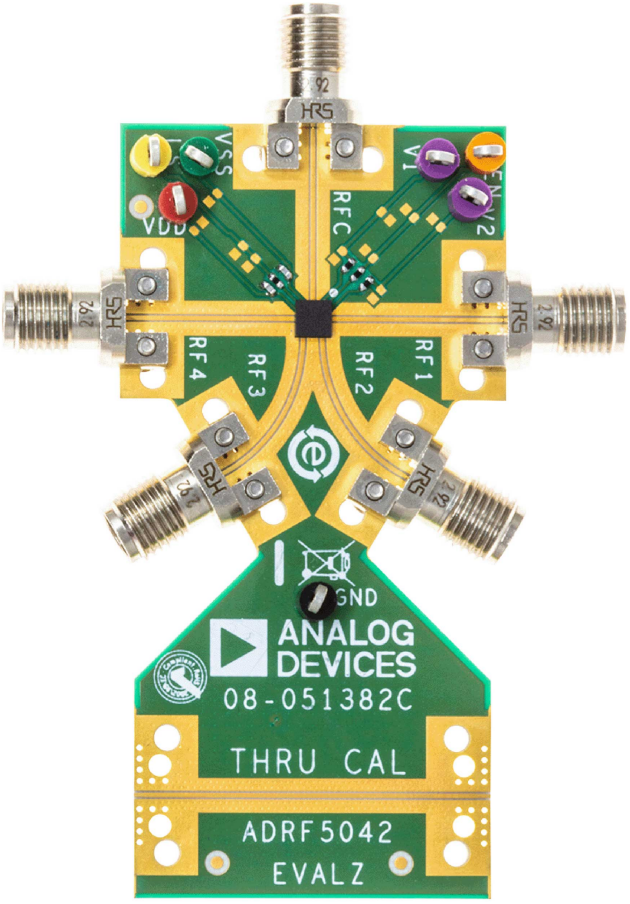

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Figure 1. Evaluation Board Photograph

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REVISION HISTORY

8/2023—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5048-EVALZ is a connectorized board, assembled with the ADRF5048 and its application circuitry. All components are placed on the primary side of ADRF5048-EVALZ. An assembly drawing for the ADRF5048-EVALZ is shown in Figure 9, and an evaluation board schematic is shown in Figure 8.

BOARD LAYOUT

The ADRF5048-EVALZ was designed using RF circuit design techniques on a 4-layer printed circuit board (PCB). The PCB stack-up is shown in Figure 2.

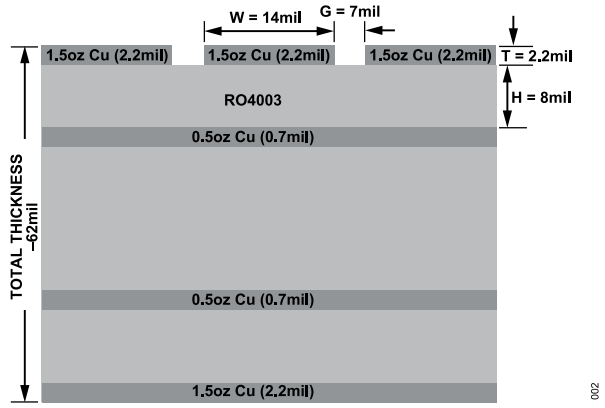

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 1.5 oz (2.2 mil) thick and the inner layers are 0.5 oz (0.7 mil) thick.

The top dielectric material is 8 mil Rogers 4003, which provides 50 Ω controlled impedance and optimizes the high frequency performance. All RF traces are routed on the top layer, and the second layer is used as the ground plane for RF transmission lines. The remaining two layers are also ground planes filled with FR4 material to manage the thermal rise during high power operations and are supported with dense and filled vias to the PCB bottom for thermal relief. The overall board thickness is approximately 62 mil for mechanical strength.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14 mil and ground spacing of 7 mil to have a characteristic impedance of 50 Ω. Ground via fences are arranged on both sides of a CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5048, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled, through vias to provide the lowest possible thermal resistance path from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

POWER SUPPLY AND CONTROL INPUTS

The ADRF5048-EVALZ has two power supply inputs, four control inputs, and a ground, as shown in Table 1. The DC test points are populated on VDD, VSS, V1, V2, EN, LS, and GND. A 3.3 V supply is connected to the DC test point on VDD and a −3.3 V supply is connected to the DC test point on VSS. Ground reference can be connected to GND. Connect the control inputs, V1, V2, EN, and LS, to 3.3 V or 0 V. The typical total current consumption for the ADRF5048 is 0.67 mA.

The VDD and VSS supply pins of the ADRF5048 are decoupled with 100 pF capacitors.

Table 1. Power Supply and Control Inputs

Test Points	Description
VDD	+3.3 V supply voltage
VSS	−3.3 V supply voltage
V1	Control input 1
V2	Control input 2
EN	Enable
LS	Logic select
GND	Ground

RF INPUTS AND OUTPUTS

The ADRF5048-EVALZ has seven edge-mounted, 2.92 mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

2.92 mm Connectors	Description
RFC	RF common port
RF1	RF Throw Port 1
RF2	RF Throw Port 2
RF3	RF Throw Port 3
RF4	RF Throw Port 4
THRU1	Thru line input and output
THRU2	Thru line input and output

The through calibration line, connecting the THRU1 and THRU2 RF connectors, calibrates out the board loss effects from the measurements of the ADRF5048-EVALZ to determine the device performance at the pins of the IC.

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5048-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the VSS test point.
4. Bias up the V1, V2, EN, and LS test points.
5. Apply an RF input signal.

The ADRF5048-EVALZ is shipped fully assembled and tested. Figure 3 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Perform the following steps to complete the test setup and to verify the operation of the ADRF5048-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage output terminal of the +3.3 V supply. Note that the current must be 0.15 mA.
3. Connect the VSS test point to the voltage output terminal of the −3.3 V supply. Note that the current must be 0.52 mA.
4. Connect the V1, V2, EN, and LS test points to the voltage output terminal of the 3.3 V supply. The ADRF5048 can be configured in different modes by connecting the control test points to 3.3 V or 0 V, as shown in Table 3.
5. Connect a calibrated network analyzer to the RFC, RF1, RF2, RF3, and RF4 2.92 mm connectors. If network analyzer port count is not enough, terminate unused RF ports with 50 Ω. Sweep the frequency from 10 MHz to 45 GHz and set the power to –5 dBm.
6. The ADRF5048-EVALZ is expected to have an insertion loss of 2.4 dB at 40 GHz. See the expected results in Figure 4.

Additional test equipment is needed to fully evaluate the ADRF5048-EVALZ functions and performance.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is also recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

The ADRF5048-EVALZ comes with a support plate attached to the bottom side. To ensure maximum heat dissipation and to reduce thermal rise on the ADRF5048-EVALZ during high power evaluations, this support plate must be attached to a heat sink using thermal grease.

Note that the measurements performed at the 2.92 mm connectors of the ADRF5048-EVALZ include the losses of the 2.92 mm connectors and the PCB. The thru line must be measured to calibrate out the effects on the ADRF5048-EVALZ. The thru line is the summation of an RF input line and an RF output line that are connected to the ADRF5048-EVALZ and equal in length.

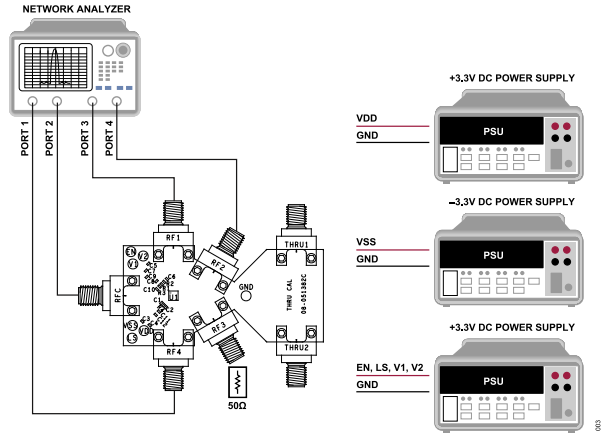

Figure 3. Test Setup Diagram

Table 3. Control Voltage Truth Table

Digital Control Inputs				RFx Paths			
EN	LS	V1	V2	RF1 to RFC	RF2 to RFC	RF3 to RFC	RF4 to RFC
Low	Low	Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	Low	High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	Low	Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	High	Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low or high	Low or high	Low or high	Isolation (off)	Isolation (off)	Isolation (off)	Isolation (off)

TEST PROCEDURE

EXPECTED RESULTS

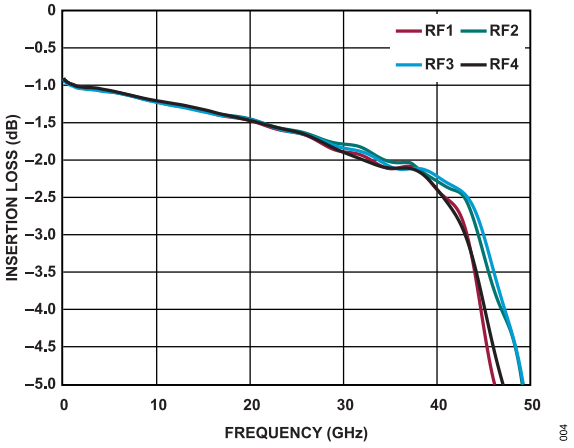

Figure 4. Insertion Loss for RFC to RFx Selected vs. Frequency

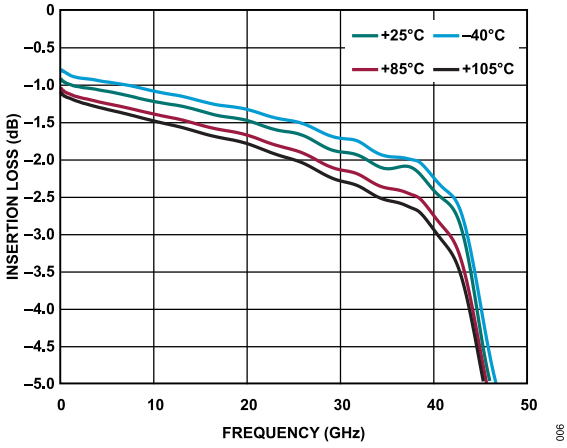

Figure 6. Insertion Loss for RFC to RF1 vs. Frequency over Temperature

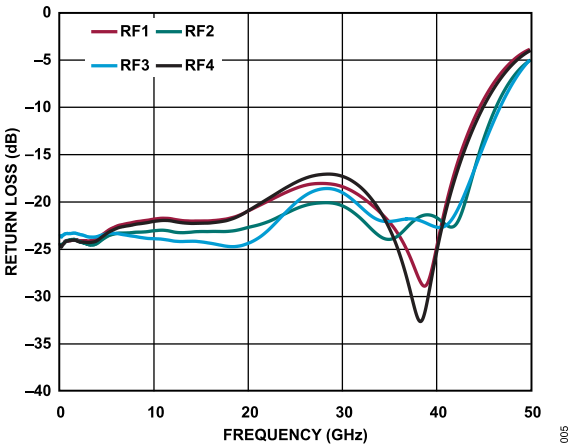

Figure 5. Return Loss for RFC when RFx Selected vs. Frequency

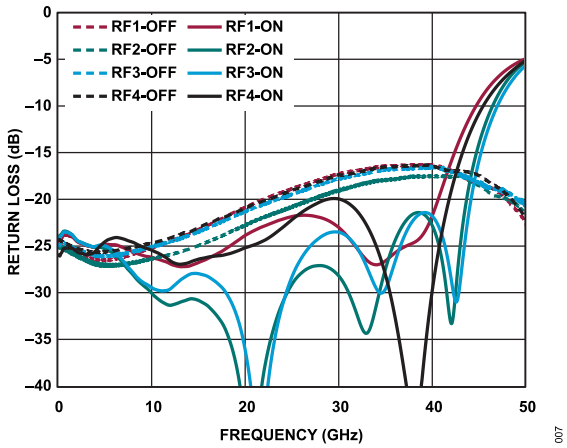

Figure 7. Return Loss for RFx Selected vs. Frequency

EVALUATION BOARD SCHEMATIC AND ARTWORK

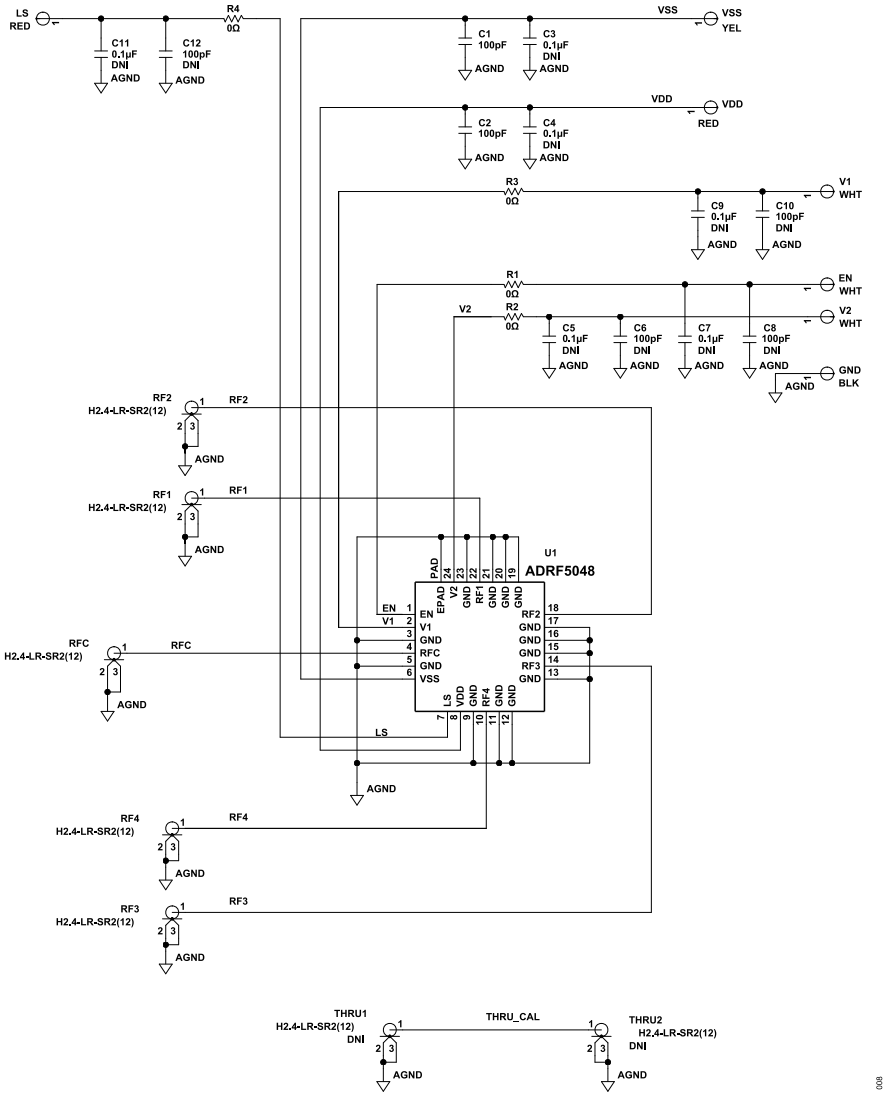

Figure 8. ADRF5048-EVALZ Evaluation Board Schematic

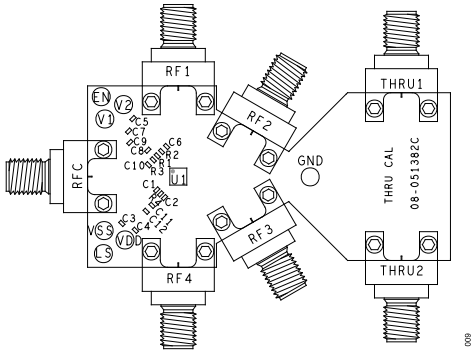

Figure 9. ADRF5048-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for the ADRF5048-EVALZ

Qty	Reference Designator	Description	Manufacturer	Part Number
2	C1, C2	Capacitors, 100 pF, 50 V, C0402 package	Murata	GCM1555C1H101JA16D
4	C6, C8, C10, C12	Capacitors, 100 pF, 50 V, C0402 package (do not insert (DNI))	Murata	GCM1555C1H101JA16D
6	C3, C4, C5, C7, C9, C11	Capacitor, 0.1 µF, 25 V, C0402 package (DNI)	Taiyo Yuden	TMK105B7104KVHF
4	R1, R2, R3, R4	Resistor, 0 Ω, C0402 package	Panasonic	ERJ-2GE0R00X
5	RFC, RF1, RF2, RF3, RF4,	Edge-mount 2.92 mm connectors	Hirose Electric	HK-LR-SR2(12)
2	THRU1, THRU2	Edge-mount 2.92 mm connectors (DNI)	Hirose Electric	HK-LR-SR2(12)
5	GND, LS, EN, V1, V2, and VDD	Surface-mount test points	Keystone Electronics	5005
1	U1	Silicon, SP4T switch, nonreflective, 100 MHz to 45 GHz	Analog Devices, Inc.	ADRF5048BBCZN
1	PCB	ADRF5049-EVALZ	Analog Devices	BR-051382

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.