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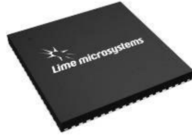
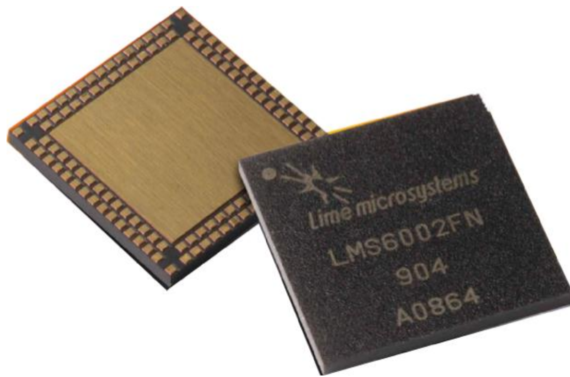


# LMS6002DFN

## Multi-band Multi-standard Transceiver – PCB layout

### Purpose

**This document provides PCB design guidelines for LMS6002DFN assembly, based on the industry standard dQFN120 type package. It outlines the package dimensions and the PCB design rules used on the LIME evaluation platforms and reference boards. It also provides for two footprint options for reliable and reproducible manufacturing for a given application. The instructions are meant as a guideline only and may need to be modified depending on specific PCB manufacturing processes.**




### Package description

The LMS6002DFN comes in a 120 pin dual row QFN (dQFN) 9mmx9mm package. The pads are 0.3mm square with 0.5mm pitch. The outer rows consist of 15 pins and inner rows of 14 pins, making a total of 29 pins per side. There are 4 corner pins, making a total of 120 pins. The LMS6002D IC does not use these 4 corner pins and they are unconnected. There is also a centre ground pad for electrical grounding and thermal cooling. The package height is 0.85mm.

### Package dimensions

Please refer to figure 1 for package dimension and measurements.

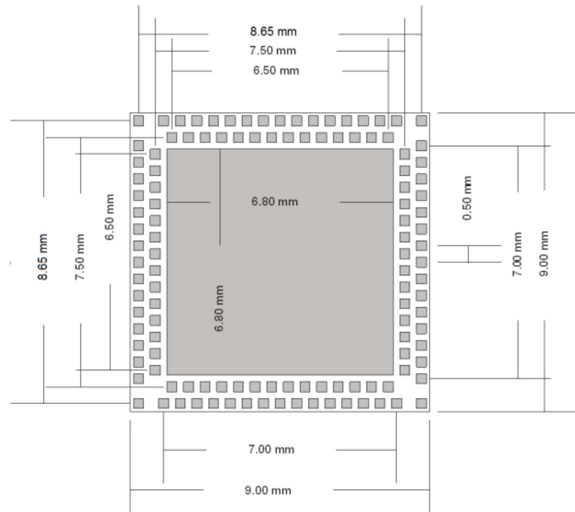



Figure 1: LMS6002DFN land pattern

### PCB pattern (option 1, Via in Pad)

As shown in figure 2, the outer rows use pads of 0.3mm x 0.45mm so that the pads extend by 0.15mm from the edge of the package. The inner rows use pad size of 0.3mm x 0.3mm, as shown in figure 3. No pads are provided for the 4 corner pins. The gaps between the pads are 0.2mm.

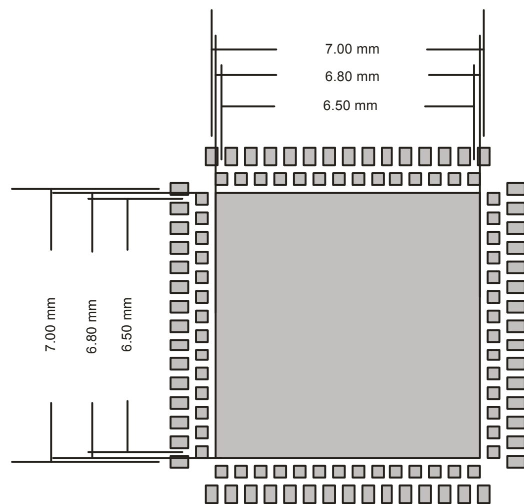



Figure 2: LMS6002DFN land pattern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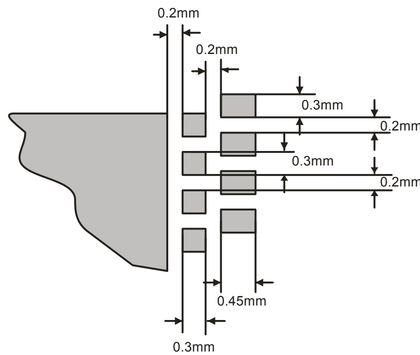


Figure 3: LMS6002DFN land pattern – detail

***Note*** *When designing the pattern, care should be taken for the fact that the outer row of the pins are not square. Therefore, the centre of these rows are not the same as the centre of the square pins on the package drawing.*

## Solder resist

The solder resist clearance is 0.05mm, see Figure 4. This leaves 0.1mm of solder resist between pads of the footprint.

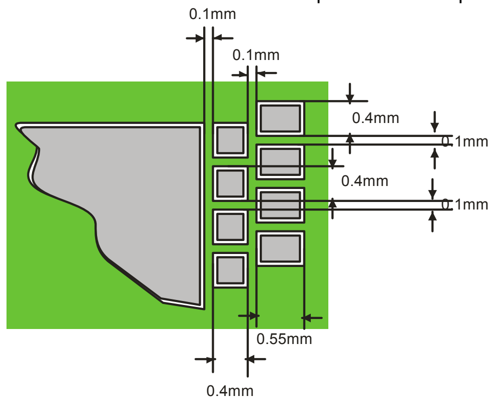


Figure 4: Solder resist clearance – detail

## Solder paste

The solder paste mask is the same size as the IC pads with the exception of the large centre pad where a hatched pattern is used to reduce the amount of solder paste on the centre pin, as shown in figure 5.

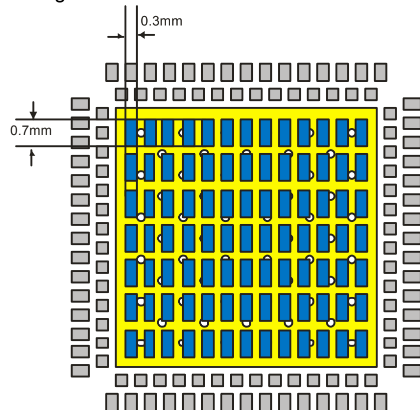


Figure 5: Centre pad solder paste

Solder paste grid used on the centre pad is a grid of 13x7 0.3mmx0.7mm rectangles (approx 40% coverage).

## Thermal ground pad

The centre pad of the dQFN120 package is used for both electrical ground as well as providing the required thermal path. There should be both a low inductance path to the RF ground plane of the PCB as well as a low thermal resistance to copper planes which are used to dissipate the heat. It has been found that with proper design of PCB, no additional heat sinking is required to cool the LMS6002D IC.
A pattern of 51 x 0.2mm through Vias (shown in Figure 6) are used on the centre pad to provide for the above.

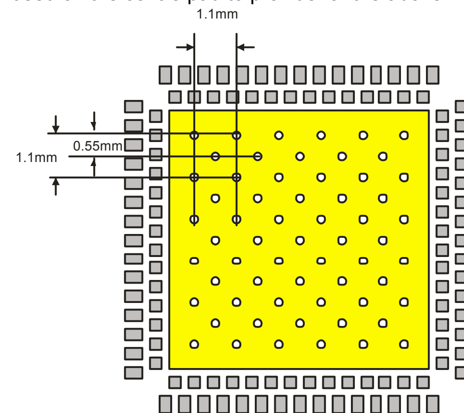


Figure 6: Centre pad thermal / ground Vias

On the other/back side of the PCB, it is important to note that the Vias are connected to copper which in turn allows for the heat to radiate from the PCB surface. The copper area on the back should be larger than the thermal pad on the device; if possible the back of the pcb should be copper filled to dissipate as much heat as possible.

## Inner pins and routing

The inner rows of pins of the LMS6002D carry no RF critical signals but do need to be routed away from the device. Due to the location of the centre ground pad this means that Via in pad maybe required.

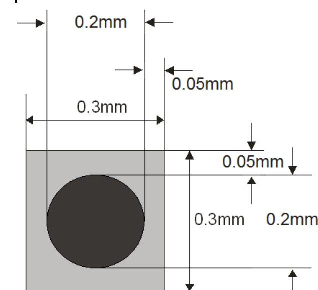


Figure 7: Via in pad

The LIME design uses a 0.2mm drilled Via with a 0.2mm annulus, as shown in Figure 7. It uses a 6 layer board, layer 1(top) for RF tracks and routing, layer 2 for ground and layers 3, 4, 5 and 6 (bottom) are for routing. The Vias in the pads of the LMS6002D footprint are routed to the bottom layer. The Board has a 0.172mm (6.8mil) layer 1 to 2 height and a 0.076mm (3mil) layer 2 to 3 prepreg.



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## PCB pattern (option 2, Via off Pad)

As shown in figure 8, the outer rows use pads of 0.3mm x 0.45mm so that the pads extend by 0.15mm from the edge of the package. The inner rows use pad size of 0.3mm x 0.3mm, as shown in Figure 9. No pads are provided for the 4 corner pins. The gaps between the pads are 0.2mm.

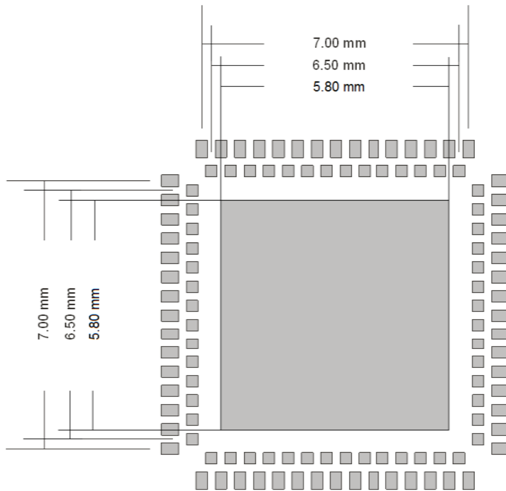


Figure 8: LMS6002DFN land pattern

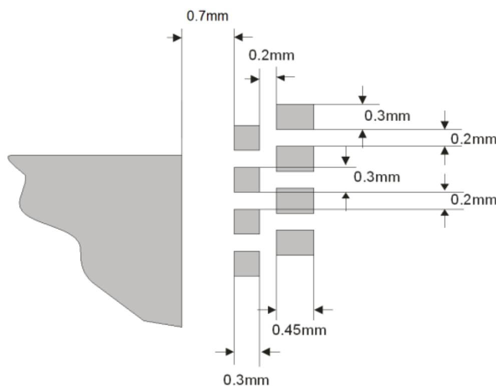


Figure 9: LMS6002DFN land pattern – detail

***Note*** *When designing the pattern, care should be taken for the fact that the outer row of the pins are not square. Therefore, the centre of these rows are not the same as the centre of the square pins on the package drawing.*

## Solder resist

The solder resist clearance is 0.05mm, see Figure 10. This leaves 0.1mm of solder resist between pads of the footprint.

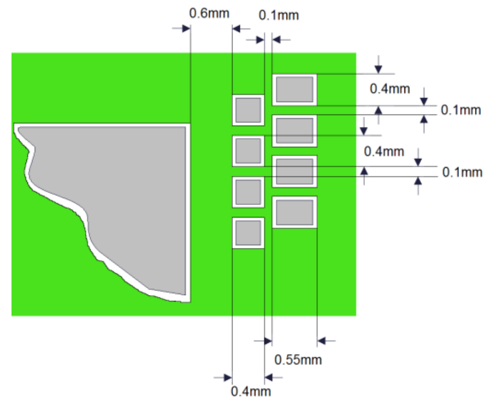


Figure 10: Solder resist clearance – detail

## Solder paste

The solder paste mask is the same size as the IC pads with the exception of the large centre pad where a hatched pattern is used to reduce the amount of solder paste on the centre pin, as shown in figure 11.

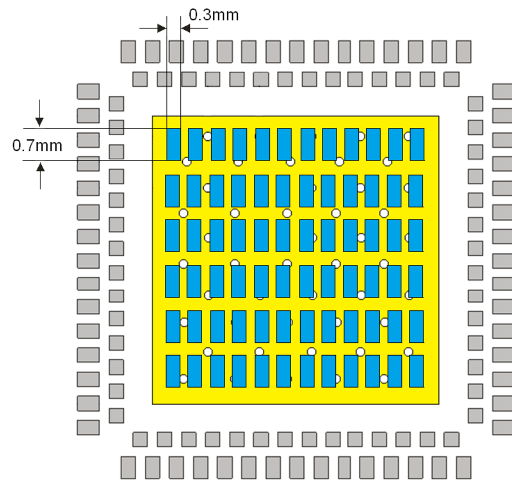


Figure 11: Centre pad solder paste

Solder paste grid used on the centre pad is a grid of 12x6 0.3mmx0.7mm rectangles (approx 45% coverage).

## Thermal ground pad

The centre pad of the dQFN120 package is used for both electrical ground as well as providing the required thermal path. There should be both a low inductance path to the RF ground plane of the PCB as well as a low thermal resistance to copper planes which are used to dissipate the heat. It has been found that with proper design of PCB, no additional heat sinking is required to cool the LMS6002D IC.
A pattern of 50 x 0.2mm through Vias (shown in Figure 612) are used on the centre pad to provide for the above.



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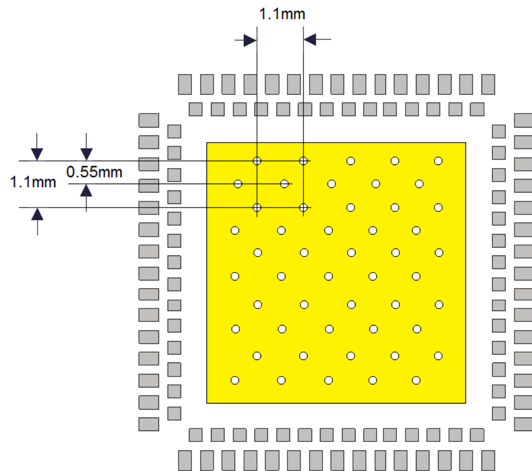


Figure 12: Centre pad thermal / ground Vias

On the other/back side of the PCB, it is important to note that the Vias are connected to copper which in turn allows for the heat to radiate from the PCB surface. The copper area on the back should be larger than the thermal pad on the device; if possible the back of the pcb should be copper filled to dissipate as much heat as possible.

## Inner trace and routing

As in the case above, the inner rows of pins need to be routed away from the device. This could be done by using a smaller center pad to avoid the Via in pad, as shown in Figure 13. Due to reduced centre ground pad surface, Via off pad can be used to route out the signals from inner pads of LMS6002D IC.

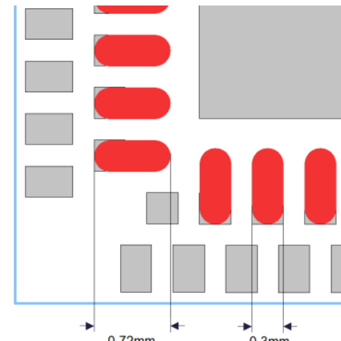


Figure 13: inner trace

Please note that the Inner traces and Vias are covered with solder resist.

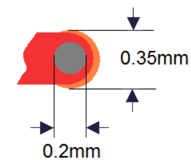


Figure 14: Via off pad

The LIME reference design uses a 0.2mm drilled Via with a 0.15mm annulus, as shown in Figure 14. The other general rules and dimensions remain as in the Via in Pad version, given the pervious section.



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