MASW-011043

GaAs SP3T / SPDT
DC - 6.0 GHz (Optimized for 2.4 / 5.8 GHz operation)

Rev. V2

Features

- Dual Band, Integrated SP3T (2.4 GHz) and SPDT (5.8 GHz) Switch
- Ideal for 802.11n, ac Applications
- Lead-Free 2 mm 12-Lead STQFN package
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant and 260°C Reflow Compatible

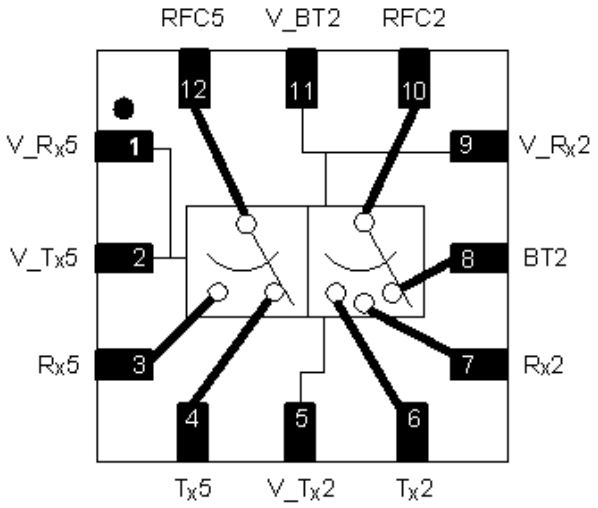
Description

The MASW-011043 is an integrated MMIC design which includes a SPDT switch and a SP3T switch. This part would typically be used on the front end of 802.11 n, ac applications.

This switch delivers high isolation and low insertion loss in a lead free 2 mm 12-lead STQFN package.

The MASW-011043 is ideal for broad band applications. The low frequency roll-off is controlled by the series blocking capacitors.

Functional Schematic



Pin Configuration[3,4]

Pin No.	Function	Description
1	V_RX5	Vcontrol SP2T RX
2	V_TX5	Vcontrol SP2T TX
3	RX5	SPDT RX Port
4	TX5	SPDT TX Port
5	V_TX2	Vcontrol SP3T TX
6	TX2	SP3T TX Port
7	RX2	SP3T RX Port
8	BT2	SP3T BT Port
9	V_RX2	Vcontrol SP3T RX
10	RFC2	SP3T RFC Port
11	V_BT2	Vcontrol SP3T BT
12	RFC5	SP2T RFC
13	GND (paddle)	Ground

3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.
4. To achieve optimum performance, connect 620 Ω, size 0201 resistors to all control pins. See recommended PCB layout on page 6.

Ordering Information[1,2]

Part Number	Package
MASW-011043-TR3000	3000 piece reel
MASW-011043-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

GaAs SP3T / SPDT
DC - 6.0 GHz (Optimized for 2.4 / 5.8 GHz operation)

Rev. V2

SP3T Electrical Specifications:
Freq. = 2.4 GHz, T_A = 25°C, $V_{Control}$ = 0 V / 3 V, P_{IN} = 0 dBm, Z_0 = 50 Ω[5]

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	RFC2 to T_X2/R_X2/BT2	dB	—	0.6	0.9
Isolation	RFC2 to T_X2 RFC2 to R_X2 RFC2 to BT2 R_X2-T_X2 (T_X2 IL) T_X5 to R_X2 (R_X2 IL)	dB	22 25 25 — —	27 30 30 27 33	—
Return Loss	—	dB	—	25	—
Input P0.1dB	3 V 5 V	dBm	—	26 32	—
Input P1dB	3 V 5 V	dBm	—	29 35	—
Output IP3	1 MHz Spacing, 15 dBm, 3 V 1 MHz Spacing, 15 dBm, 5 V	dBm	—	54 57	—
2nd Harmonic	T_X2, 20 dBm, 3 V T_X2, 20 dBm, 5 V	dBc	—	-68 -71	—
T_{ON}, T_{OFF}	50% control to 90% RF 50% control to 10% RF	ns	—	200	—
Current	$V_{Control}$ = 3 V	µA	—	1.5	5.0

5. External DC blocking capacitors are required on all RF ports. Specified performance is with 22 pF capacitors as shown in the recommended PCB layout on page 6.

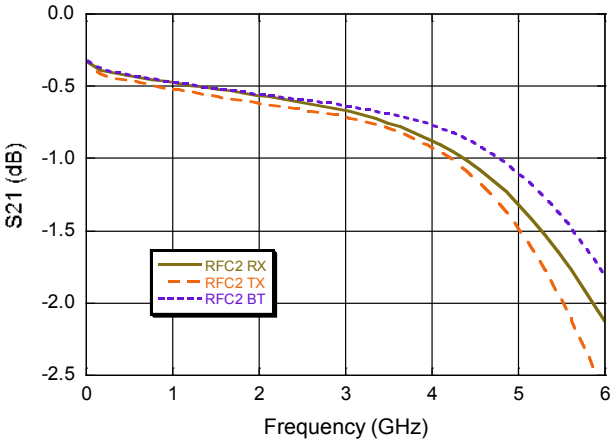
SPDT Electrical Specifications:
Freq. = 5.8 GHz, T_A = 25°C, $V_{Control}$ = 0 V / 3 V, P_{IN} = 0 dBm, Z_0 = 50 Ω[6]

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	RFC5 to T_X5/R_X5	dB	—	0.95	1.25
Isolation	RFC5 to T_X5 RFC5 to R_X5 R_X5 to T_X5 R_X5 to T_X2	dB	16 16 — —	21 21 21 30	—
Return Loss	—	dB	—	17	—
Input P0.1dB	3 V 5 V	dBm	—	26 29	—
Input P1dB	3 V 5 V	dBm	—	32 35	—
Output IP3	1 MHz Spacing, 15 dBm, 3 V 1 MHz Spacing, 15 dBm, 5 V	dBm	—	52 56	—
2nd Harmonic	T_X5, 20 dBm, 3 V	dBc	—	-70	—
2nd Harmonic Interferer	Rx5: Stimulate Tx2, 20 dBm, 3 V	dBc	—	-50	—
T_{ON}, T_{OFF}	50% control to 90% RF 50% control to 10% RF	ns	—	14	—
Current	$V_{Control}$ = 3 V	µA	—	1.5	5.0

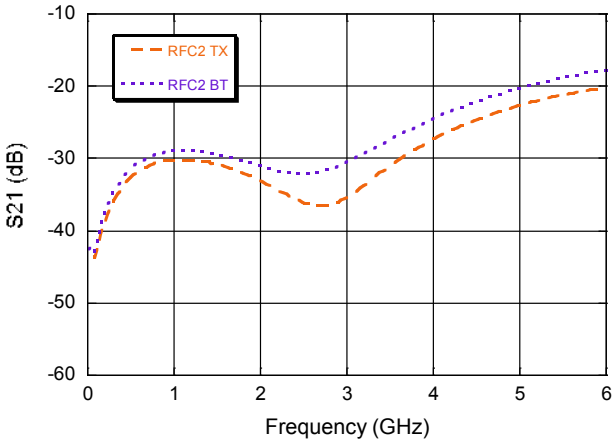
6. External DC blocking capacitors are required on all RF ports. Specified performance is with 8 pF capacitors as shown in the recommended PCB layout on page 6.

SP3T Typical Performance Curves:

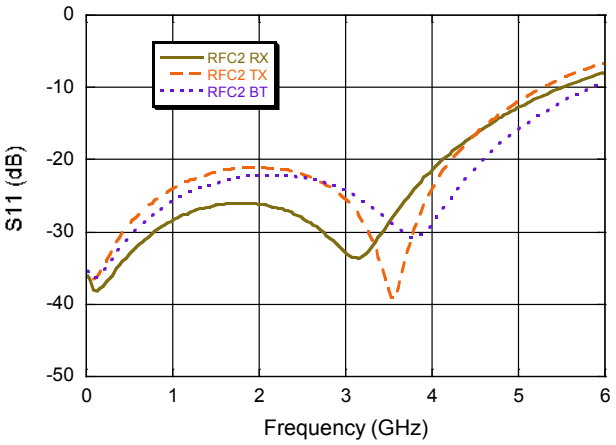
Insertion Loss



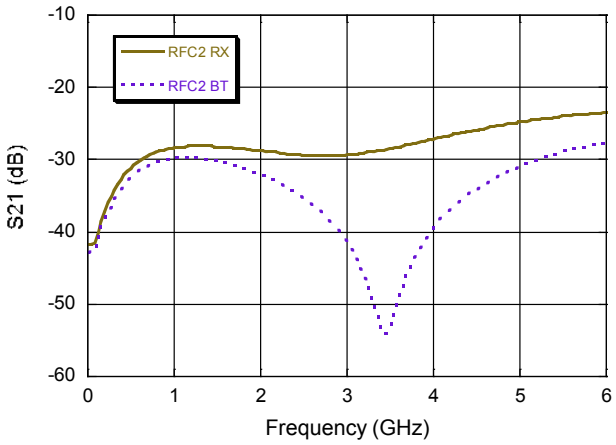
Isolation RFC2 - RX2



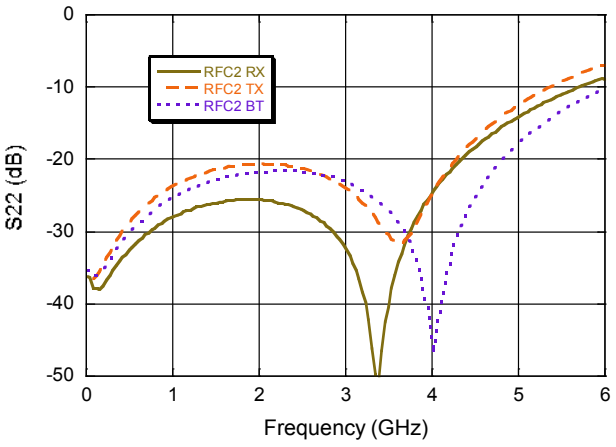
Input Return Loss (Insertion Loss Cases)



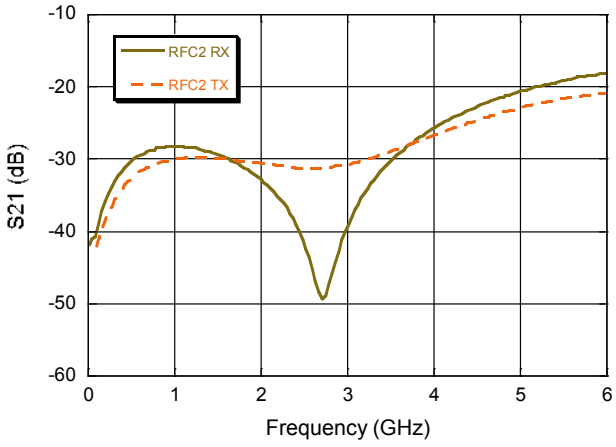
Isolation RFC2 - TX2



Output Return Loss (Insertion Loss Cases)

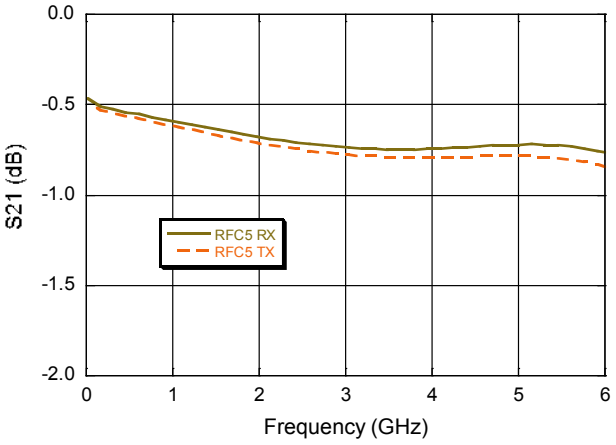


Isolation RFC2 - BT2

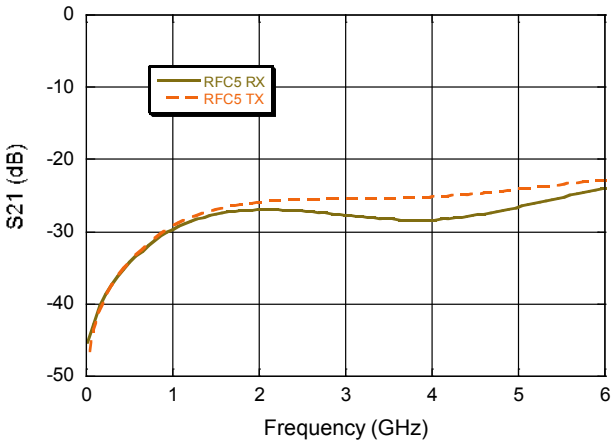


SPDT Typical Performance Curves:

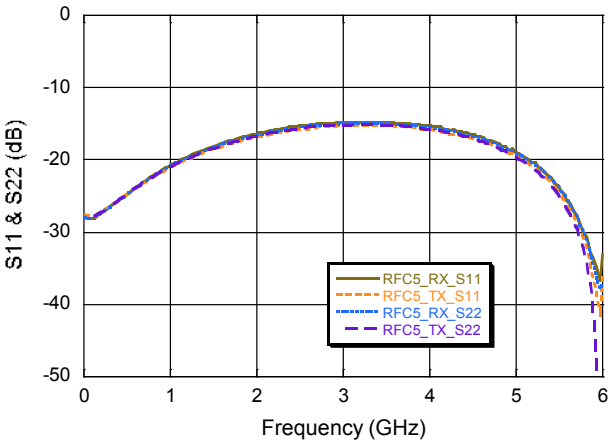
Insertion Loss



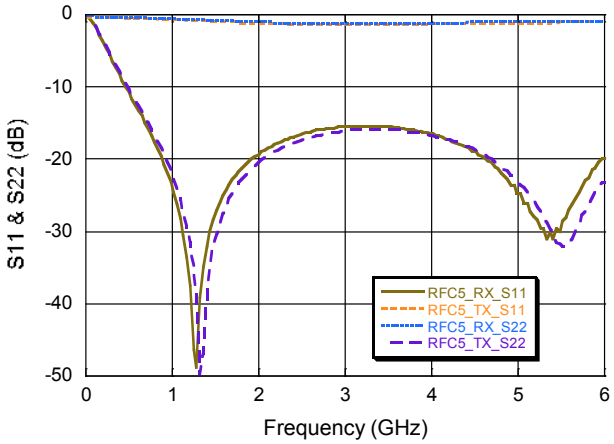
Isolation



Return Loss (Insertion Loss Cases)



Return Loss (Isolation Cases)



Absolute Maximum Ratings[7,8]

Parameter	Absolute Maximum
Input Power (0.5 - 6.0 GHz, 3 V Control)	+32.0 dBm SPDT +33.5 dBm SP3T
Control Voltage	+5 volts
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

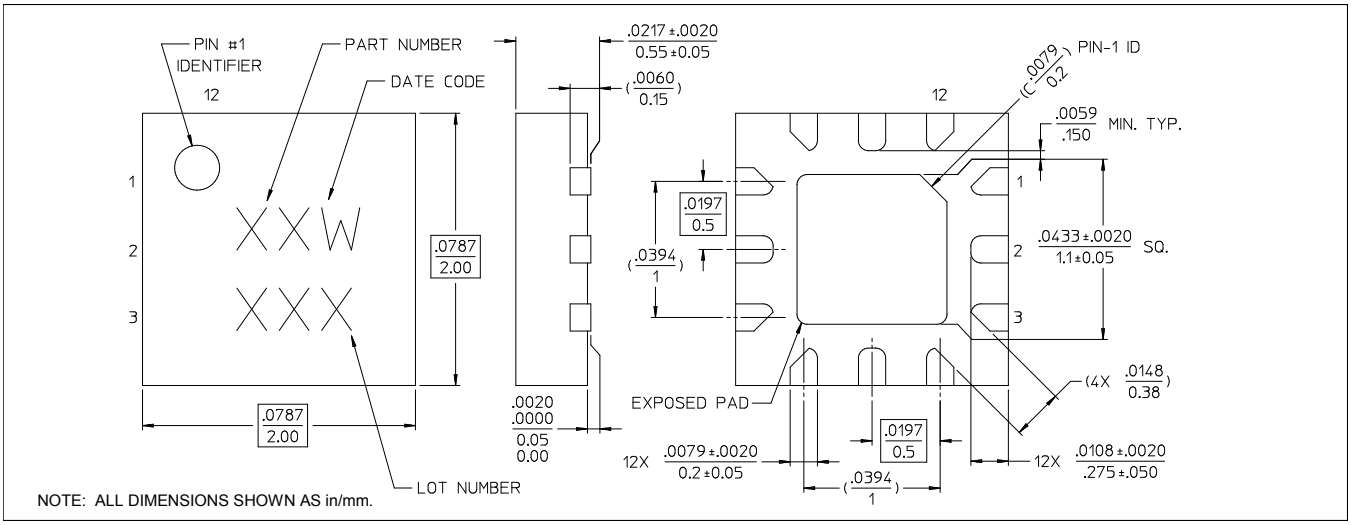
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Truth Table[9,10,11]

State	V_BT2	V_RX2	V_TX2	V_RX5	V_TX5	Insertion Path	Band
1	1	0	0	0	0	RFC2 - BT2	2.4 GHz
2	0	1	0	0	0	RFC2 - RX2	2.4 GHz
3	0	0	1	0	0	RFC2 - TX2	2.4 GHz
4	0	0	0	1	0	RFC5 - RX5	5.8 GHz
5	0	0	0	0	1	RFC5 - TX5	5.8 GHz

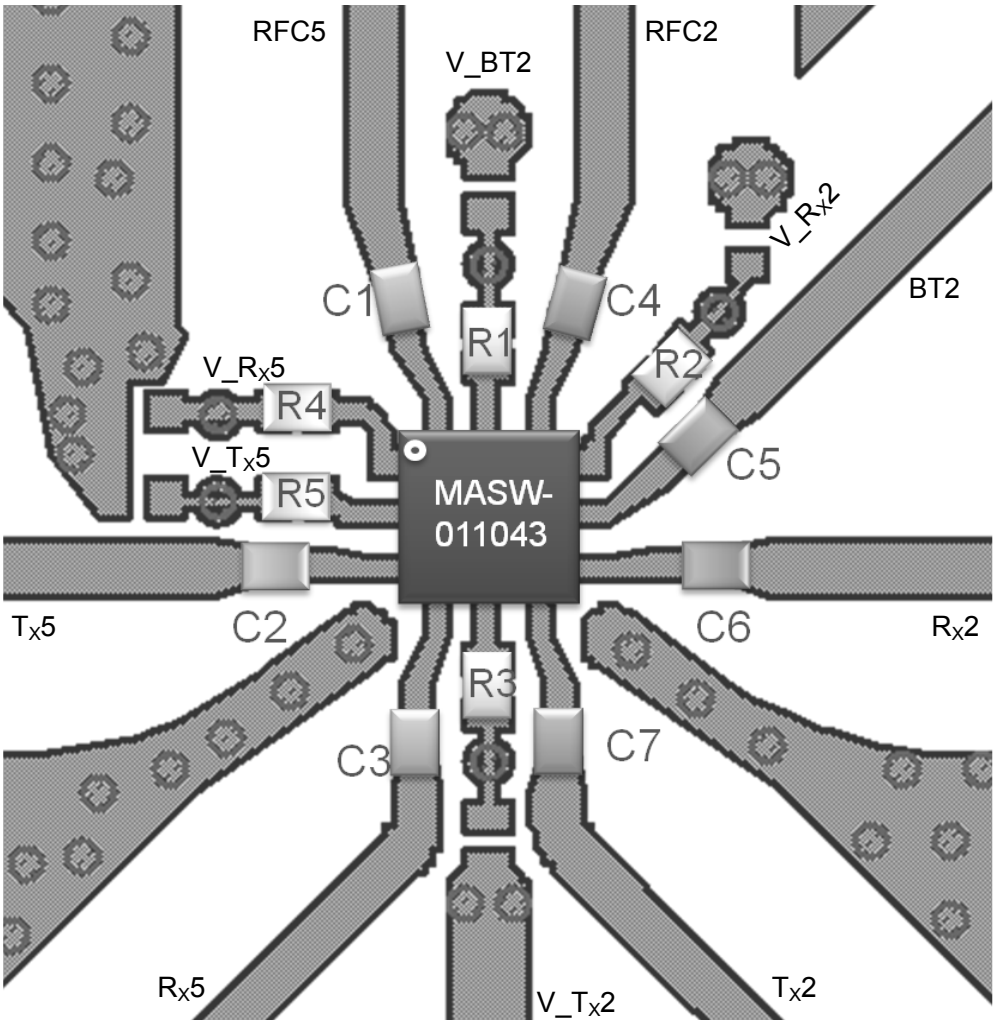
9. Vcontrol: “0”= 0 V +/- 0.2 V, “1” = +2.6 V to +5 V.
10. Differential voltage, Vcontrol “1” - Vcontrol “0” should be 2.6 V minimum and must not exceed 5 V.
11. SPDT and SP3T can be used simultaneously.

Lead-Free 2mm STQFN-12LD 0.5 mm Pitch†



† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.

Recommended PCB Layout[12,13]



12.The exposed pad centered on the package bottom must be connected to ground to ensure a good thermal path.
13.To achieve optimum performance, connect 620 Ω, size 0201 resistors to all control pins.

Parts List

Component	Value	Package
C1 - C3	8 pF	0201
C4 - C7	22 pF	0201
R1 - R5	620 Ω	0201