DC–24 GHz 0.5W Self-Biased Single Positive Supply Distributed Power Amplifier

Product Overview

MMA052PP45 is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic highelectron-mobility transistor (pHEMT) distributed self-biased amplifier in plastic package form that operates between DC and 24 GHz. It is ideal for test instrumentation, wideband military and space applications. The amplifier provides a 14 dB of gain with a rising slope, 3.5 dB noise figure, output IP3 of 35 dBm, and 28 dBm of output power at 3dB gain compression at 10 GHz. The MMA052PP45 amplifier features RF I/Os that are internally matched to 50 Ω, which is ideal for any surface mount technology (SMT) assembly equipment.

Key Features

- **Broadband performance: DC to 24 GHz**
- **Psat: 28 dBm**
- **Gain: 14 dB with positive Gain Slope**
- **High IP3: 35 dBm**
- **Single Positive Supply: 9V at 310 mA**
- **50Ω matched I/O**
- **4.5 mm × 4.5 mm, 32L plastic QFN Passivated space-qualified process listed on EPPL007-38**

Functional Block Diagram

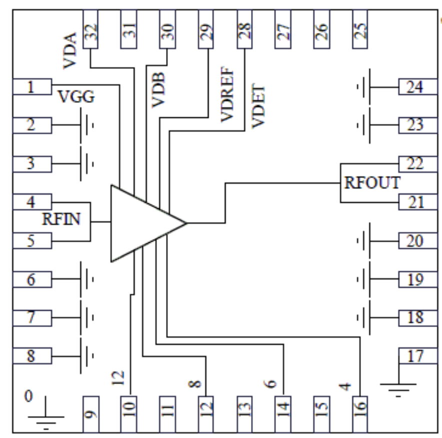


Figure 1 - Gain, IM3, Psat Performances

Applications

- Test and measurement instrumentation
- Military, EW, ECM, RADAR and space
- Telecom infrastructure
- Wideband microwave radios

Performance Overview

Parameter	Typ.	Units
Operational frequency range	DC-24	GHz
Gain	14	dB
Psat	+28	dBm
IM3 @ 20dBm	-33	dBc
Current @ +9V Supply	310	mA

Export Classification: EAR-99

Contents

1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1 - Typical Electrical Performance at 25 C, Vdd=9V, Idd=310 mA (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		24	GHz
Gain	DC – 6 GHz	12	14		dB
	6 GHz – 12 GHz	13	14.5		
	12 GHz – 24 GHz	14	15.5		
Gain flatness	4 GHz – 12 GHz		± 1		dB
	12 GHz – 24 GHz		± 0.7		
Noise figure	2 GHz – 6 GHz		5		dB
	6 GHz – 12 GHz		3.5		
	12 GHz – 24 GHz		4.5		
Input return loss	DC – 6 GHz		15		dB
	6 GHz – 12 GHz		15		
	12 GHz – 24 GHz		12		
Output return loss	DC – 6 GHz		14		dB
	6 GHz – 12 GHz		14		
	12 GHz – 24 GHz		12		
P1dB	DC – 6 GHz	25	27		dBm
	6 GHz – 12 GHz	25	27		
	12 GHz – 20 GHz	24.5	26		
	20 GHz – 24 GHz	24	25.5		
Psat (Measured at 3dB Gain Compression)	DC – 6 GHz		29		dBm
	6 GHz – 12 GHz		28		
	12 GHz – 20 GHz		27.5		
	20 GHz – 24 GHz		27		
OIP3	DC–6 GHz		36		dBm
	6 GHz–12 GHz		35		
	12 GHz – 24 GHz		32		
IM3 @ 20dBm	DC–6 GHz		-35		dBc
	6 GHz–12 GHz		-33		
	12 GHz – 24 GHz		-26		
Phase Noise					dBm/Hz
OIP2(low) (2-nd Order Intercept point F2-F1)			57		dBm
VDD (drain voltage supply)			9	11	V
IDD (drain current)			310	400	mA

1.2 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA052PP45 device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 2 - Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	12 V
Gate bias voltage (V_G)	–2 V to 0.5 V
RF input power (Pin)	24 dBm (or 6 dB Compression)
Channel temperature	165 °C
V_{DD} current (I_{DD})	400 mA
DC power dissipation (T = 85 °C)	4.8 W
Thermal resistance	15°C/W
Storage temperature	–65 °C to 150 °C
Operating temperature	–55 °C to 85 °C

ESD Sensitive Device

1.3 Typical Performance Curves

1.1.1 Typical Performances vs. Temperature

The following graphs show the typical performance curves of the MMA052PP45 device at 25 °C vs. Bias conditions; measurements performed using application circuit shown on Figure 71 - below. Currents were set by States according to Table 3-3

Figure 1 - Gain vs. Temperature @ 5V/220mA

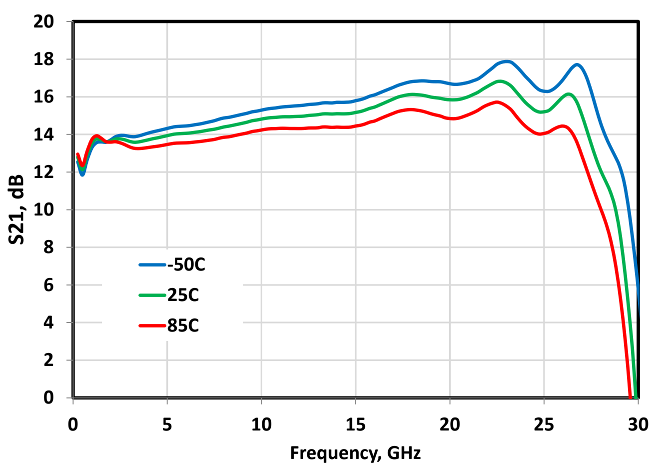


Figure 2 - Gain vs. Temperature @ 8V/270mA

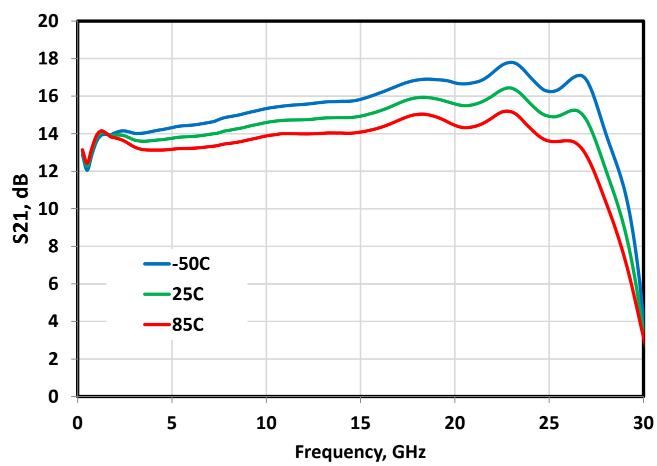


Figure 3 - Gain vs. Temperature @ 9V/310mA

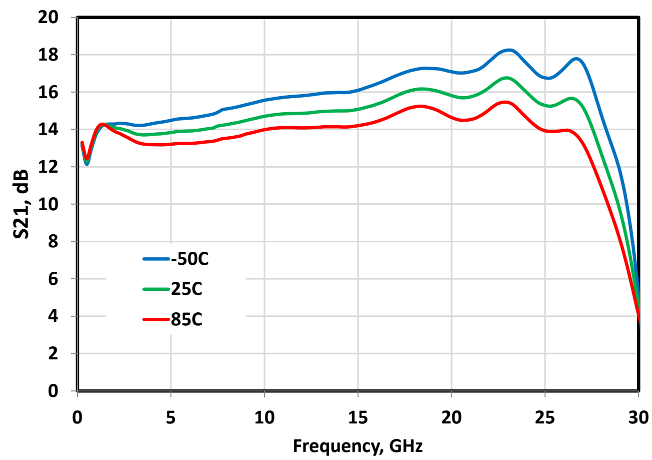


Figure 4 - Gain vs. Temperature @ 10V/360mA

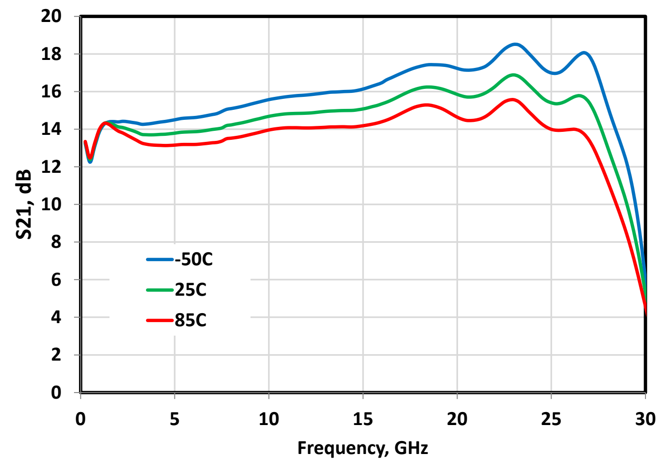


Figure 5 - S11 vs. Temperature @ 5V/220mA

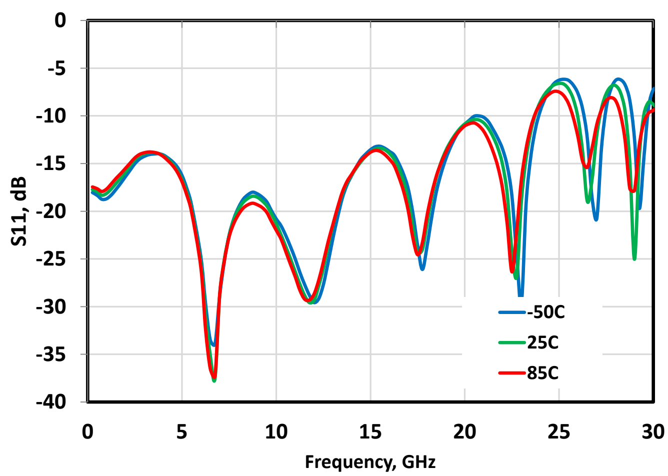


Figure 6 - S11 vs. Temperature @ 8V/270mA

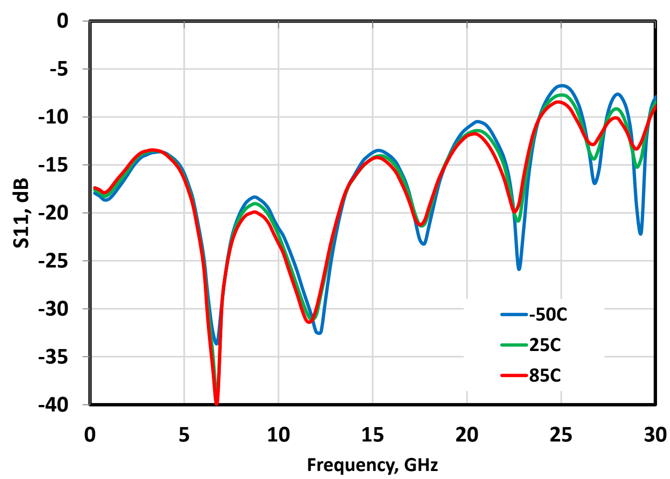


Figure 7 - S11 vs. Temperature @ 9V/310mA

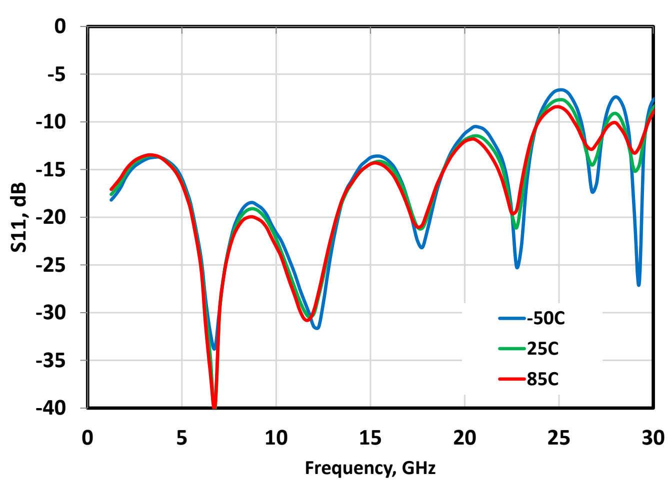


Figure 8 - S11 vs. Temperature @ 10V/360mA

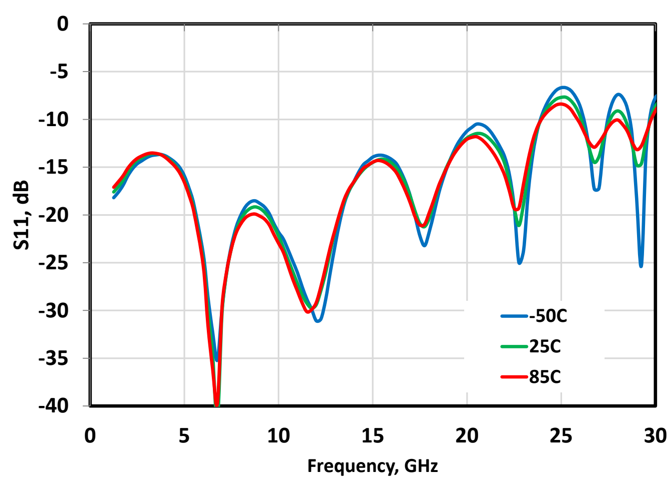


Figure 9 - S22 vs. Temperature @ 5V/220mA

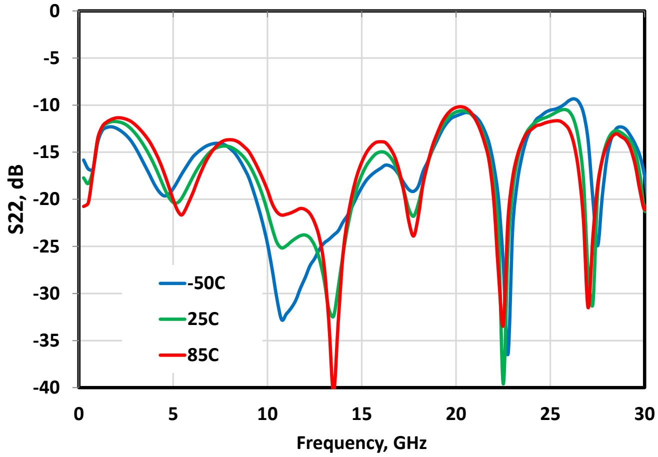


Figure 10 - S22 vs. Temperature @ 8V/270mA

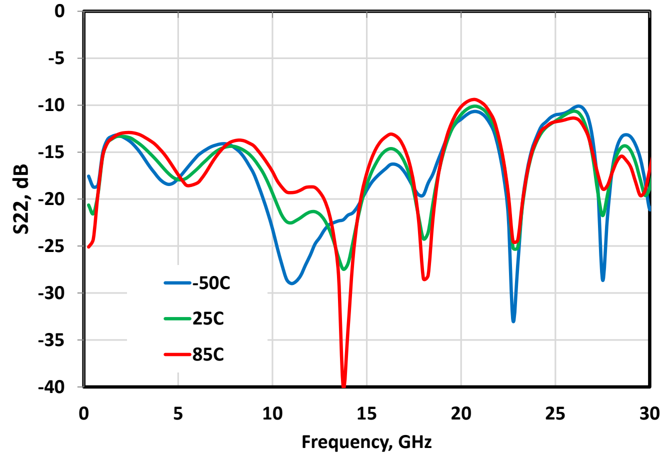


Figure 11 - S22 vs. Temperature @ 9V/310mA

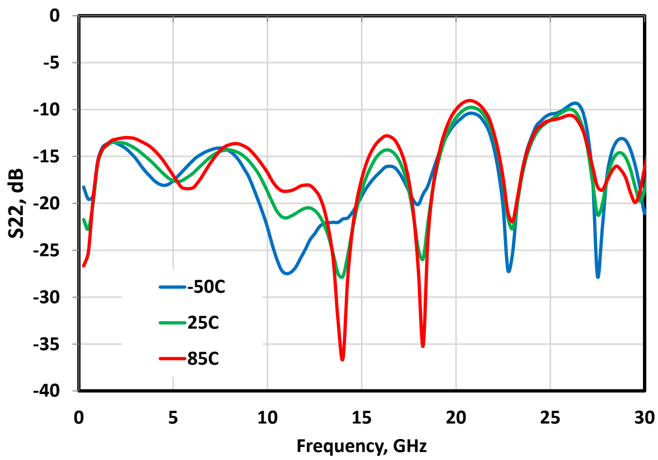


Figure 12 - S22 vs. Temperature @ 10V/360mA

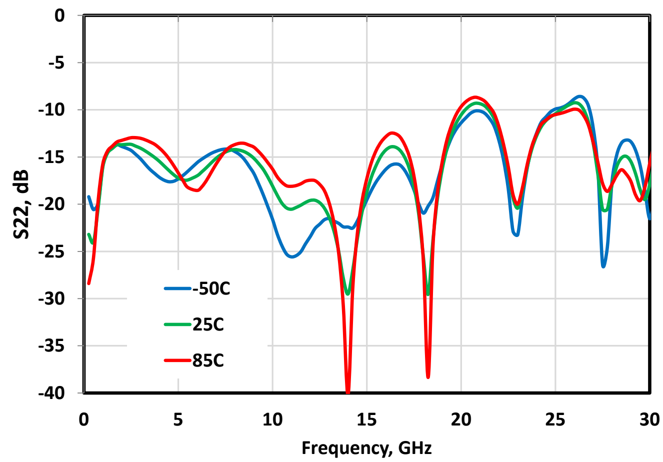


Figure 13 - S12 vs. Temperature @ 5V/220mA

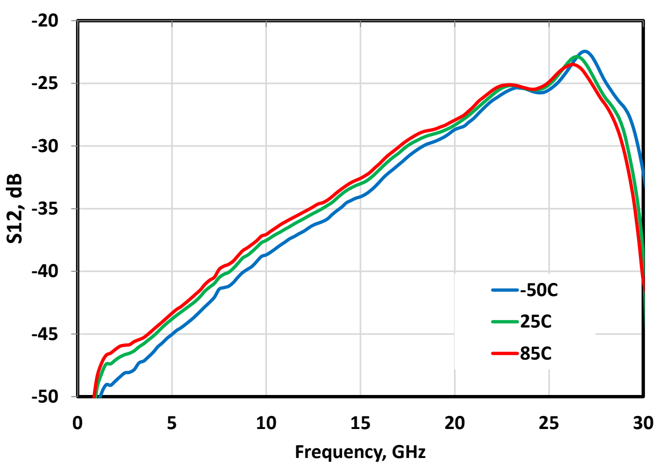


Figure 14 - S12 vs. Temperature @ 8V/270mA

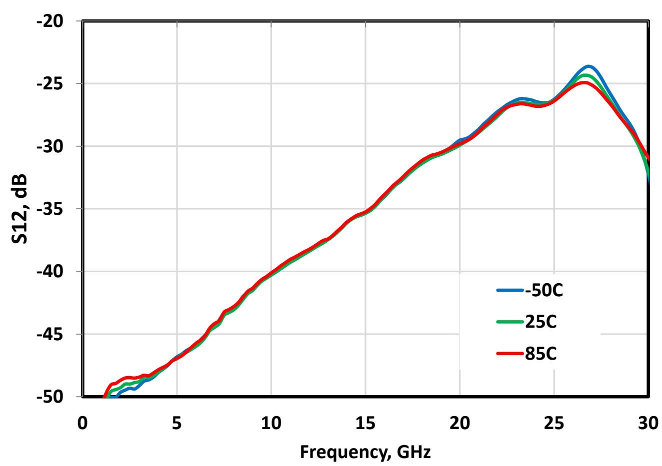


Figure 15 - S12 vs. Temperature @ 9V/310mA

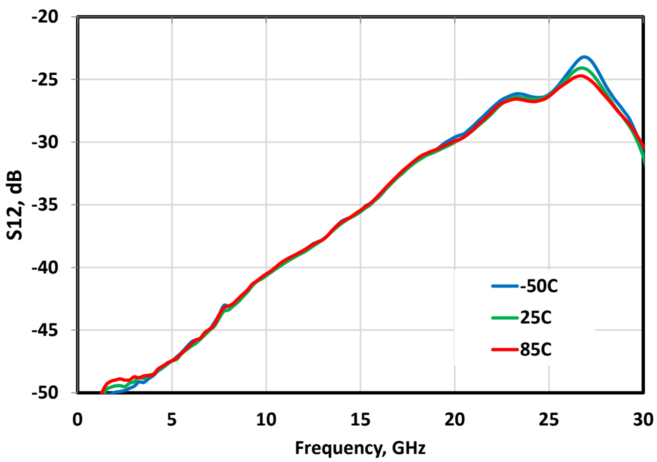


Figure 16 - S12 vs. Temperature @ 10V/360mA

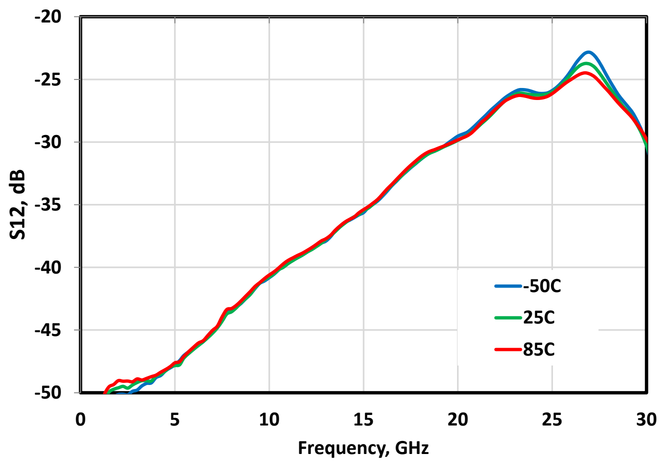


Figure 17 - NF vs. Temperature @ 5V/220mA

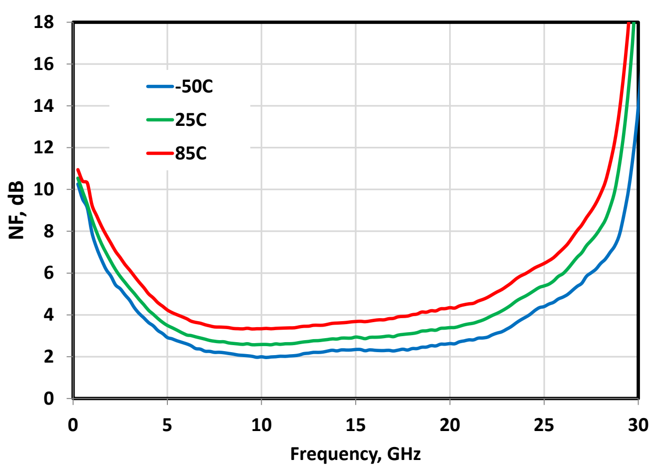


Figure 18 - NF vs. Temperature @ 8V/270mA

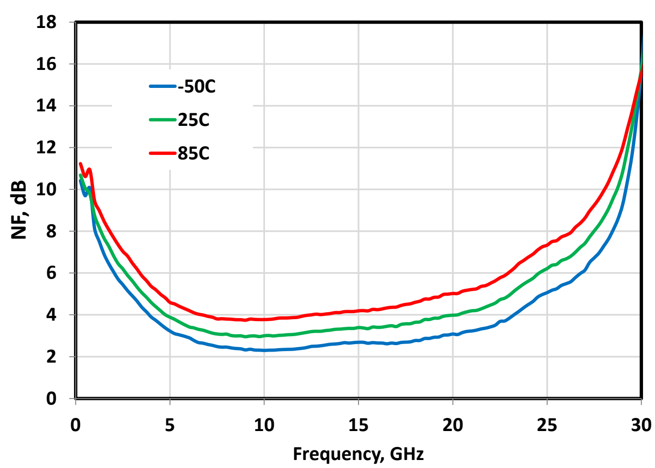


Figure 19 - NF vs. Temperature @ 9V/310mA

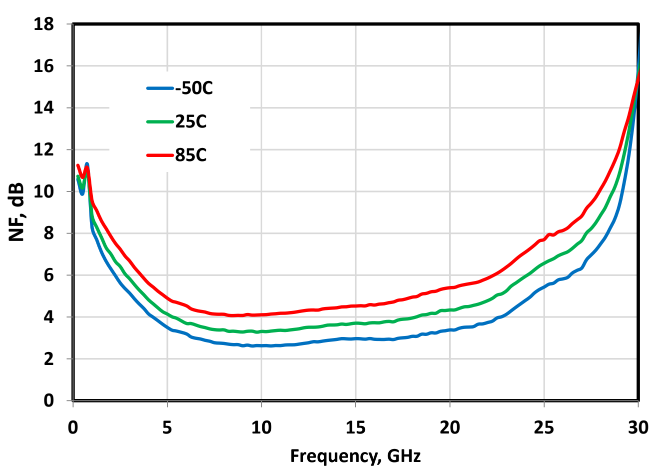


Figure 20 - NF vs. Temperature @ 10V/360mA

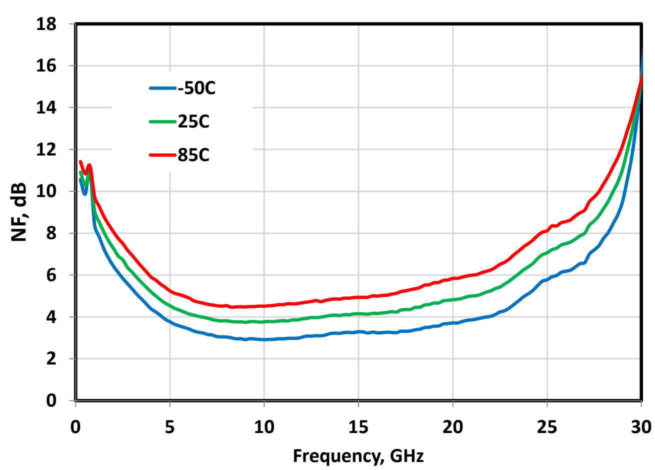


Figure 21 - P1dB vs. Temperature @ 5V/220mA

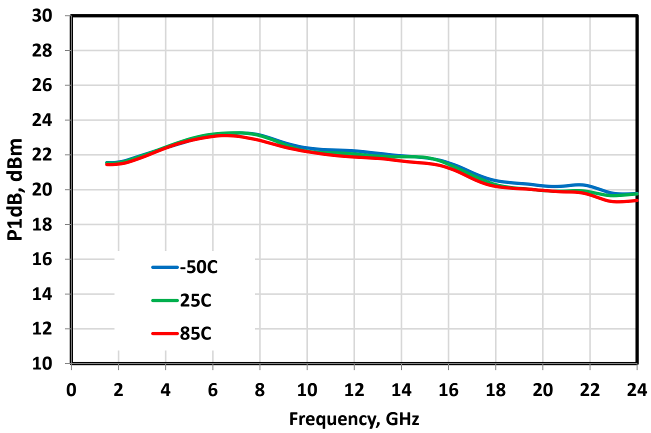


Figure 22 - P1dB vs. Temperature @ 8V/270mA

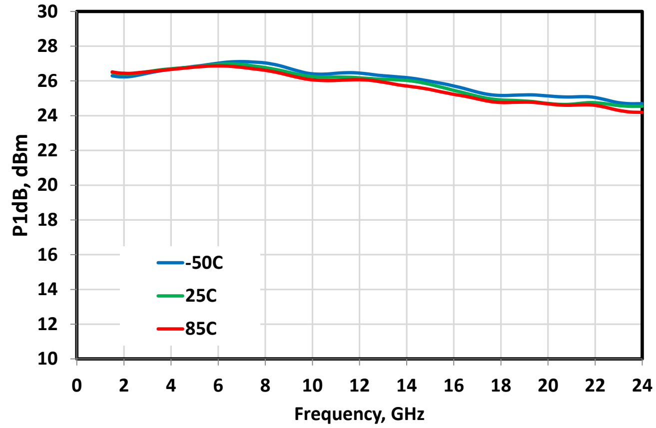


Figure 23 - P1dB vs. Temperature @ 9V/310mA

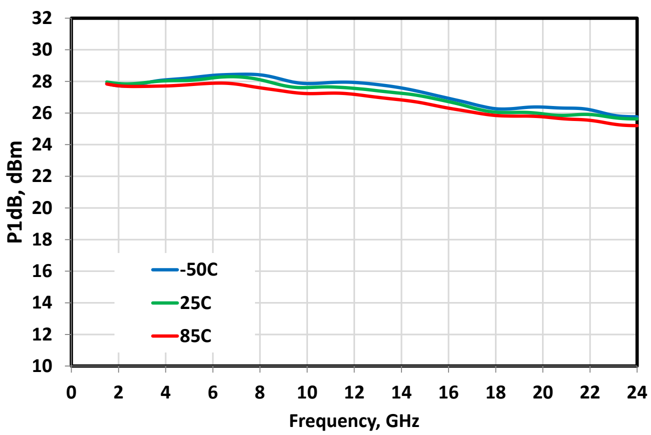


Figure 24 - P1dB vs. Temperature @ 10V/360mA

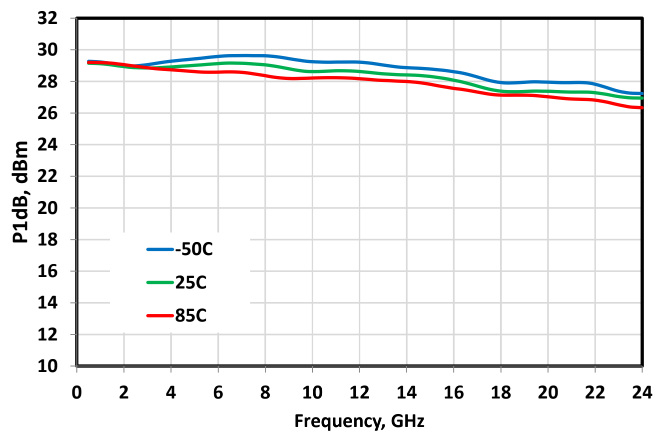


Figure 25 - Psat vs. Temperature @ 5V/220mA

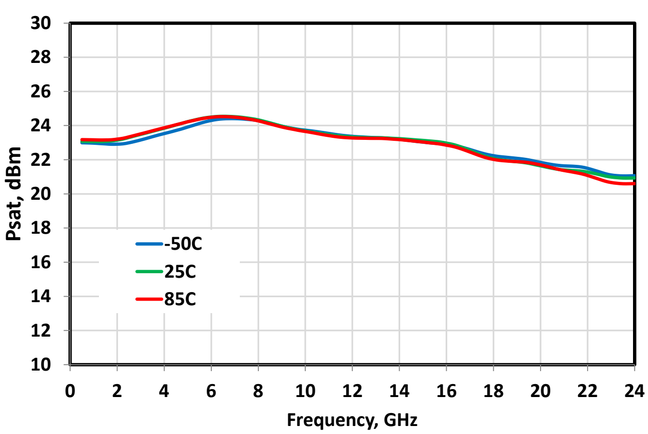


Figure 26 - Psat vs. Temperature @ 8V/270mA

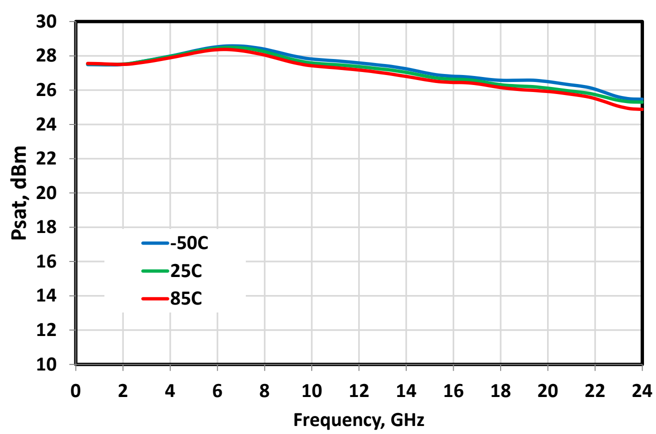


Figure 27 - Psat vs. Temperature @ 9V/310mA

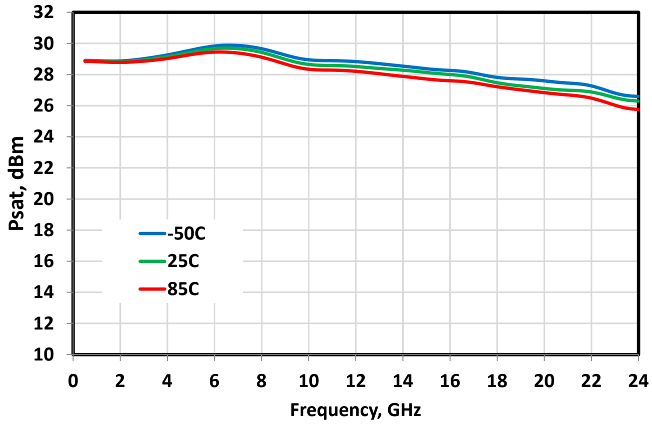


Figure 28 - Psat vs. Temperature @ 10V/360mA

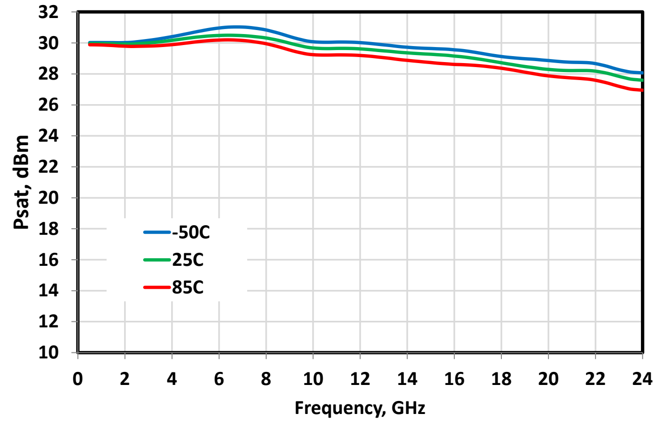


Figure 29 - OIP3 vs. Temperature @ 5V/220mA

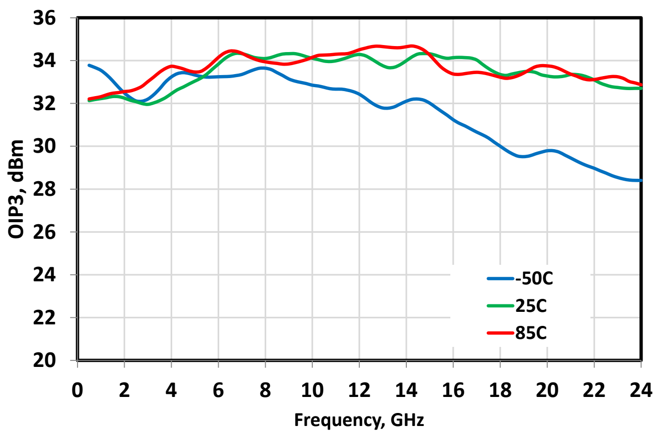


Figure 30 - OIP3 vs. Temperature @ 8V/270mA

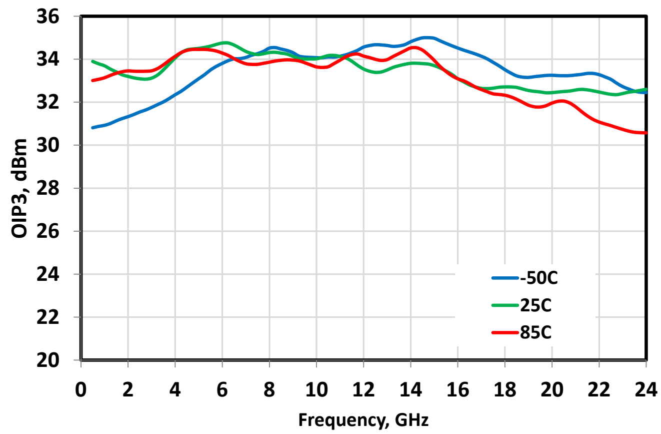


Figure 31 - OIP3 vs. Temperature @ 9V/310mA

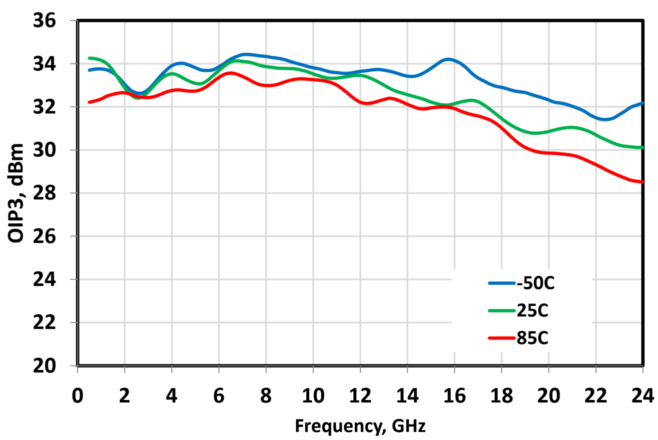


Figure 32 - OIP3 vs. Temperature @ 10V/360mA

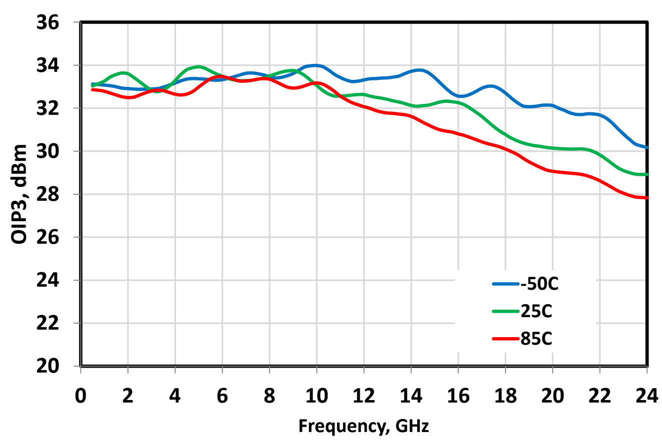


Figure 33 - OIP2(low) vs. Temperature @ 5V/220mA

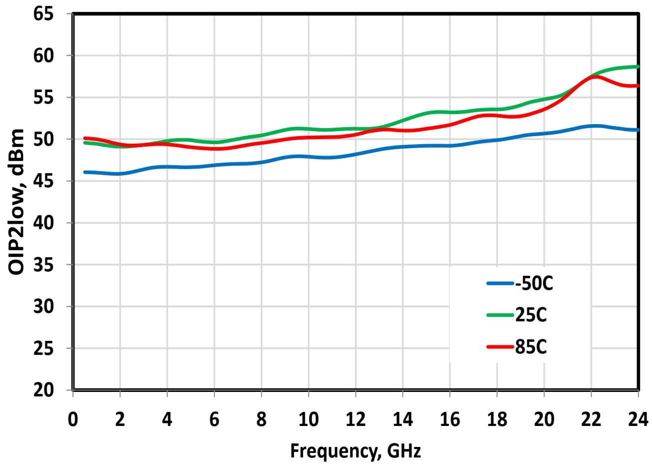


Figure 34 - OIP2(low) vs. Temperature @ 8V/270mA

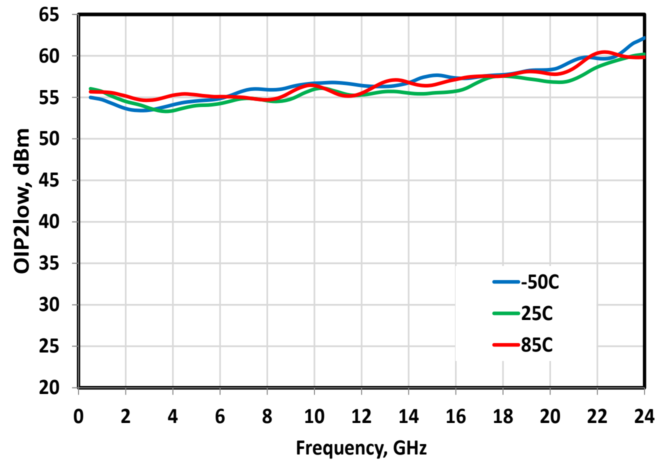


Figure 35 - OIP2(low) vs. Temperature @ 9V/310mA

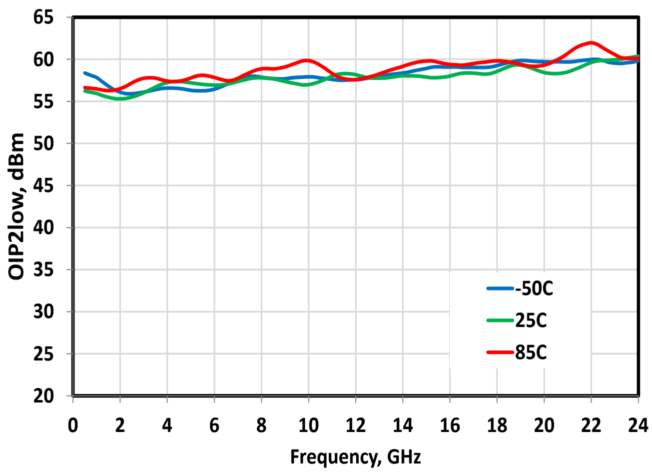


Figure 36 - OIP2(low) vs. Temperature @ 10V/360mA

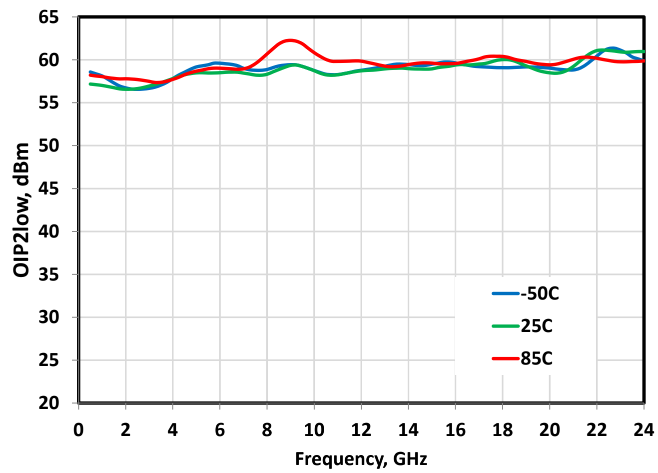


Figure 37 - IM3 vs. Temperature @ 5V/220mA, 20dBm(per tone)

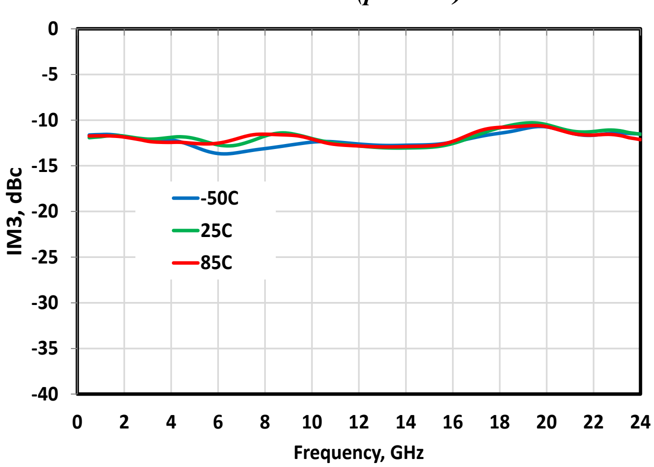


Figure 38 - IM3 vs. Temperature @ 8V/270mA, 20dBm(per tone)

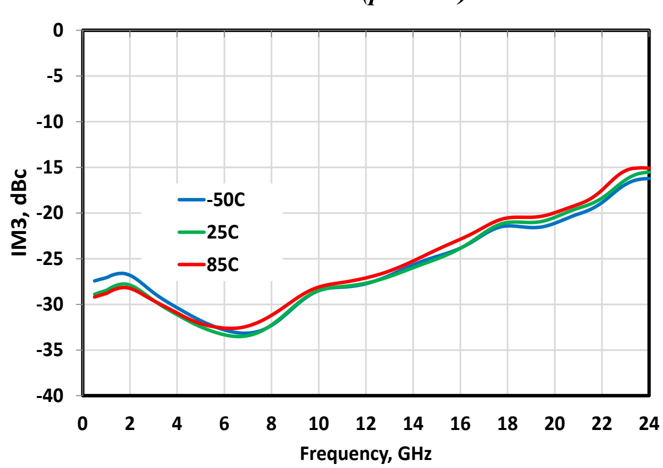


Figure 39 - IM3 vs. Temperature @ 9V/310mA, 20dBm(per tone)

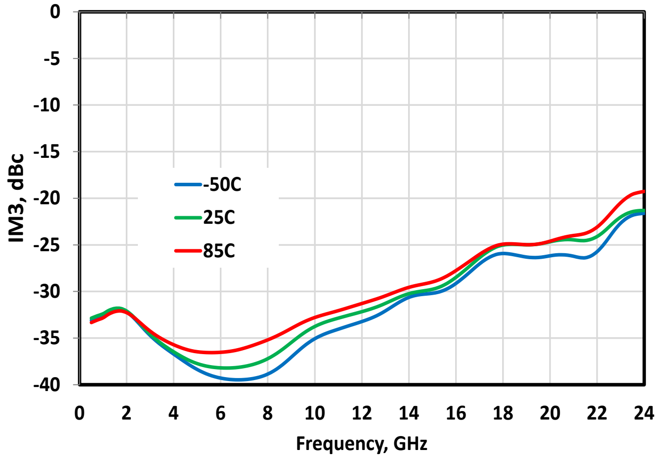
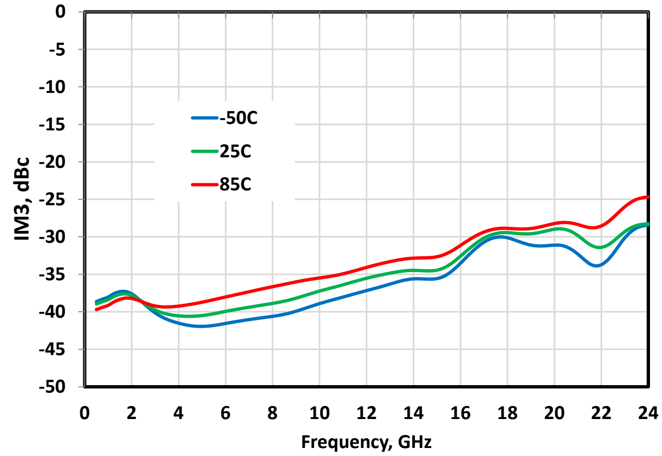


Figure 40 - IM3 vs. Temperature @ 10V/360mA, 20dBm(per tone)



1.1.2 Typical Performances vs. Bias

The following graphs show the typical performance curves of the MMA052PP45 device at 25 °C vs. Bias conditions; measurements performed using application circuit shown on Figure 71 - below. Currents were set by States according to Table 3-3

Figure 41 - Gain vs. V_{DD} @ State 1

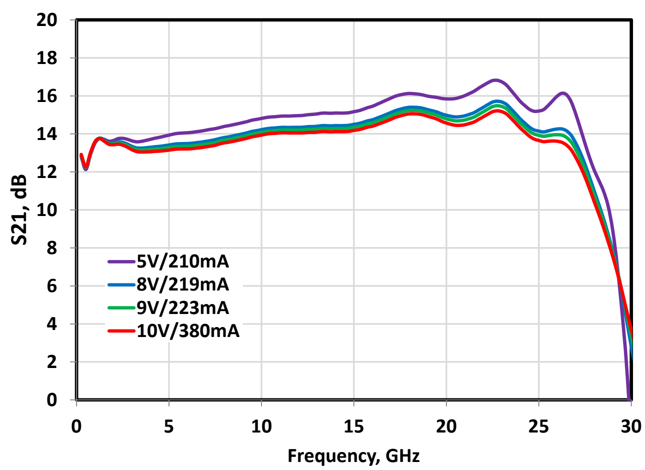


Figure 42 - Gain vs. V_{DD} @ State 5

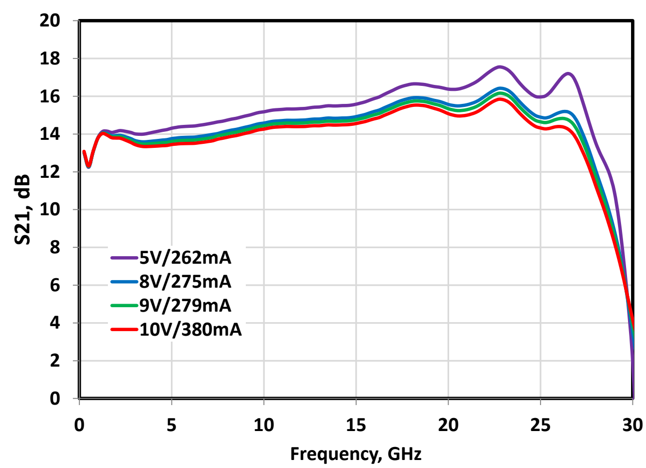


Figure 43 - Gain vs. V_{DD} @ State 8

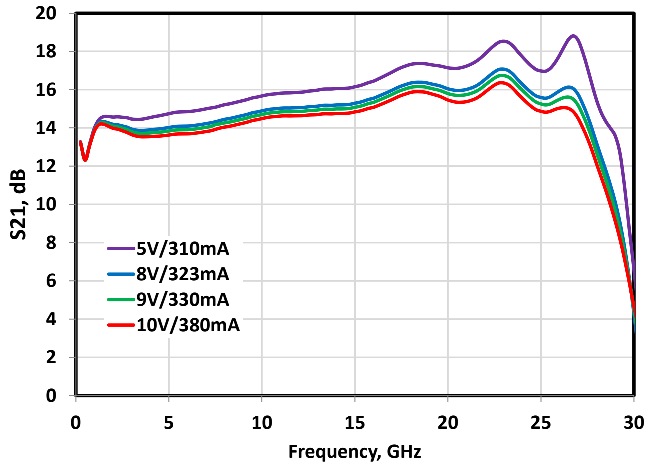


Figure 44 - Gain vs. V_{DD} @ State 16

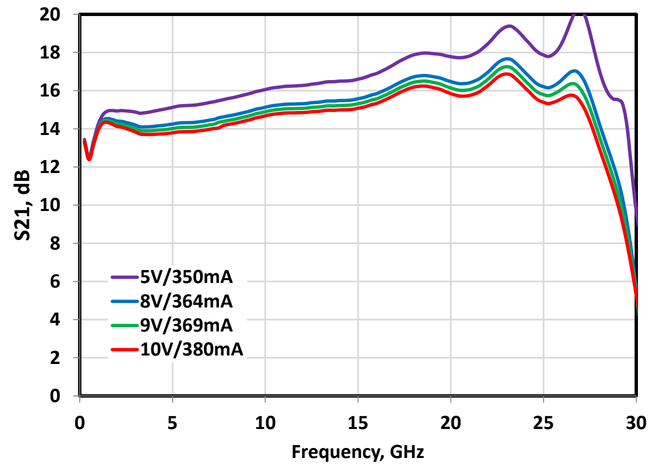


Figure 45 - NF vs. V_{DD} @ State 1

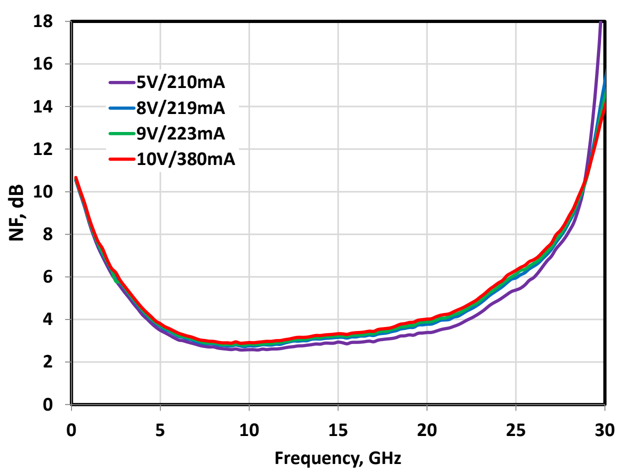


Figure 46 - NF vs. V_{DD} @ State 5

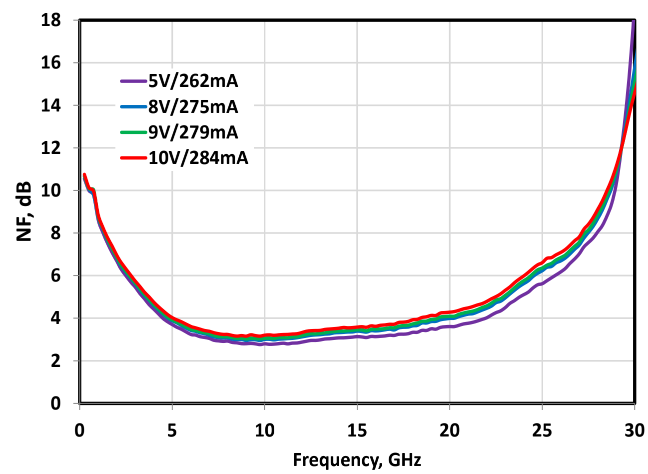


Figure 47 - NF vs. V_{DD} @ State 8

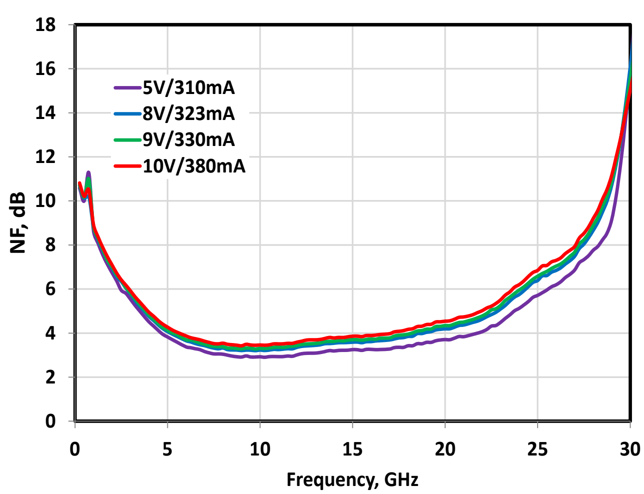


Figure 48 - NF vs. V_{DD} @ State 16

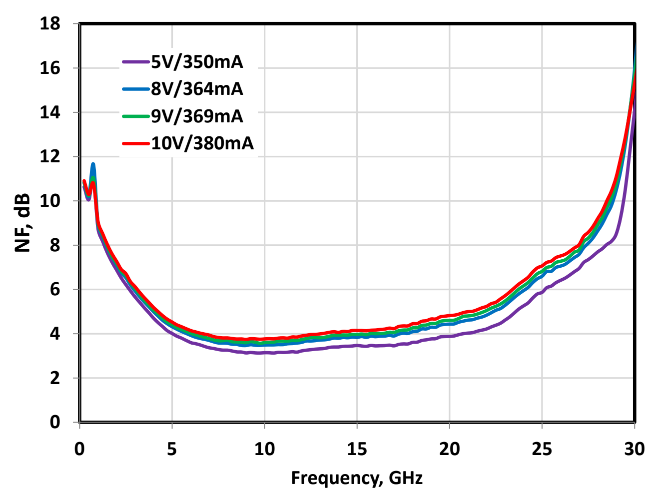


Figure 49 - P1dB vs. V_{DD}/ I_{DD}

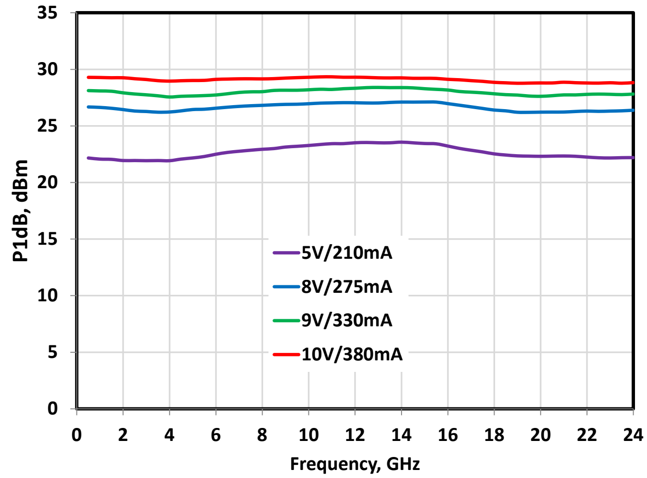


Figure 50 - Psat vs. V_{DD}/I_{DD}

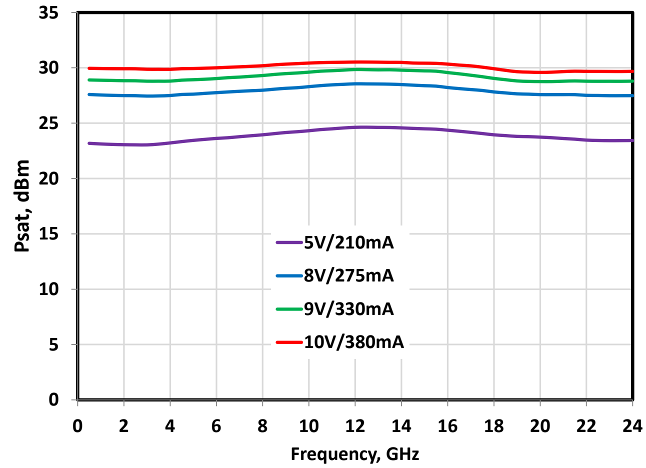


Figure 51 - OIP3 vs. V_{DD}/I_{DD}

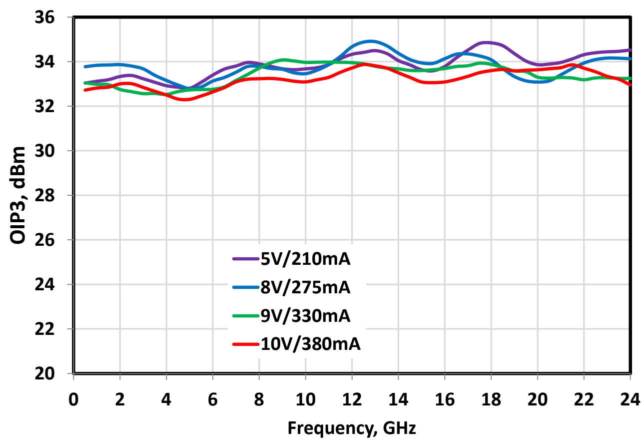


Figure 52 - OIP2 Low a t Δ=10MHz vs. V_{DD}/I_{DD}

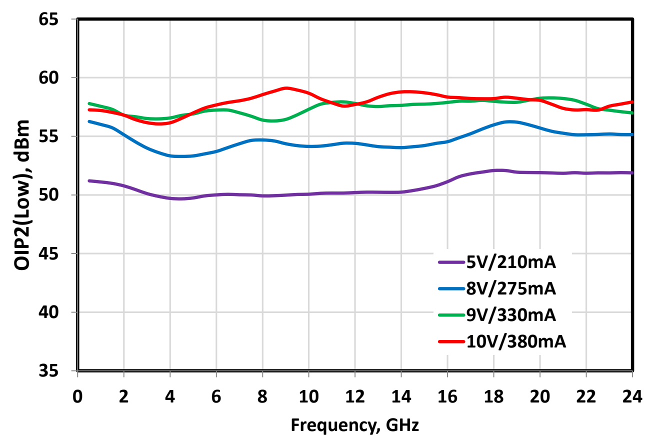
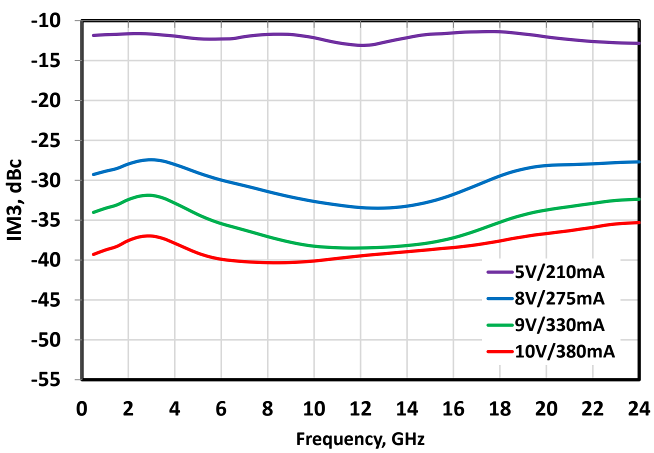


Figure 53 - IM3 vs . V_{DD}/I_{DD}, 20dBm(per tone)



1.1.3 Typical Performances vs. Output Power

The following graphs show the typical performance curves of the MMA052PP45 device at 25 °C vs. Bias conditions, measurements performed using application circuit shown on Figure 71 - below. Currents were set by States according to Table 3-3

Figure 54 - IM2 v s. Power @ 5V/220mA

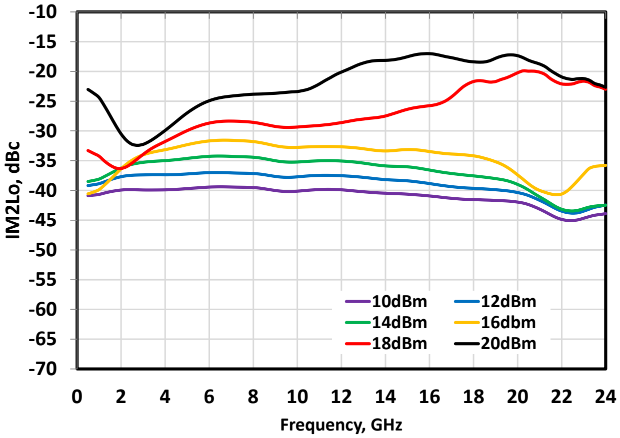


Figure 55 - IM2 vs. Power @ 8V/270mA

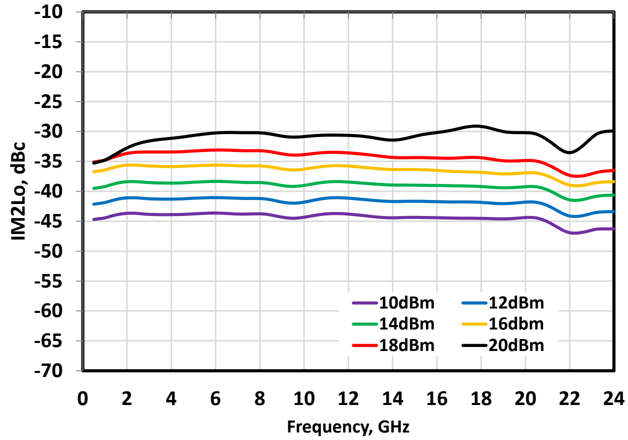


Figure 56 - IM2 vs. Power @ 9V/310mA

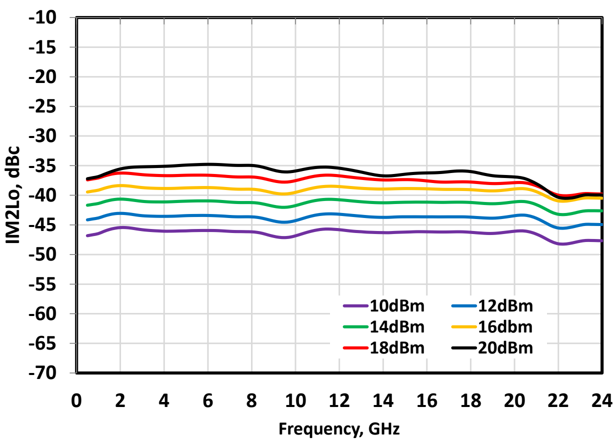


Figure 57 - IM2 vs. Power @ 10V/360mA

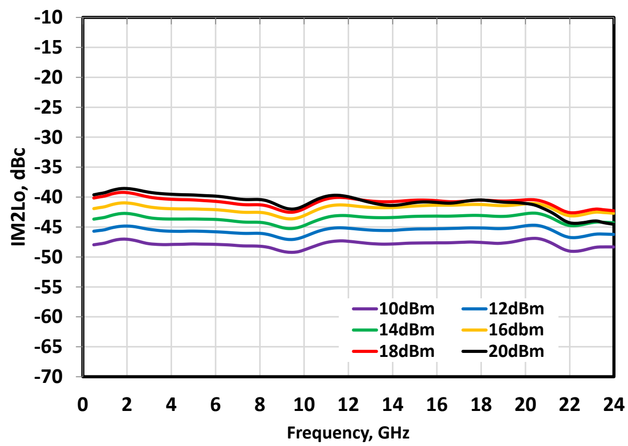


Figure 58 - IM3 vs. Power @ 5V/220mA

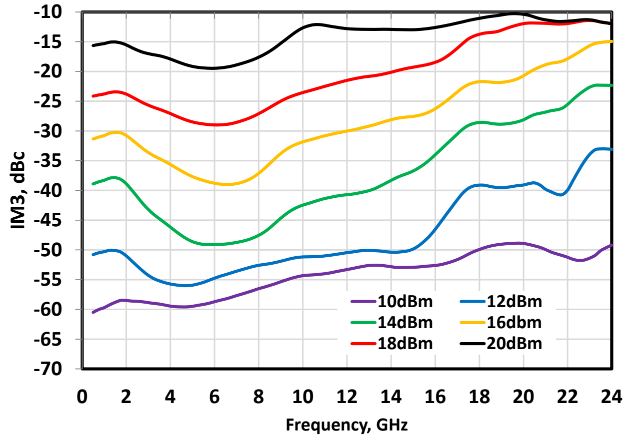


Figure 59 - IM3 vs. Power @ 8V/270mA

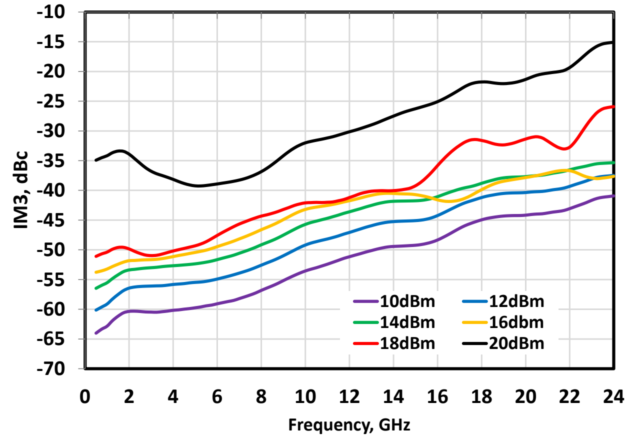


Figure 60 - IM3 vs. Power @ 9V/310mA

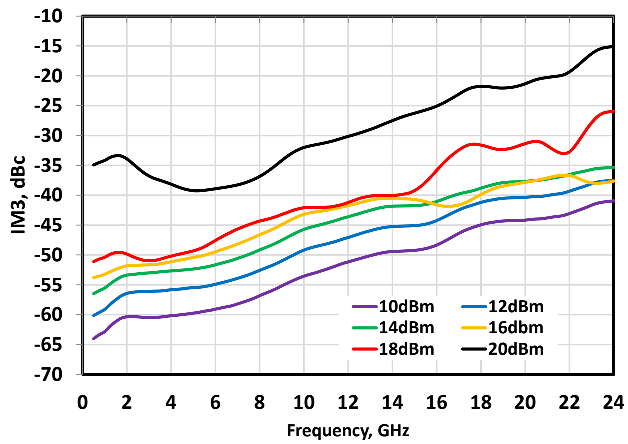


Figure 61 - IM3 vs. Power @ 10V/360mA

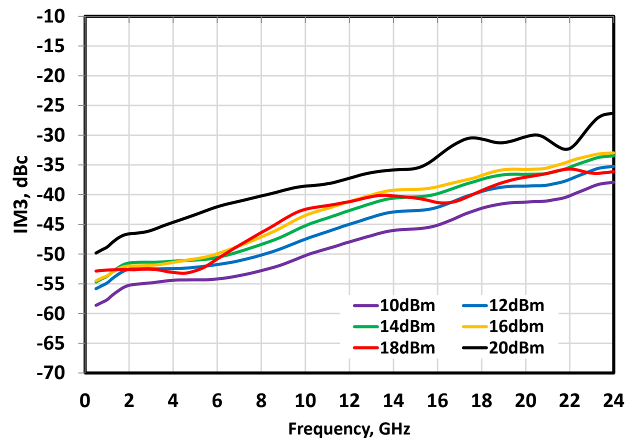


Figure 62 - 2-nd Harmonic vs. Power @ 5V/220mA

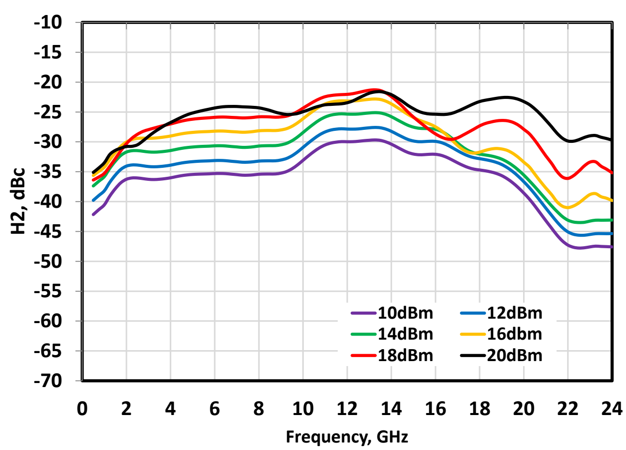


Figure 63 - 2-nd Harmonic vs. Power @ 8V/270mA

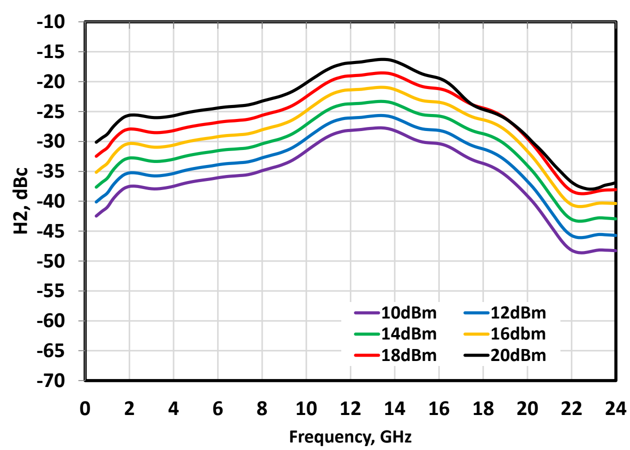


Figure 64 - 2-nd Harmonic vs. Power @ 9V/310mA

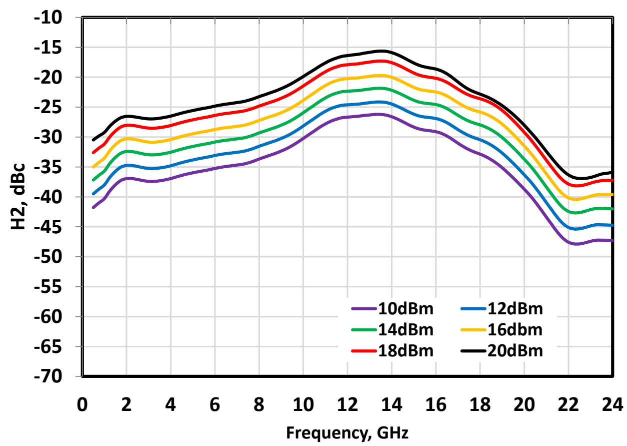


Figure 65 - 2-nd Harmonic vs. Power @ 10V/360mA

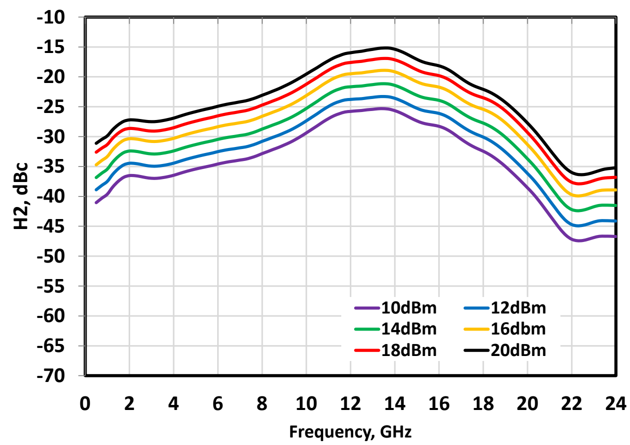


Figure 66 - I_{DD} Current vs. Power, at 10V

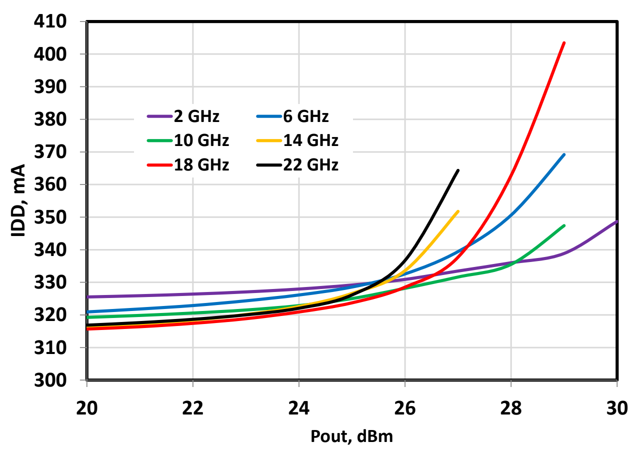
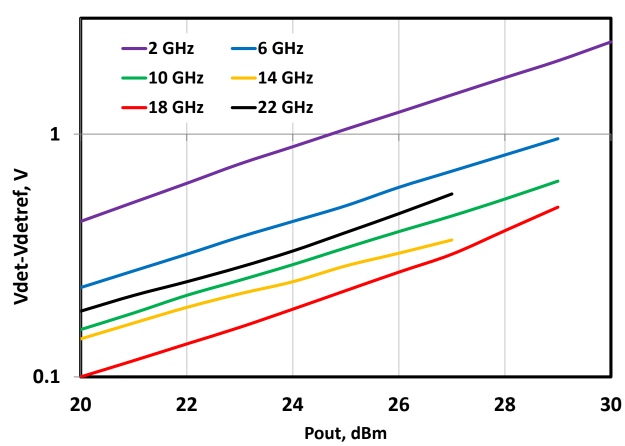


Figure 67 - V_{DET}-V_{DETREF} vs. Power



2. Package Specifications

The following illustration shows the package outline of the MMA052PP45 device. Dimensions are in millimeters [inches].

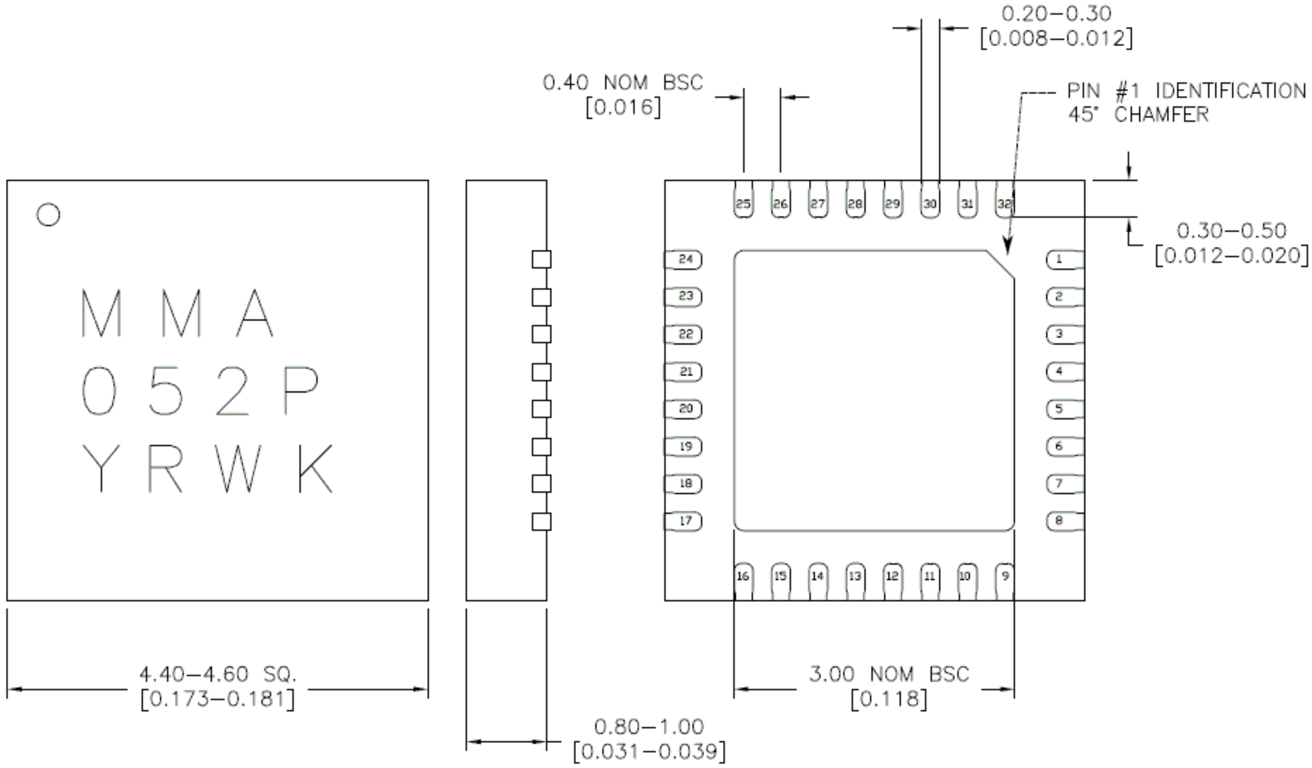


Figure 68 - Die Outline Drawing (mm)

Table 3 - I/O Description

Package	4.5mm X 4.5mm 32L Plastic QFN
Lead Frame	C194 Cu
Plating	Ni/Pd/Au
Package Body Material	RoHS Compliant Low-stress injection molded plastic

Table 4 - I/O Description

Pad Number	Pad Name	Pad Description
4, 5	RF_{IN}	Pin 4 and 5 must be merged on the layout and are matched to 50 Ω, and DC coupled to gate 1. (See figure 3-3 layout pattern.)
21, 22	RF_{OUT}	Pin 21 and 22 must be merged on the layout and are matched to 50 Ω, These pins are used for VDD Bias. (See figure 3-3 layout pattern.)
1	V_{GG}	Bias for VG2, must be coupled to VDD by connecting it to VDA or VDB externally for nominal operation (Alternately, this pin could be used for gain/linearity fine tuning)
10, 12, 14, 16	V_{SB}	Self-biasing resistors terminals, to adjust bias current by shorting one or several to the ground (see Table 3.3), if not used Die will operate with it's default current (about 200mA)
28	V_{DET}	Detector pin, with DC voltage as function of output power, for correct operation of detector use VDET-VDETREF at external comparator
29	V_{DETREF}	Detector reference voltage

30, 32	V_{DA} ,V_{DB}	DC linked to VDD internally. External bypass capacitors are required to extend RF match and gain flatness below 2 GHz. Not intended for VDD bias
3, 6, 20, 23, Middle Pad	Ground	Should be connected to RF/DC ground with as many vias as possible, see our recommended landing pattern as example
2, 7, 8, 9, 11, 13, 15, 17, 18, 19, 24, 25, 26, 27 & 31	N/C	These pins are not connected internally. All data was measured with these pins connected to RF/DC ground externally.

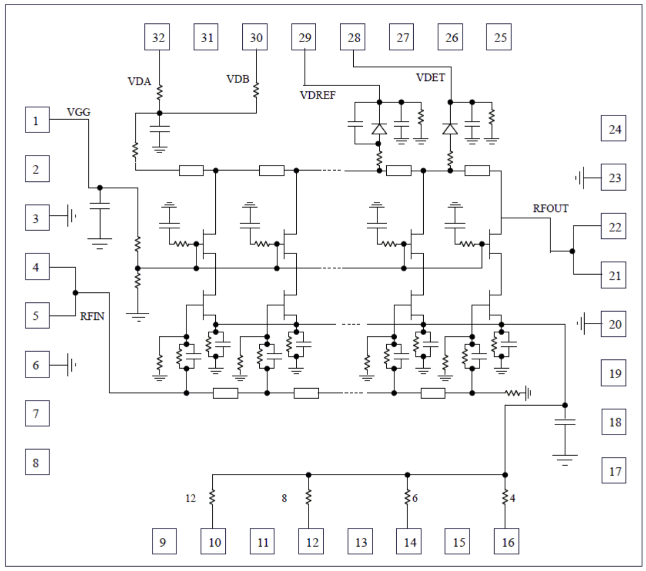


Figure 69 - Amplifier Functional Schematic

3. Application Circuits: Eval PCB

The following illustration shows the application circuit of the MMA052PP45E device. Note that there is no internal DC blocking capacitor on the input or the output, and a bias tee must be used on pin # 21 for biasing VDD

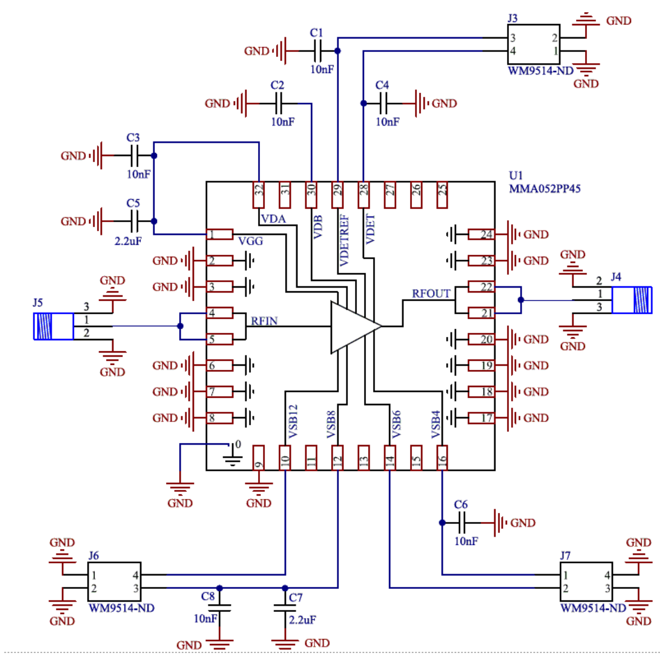


Figure 70 - MMA052PP45 Evaluation PCB

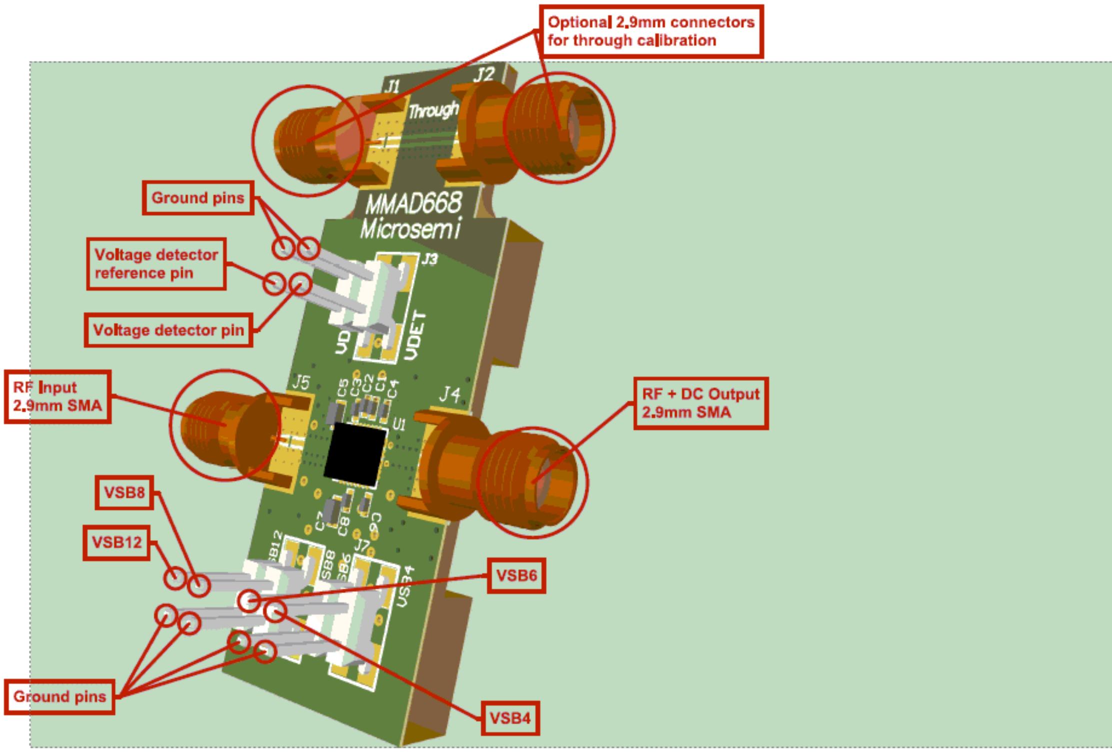


Figure 71 - Evaluation PCB

On the bottom two connectors where pins are labeled VSB12 through VSB4, the top row are connected internally to resistors that will change the drain current. The second row of pins below VSB12 through VSB4 are grounded. To use the different resistors in combinations to change the drain current jump the VSB pin to a ground pin as shown above. The average drain current values are listed below in table

Table 3-2. Bill of Material

Item Num.	Component designator	Description	Mnf. Part Num.	Mnf.	Qty.
1	U1	4.5 X 4.5 32 Leads QFN	MMA052PP45	Microchip	1
2	C1, C2, C3, C4, C6, C8	10000 pF ±10% 50V Ceramic Capacitor X7R 0402	GRM155R71H103KA88D	Murata	6
3	C5, C7	2.2 µF ±10% 16V Ceramic Capacitor X5R 0603	GRM21BR71C225KA12L	Murata	2
4	J1, J2, J4, J5	Connector, 2.9mm Jack PCB Edge Mount .012 pin	25-146-1000-90	Winchester Interconnect	4
5	J3, J6, J7	Header, 2-Pin, Dual row	15-91-2040	Molex	3

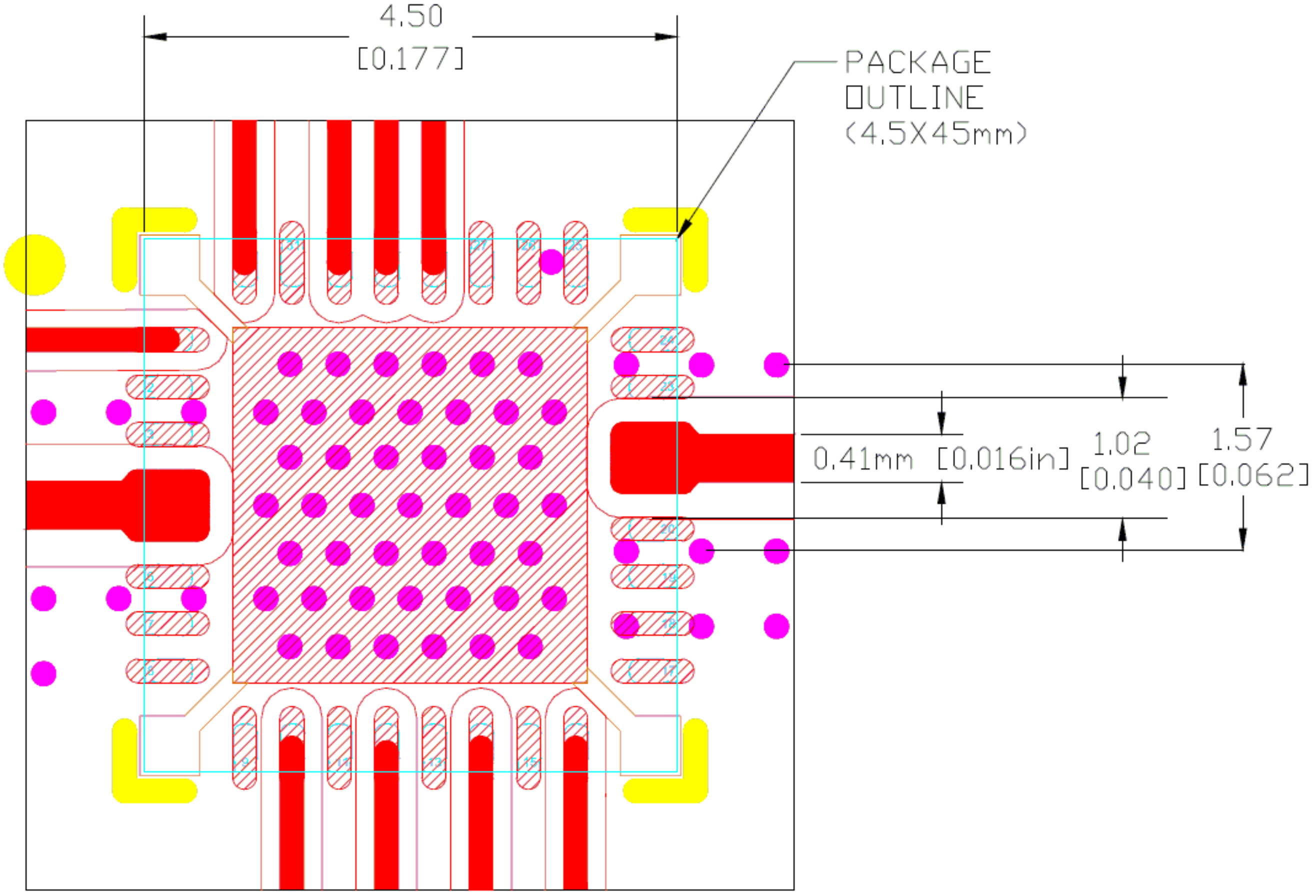
Table 3.2 MMA052PP45E Bias Sequence

Step	Bias Sequence
1	Make sure all DC and RF connections are attached before activating any DC voltage or supplies.
	Note: DC supply for VDD should be fed through an external bias-T on the RF+ DC output port (J4).
2	Make sure RF input port has no DC supplied to it as it will be terminated to grounded 50 Ohm.
3	Set VDD at 10.0V with current compliance at 400mA.
4	Use short jumpers on J6 and J7 headers to set IDD using internal resistors.
	Note: To short a resistor pin, connect a jumper to the ground pin below it.
	There are five combinations (always measure IDD current). 1. No jumpers (default IDD current = 200mA) 2. Jumper on VSB12: grounding 12Ohm resistor 3. Jumper on VSB8: grounding 8Ohm resistor 4. Jumper on VSB6: grounding 6Ohm resistor 5. Jumper on VSB4: grounding 4Ohm resistor Note: Use combination of jumpers to set required IDD current according to Table below.
	CAUTION: ENSURE NOT TO SHORT VDET OR VDETREF PINS TO AVOID DAMAGE TO PART

Table 3.3 I_{DD} currents vs V_{SB} positioning States at different Voltages V_{DD}

State	V_{SB12}	V_{SB8}	V_{SB6}	V_{SB4}	I_{DD} at 5V	I_{DD} at 8V	I_{DD} at 9V	I_{DD} at 10V
1	Open	Open	Open	Open	208	219	223	227
2	Short	Open	Open	Open	237	249	253	258
3	Open	Short	Open	Open	250	262	267	271
4	Short	Short	Open	Open	273	285	290	295
5	Open	Open	Short	Open	262	275	279	284
6	Short	Open	Short	Open	284	296	301	306
7	Open	Short	Short	Open	293	306	311	316
8	Short	Short	Short	Open	310	323	328	334
9	Open	Open	Open	Short	283	296	301	306
10	Short	Open	Open	Short	302	315	320	326
11	Open	Short	Open	Short	310	324	329	335
12	Short	Short	Open	Short	325	339	344	351
13	Open	Open	Short	Short	318	332	337	343
14	Short	Open	Short	Short	332	346	351	358
15	Open	Short	Short	Short	339	352	357	364
16	Short	Short	Short	Short	350	364	369	376

Figure 3-3. MMA052PP45 Landing Pattern (mm[inch])



4. Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

5. Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA052AA	Die
MMA052PP45	Package Part
MMA052PP45E	Evaluation PCB

5.1 Packing Information

Part Number	Description
MMA052PP45-TR	Tape and Reel

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