DC–10 GHz 1W Distributed Power Amplifier

Product Overview

MMA053PP5 is a Gallium Arsenide (GaAs) monolithic microwave integrated circuit (MMIC) PHEMT distributed power amplifier in plastic QFN package that operates between DC and 10 GHz. The amplifier provides 17 dB of gain, +43 dBm output IP3, and +31 dBm of saturated output power, while requiring only 350 mA from 10 V supply. Gain over DC to 8 GHz frequency range varies by only +/-0.5 dB, making the MMA053PP5 ideal for EW, ECM, RADAR, and test equipment application. The MMA053PP5 amplifier features Plastic Overmoded 5x5mm QFN Package and I/O that are internally matched to 50 Ω.

Key Features

- **Broadband performance: DC to 10 GHz**
- **High Gain: 17 dB**
- **High Saturated Power: 31 dBm**
- **Supply: 10 V at 350 mA**
- **50 Ohm matched input/output**
- **Die size: 3 x 2.25 x 0.075 mm**
- **Passivated space-qualified process listed on EPPL007-38**
- **Packaged in Overmolded 5X5mm QFN Plastic Package**

Functional Block Diagram

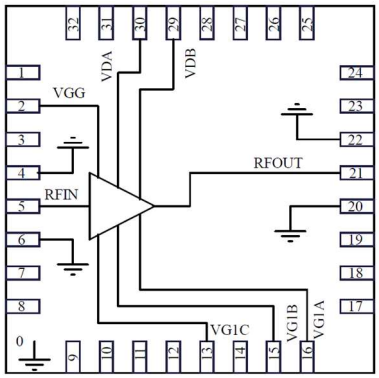


Figure 1 - Gain, IM3, Psat Performances

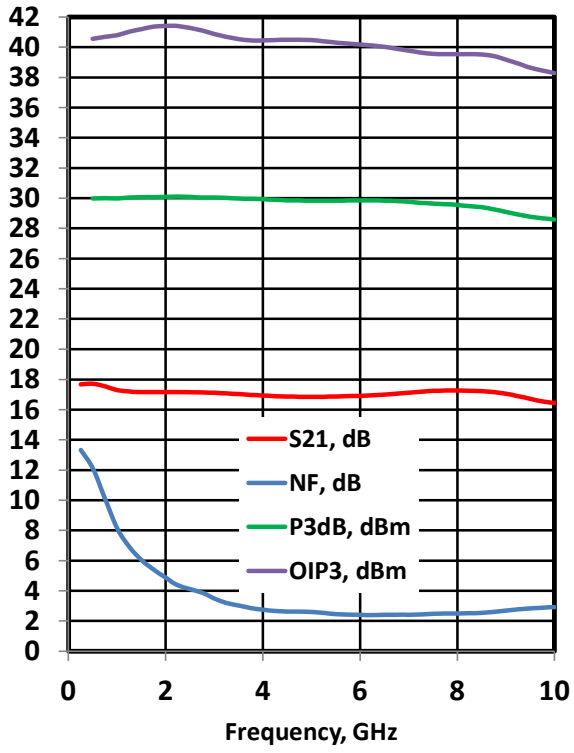
Applications

- Test and measurement instrumentation
- Military, EW, ECM, RADAR and space
- Telecom infrastructure
- Wideband microwave radios

Performance Overview

Parameter	Typ.	Units
Operational frequency range	DC-10	GHz
Gain	17	dB
P3dB	+31	dBm
OIP3	43	dBm
Current @ +10V Supply	350	mA
Operational frequency range	DC-10	GHz

Export Classification: EAR-99



Contents

1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1 - Typical Electrical Performance at 25 C, Vdd=10V, Idd=350 mA (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		10	GHz
Gain	DC–6 GHz	16	17		dB
	6 GHz–10 GHz	15.5	16.5		
Gain flatness	DC–6 GHz		0.2		
	6 GHz–10 GHz		0.5		
Noise figure	2–6 GHz		3	5	
	6 GHz–10 GHz		2.5	3	
Input return loss	DC–6 GHz	16	20		
	6 GHz–10 GHz	9	12		
Output return loss	DC–6 GHz	12	15		
	6 GHz–10 GHz	12	15		
P1dB	DC–6 GHz	26	27.5		dBm
	6 GHz–10 GHz	26	27		
Psat (Measured at 3dB Gain Compression)	DC–6 GHz	29	30		
	6 GHz–10 GHz	28	29		
OIP3	DC–6 GHz		40		
	6 GHz–10 GHz		40		
IM3 @ 20dBm	DC–6 GHz		-37		dBc
	6 GHz–10 GHz		-35		
Phase Noise			TBD		dBm/Hz
OIP2(low) (2-nd Order Intercept point F2-F1)			45		dBm
VDD (drain voltage supply)			10	11	V
IDD (drain current)			350	400	mA

1.2 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA053PP5 device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 2 - Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	12 V
Gate bias voltage (V_G)	–2 V to 0.5 V
RF input power (Pin)	17 dBm (or 6 dB Compression)
Channel temperature	165 °C
V_{DD} current (I_{DD})	520 mA
DC power dissipation (T = 85 °C)	5.7 W
Thermal resistance	14°C/W
Storage temperature	–65 °C to 150 °C
Operating temperature	–55 °C to 85 °C

ESD Sensitive Device

1.3 Typical Performance Curves

1.1.1 Typical Performances vs. Temperature

The following graphs show the typical performance curves of the MMA053PP5 device at specific bias conditions, measurements performed using application circuit shown on **Error! Reference source not found.** below.

Figure 1 - Gain vs. Temperature @ 5V/200mA

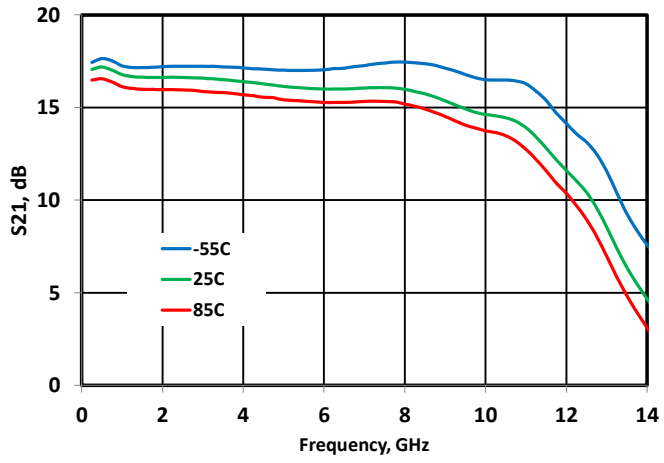


Figure 2 - Gain vs. Temperature @ 9V/300mA

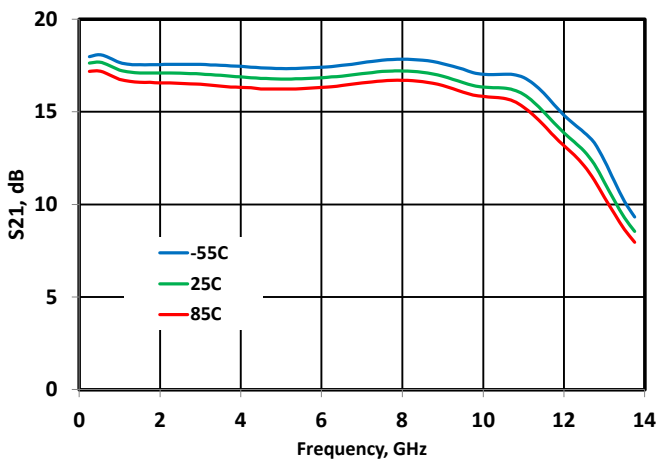


Figure 3 - Gain vs. Temperature @ 10V/350mA

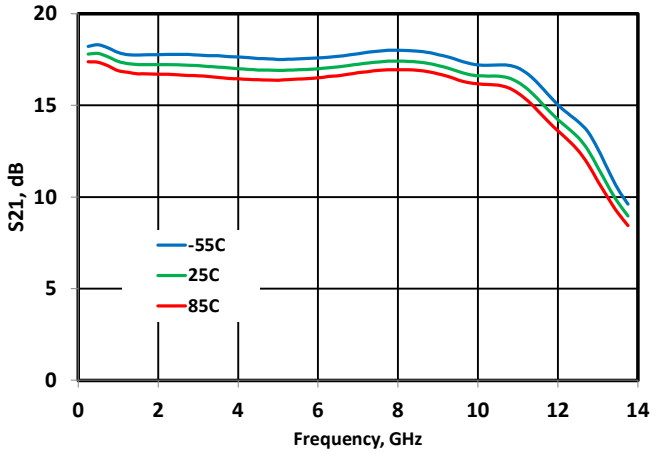


Figure 4 - Gain vs. Temperature @ 11V/400mA

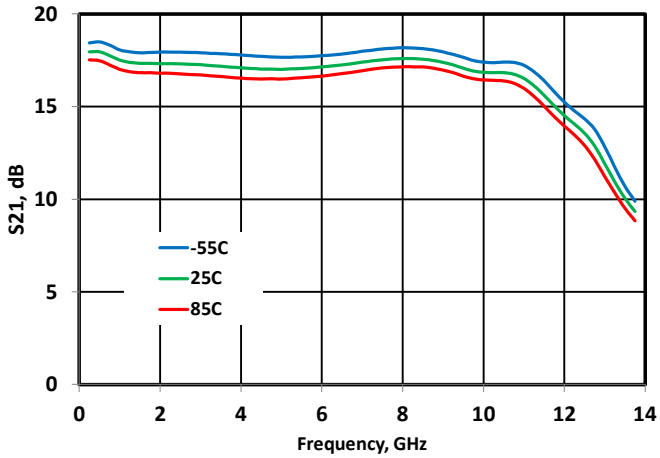


Figure 5 - S11 vs. Temperature @ 5V/200mA

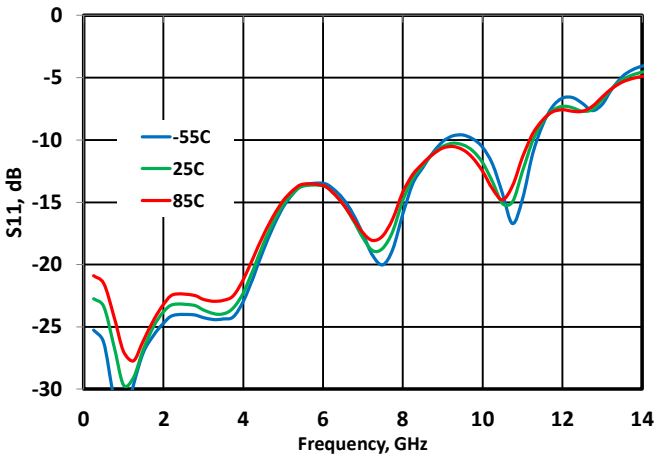


Figure 6 - S11 vs. Temperature @ 9V/300mA

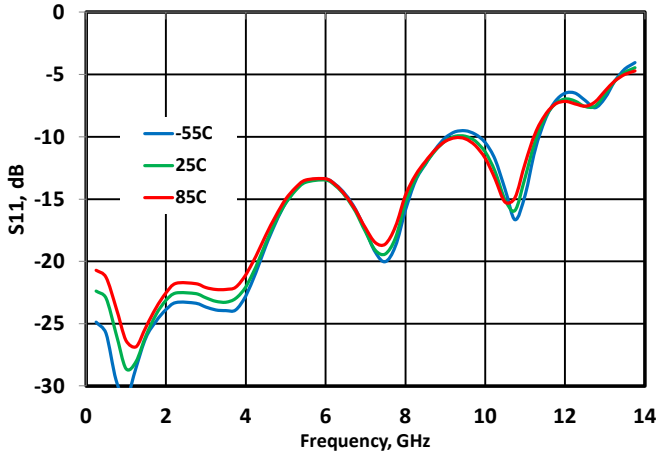


Figure 7 - S11 vs. Temperature @ 10V/350mA

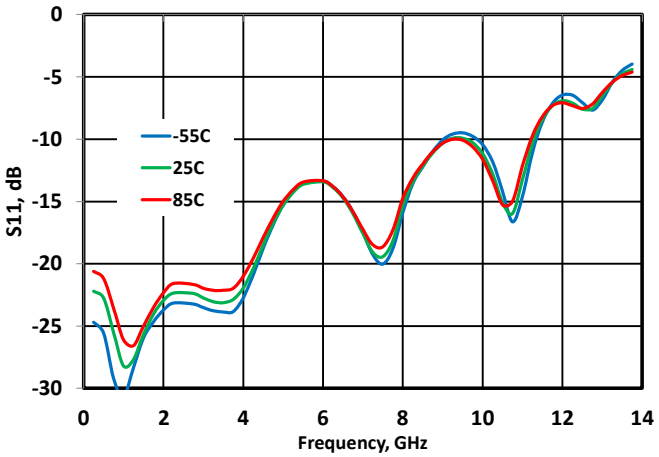


Figure 8 - S11 vs. Temperature @ 11V/400mA

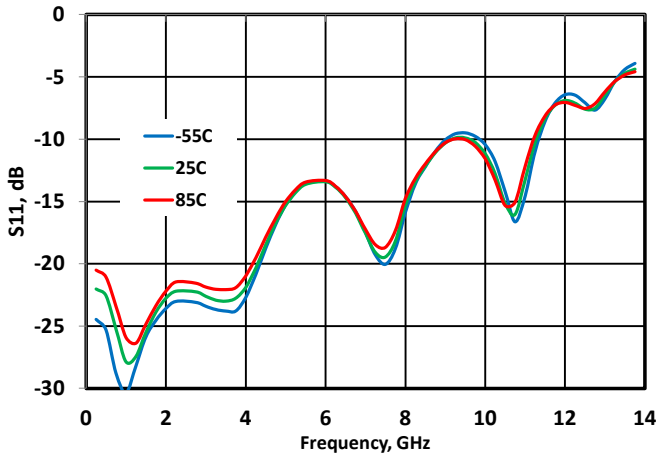


Figure 9 - S22 vs. Temperature @ 5V/200mA

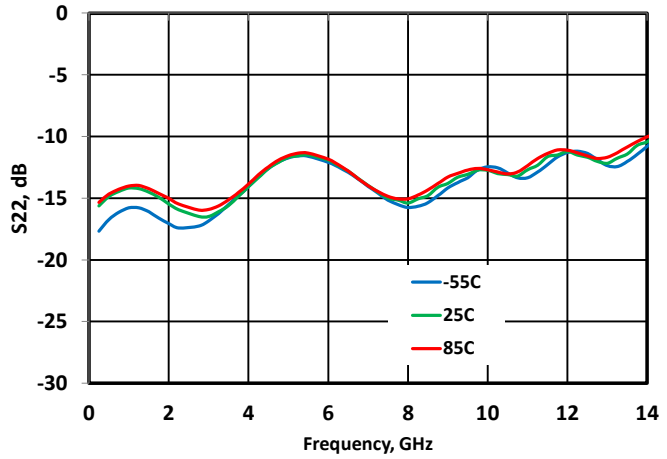


Figure 10 - S22 vs. Temperature @ 9V/300mA

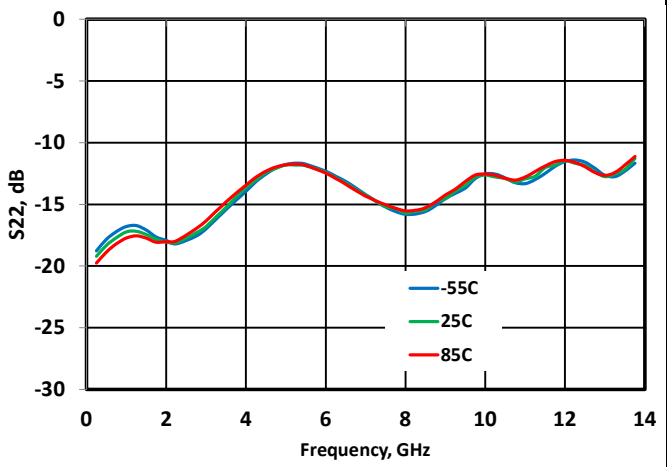


Figure 11 - S22 vs. Temperature @ 10V/350mA

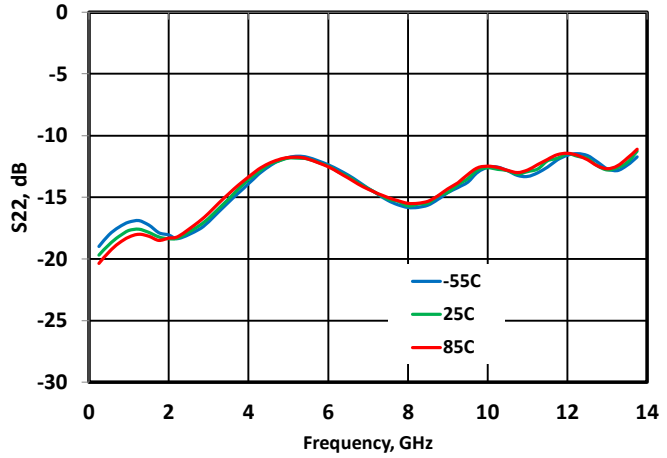


Figure 12 - S22 vs. Temperature @ 11V/400mA

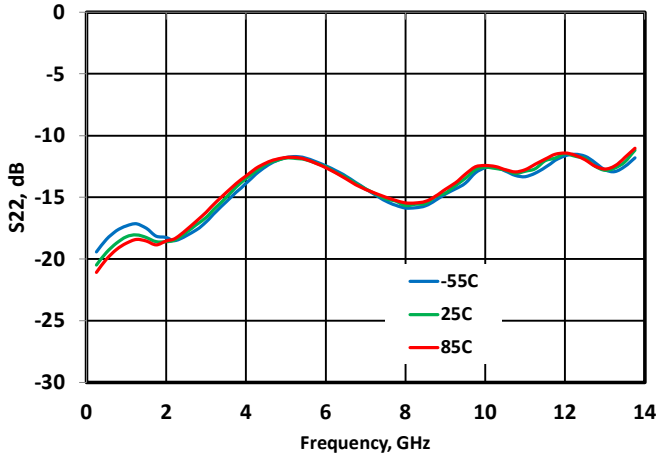


Figure 13 - S12 vs. Temperature @ 5V/200mA

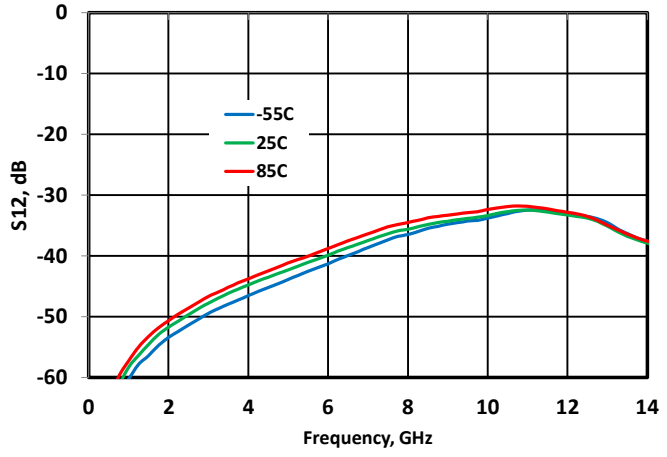


Figure 14 - S12 vs. Temperature @ 9V/300mA

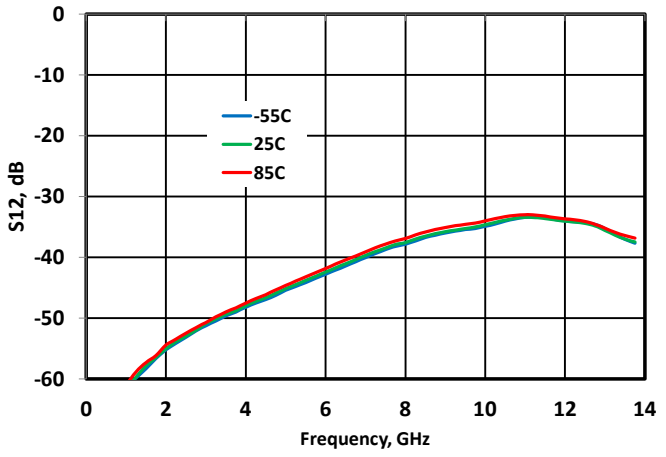


Figure 15 - S12 vs. Temperature @ 10V/350mA

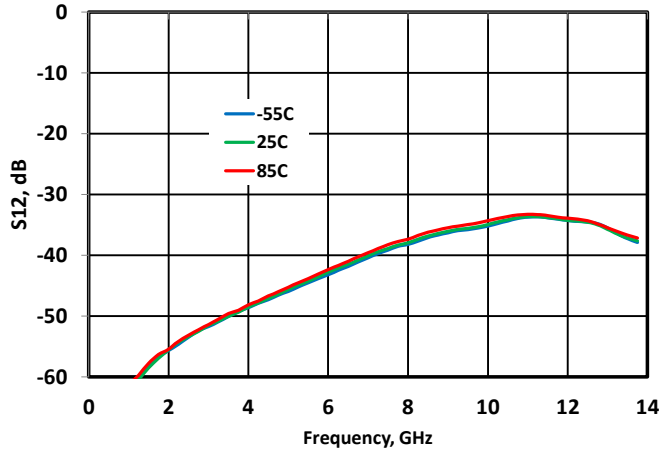


Figure 16 - S12 vs. Temperature @ 11V/400mA

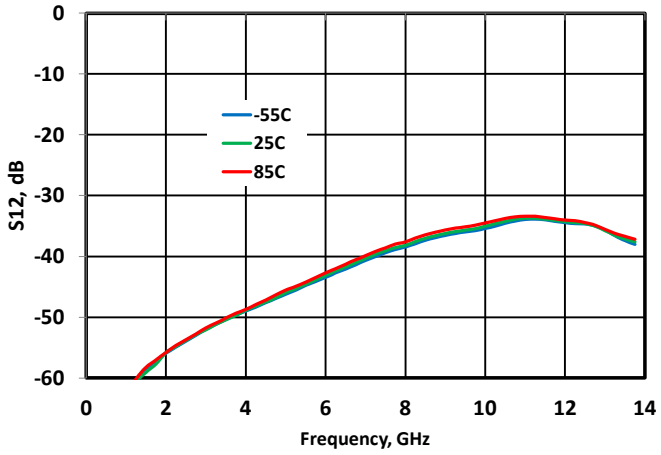


Figure 17 - NF vs. Temperature @ 5V/200mA

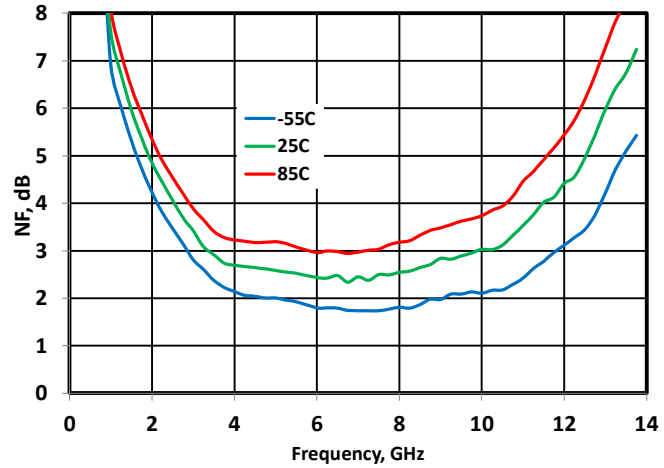


Figure 18 - NF vs. Temperature @ 9V/300mA

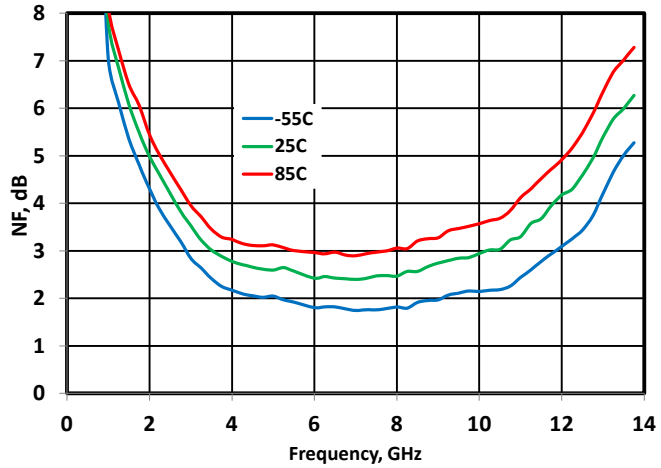


Figure 19 - NF vs. Temperature @ 10V/350mA

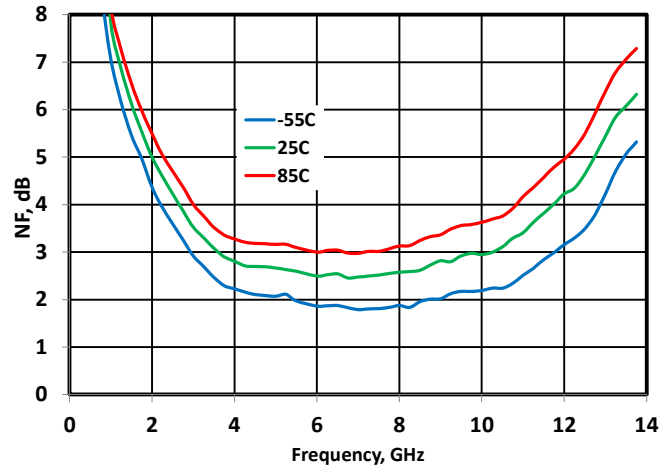


Figure 20 - NF vs. Temperature @ 11V/400mA

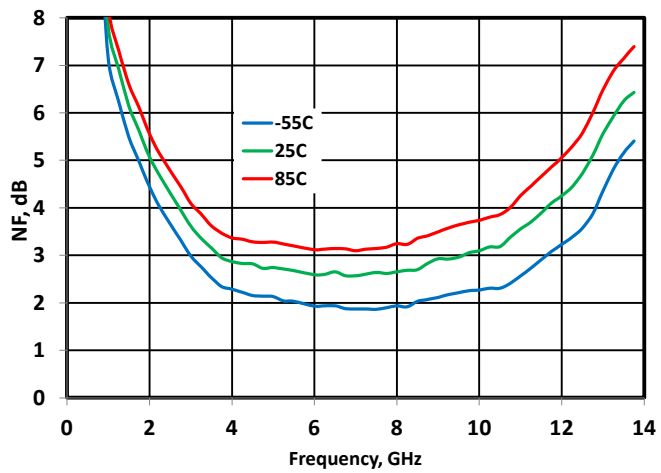


Figure 21 - P1dB vs. Temperature @ 5V/200mA

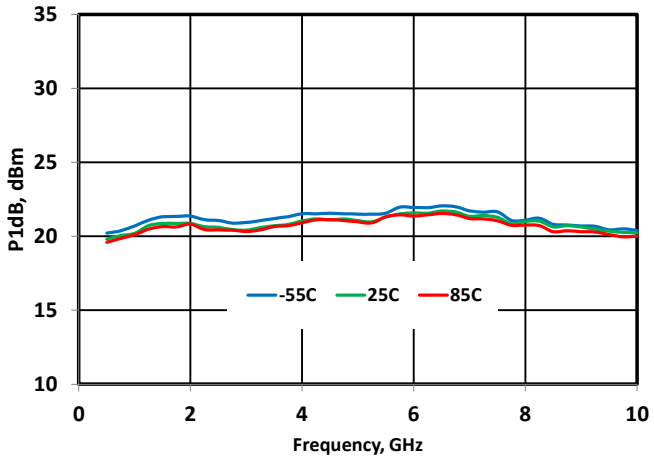


Figure 22 - P1dB vs. Temperature @ 9V/300mA

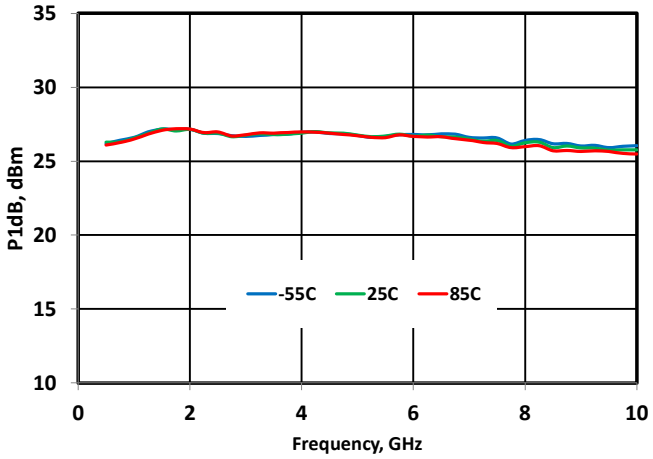


Figure 23 - P1dB vs. Temperature @ 10V/350mA

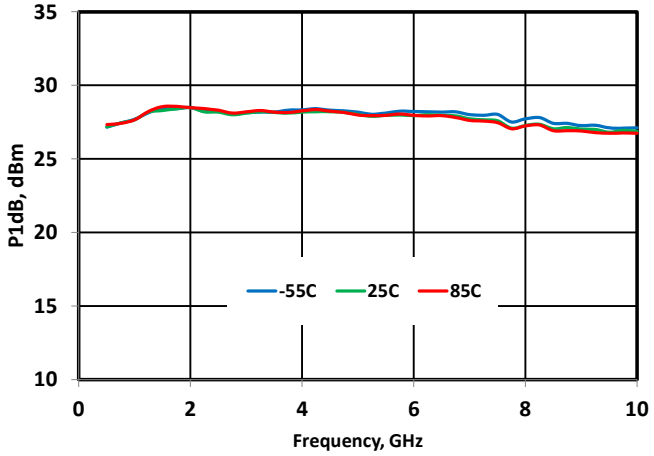


Figure 24 - P1dB vs. Temperature @ 11V/400mA

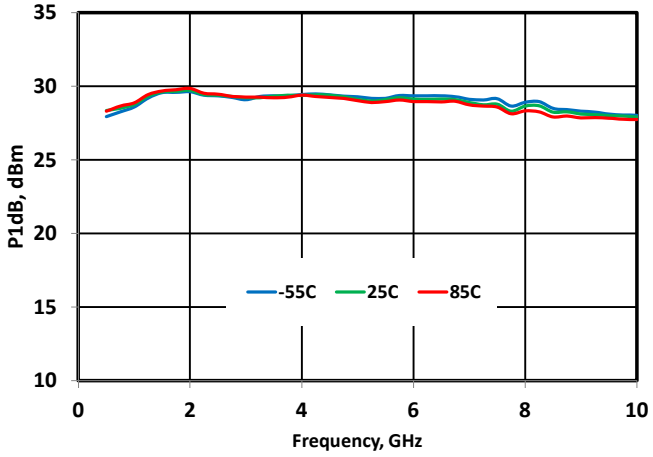


Figure 25 - Psat vs. Temperature @ 5V/200mA

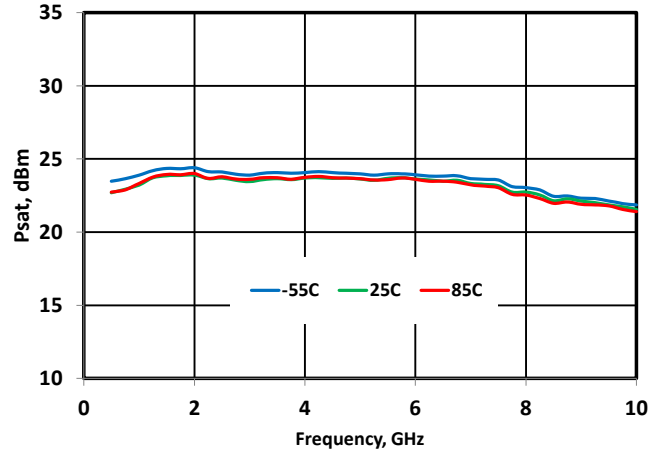


Figure 26 - Psat vs. Temperature @ 9V/300mA

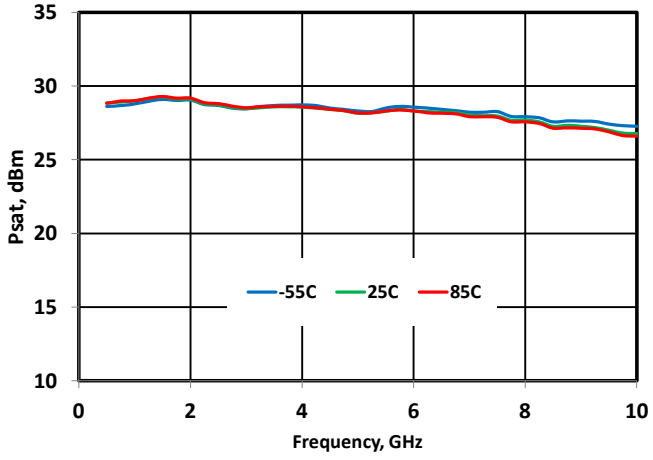


Figure 27 - Psat vs. Temperature @ 10V/350mA

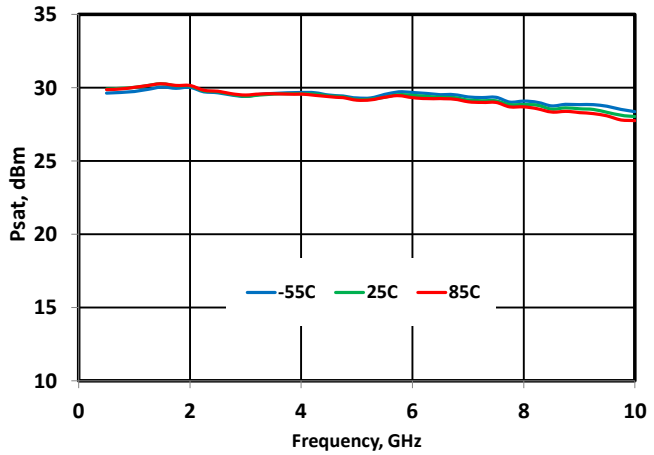


Figure 28 - Psat vs. Temperature @ 11V/400mA

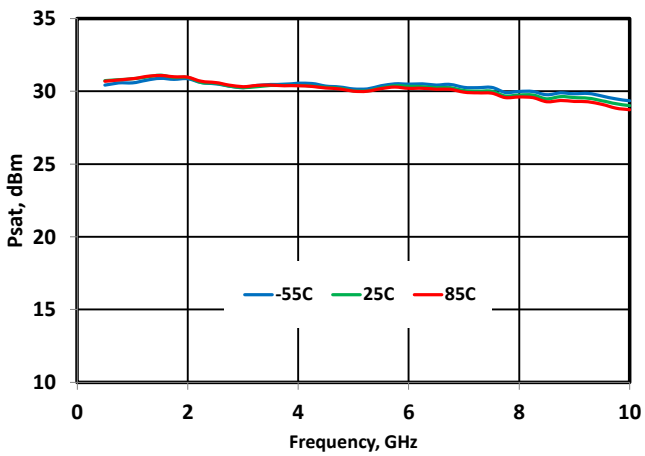


Figure 29 - OIP3 vs. Temperature @ 5V/200mA

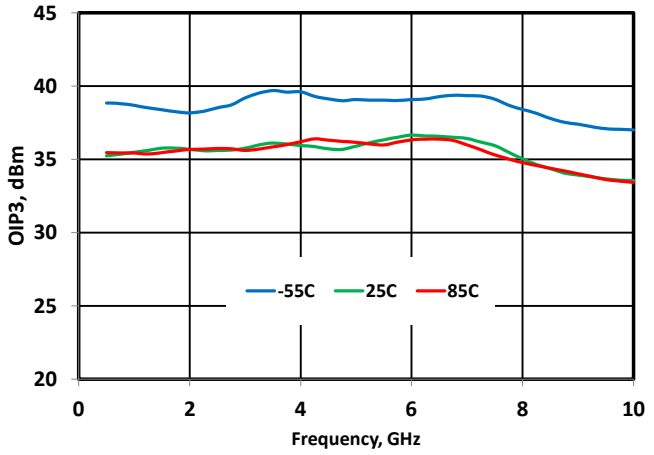


Figure 30 - OIP3 vs. Temperature @ 9V/300mA

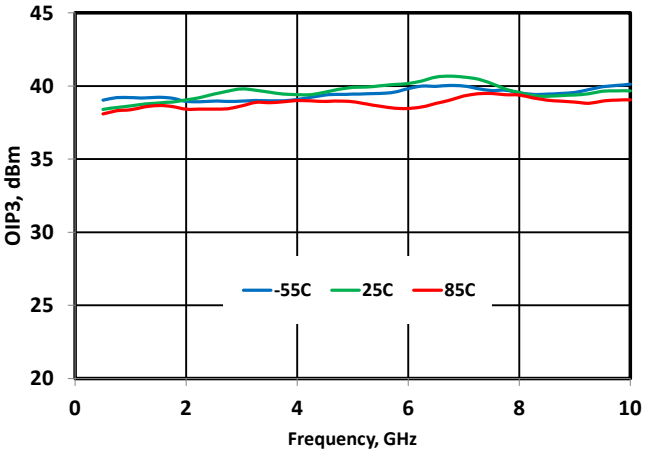


Figure 31 - OIP3 vs. Temperature @ 10V/350mA

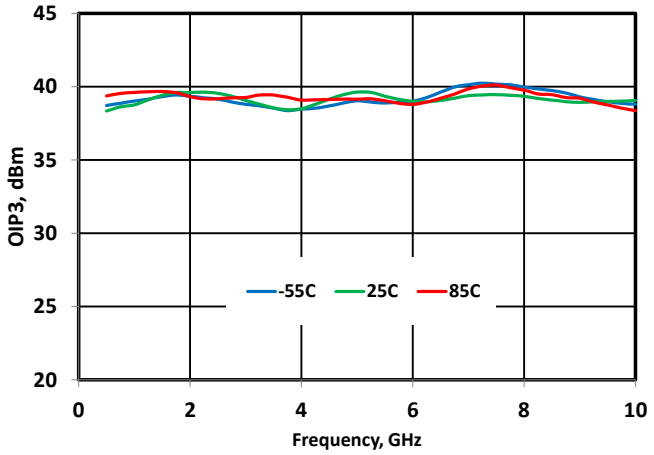


Figure 32 - OIP3 vs. Temperature @ 11V/400mA

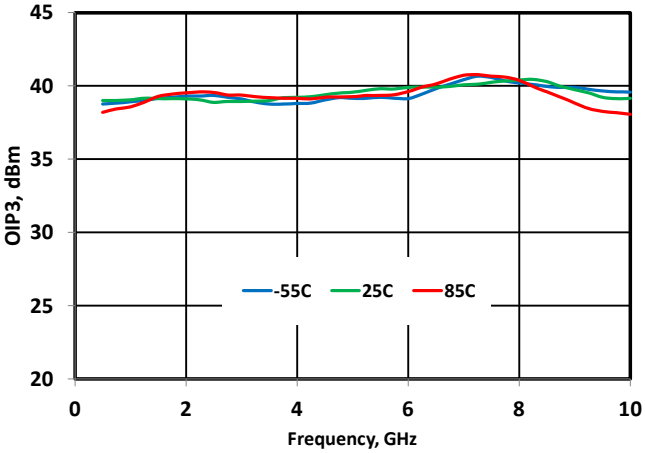


Figure 33 - OIP2(low) vs. Temperature @ 5V/200mA

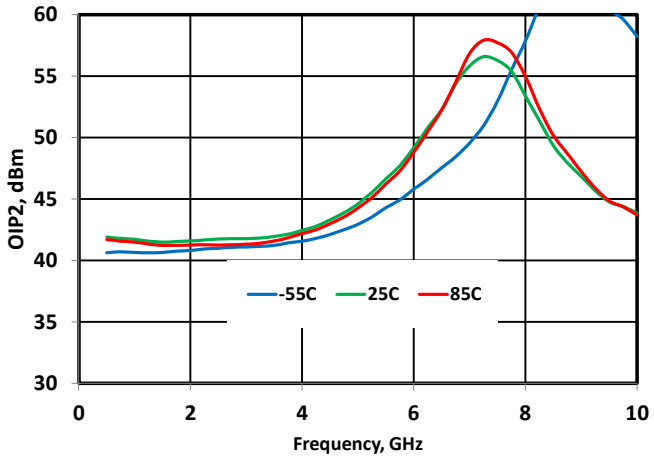


Figure 34 - OIP2(low) vs. Temperature @ 9V/300mA

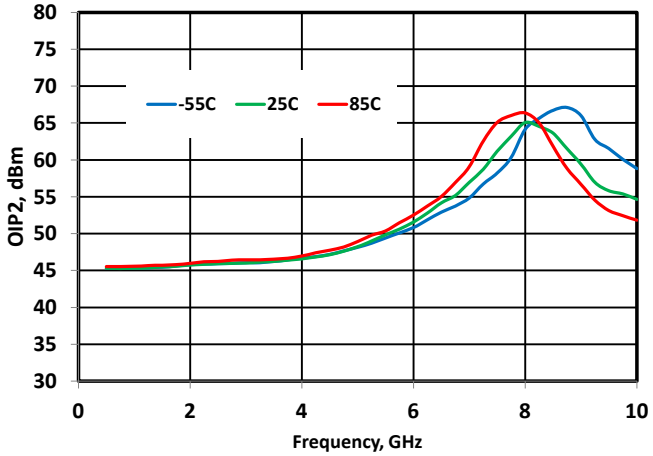


Figure 35 - OIP2(low) vs. Temperature @ 10V/350mA

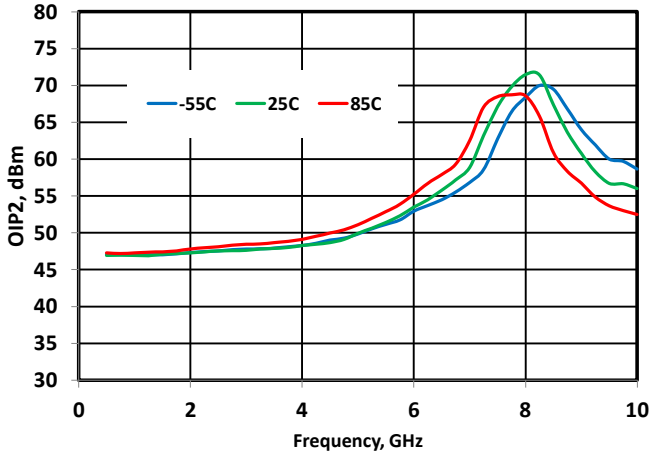


Figure 36 - OIP2(low) vs. Temperature @ 11V/400mA

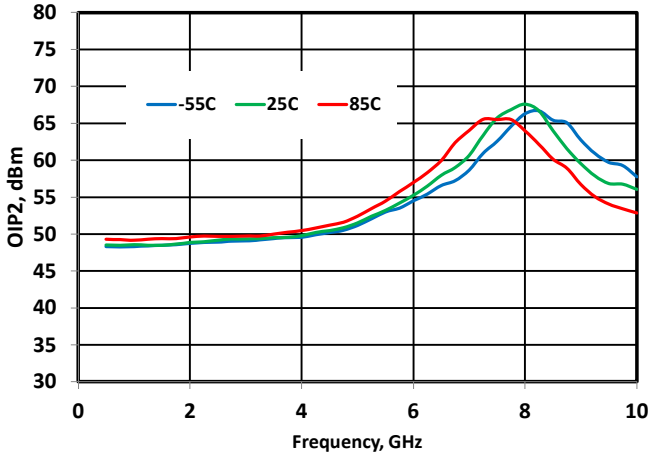


Figure 37 - IM3 vs. Temperature @ 5V/200mA, 20dBm(per tone)

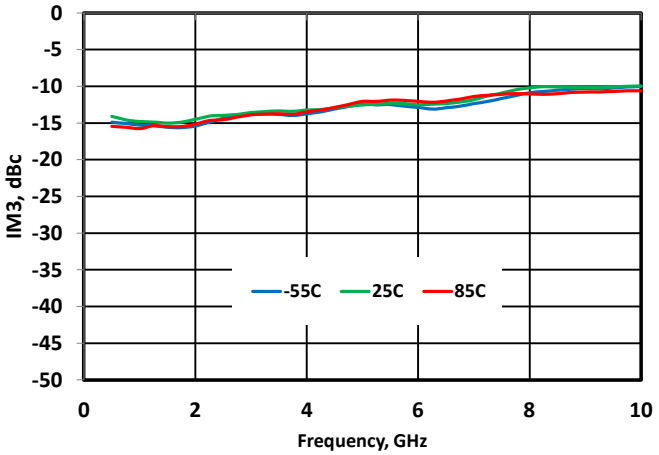


Figure 38 - IM3 vs. Temperature @ 9V/300mA, 20dBm(per tone)

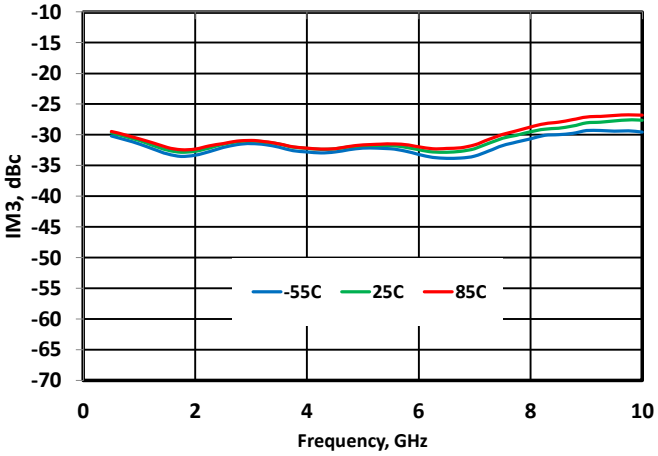


Figure 39 - IM3 vs. Temperature @ 10V/350mA, 20dBm(per tone)

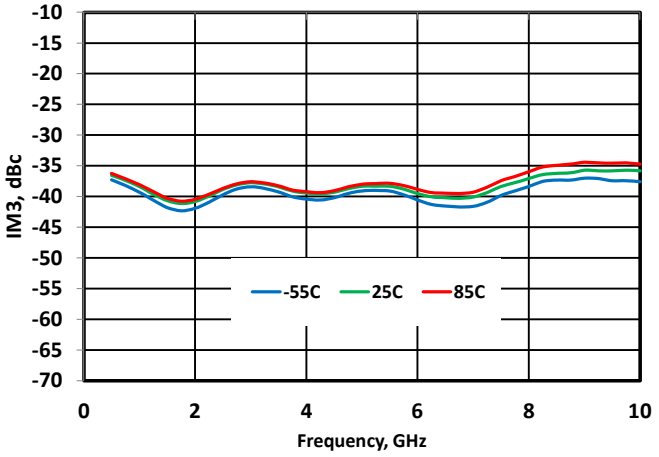
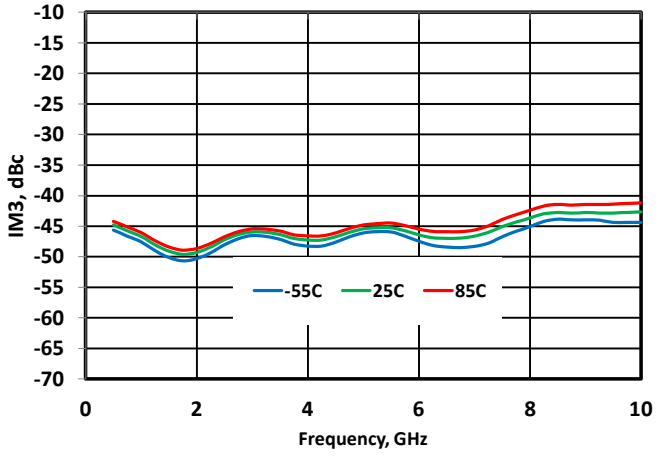


Figure 40 - IM3 vs. Temperature @ 11V/400mA, 20dBm(per tone)



1.1.2 Typical Performances vs. Bias

The following graphs show the typical performance curves of the MMA053AA device at 25 °C vs. Bias conditions, measurements performed using application circuit shown on **Error! Reference source not found.** below.

Figure 41 - Gain vs. V_{DD} @ 200mA

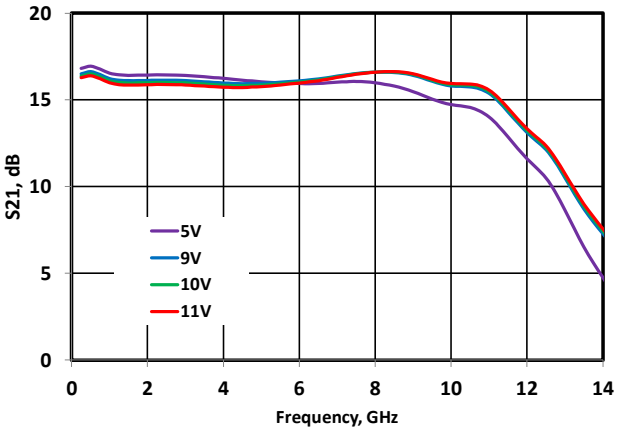


Figure 42 - Gain vs. V_{DD} @ 300mA

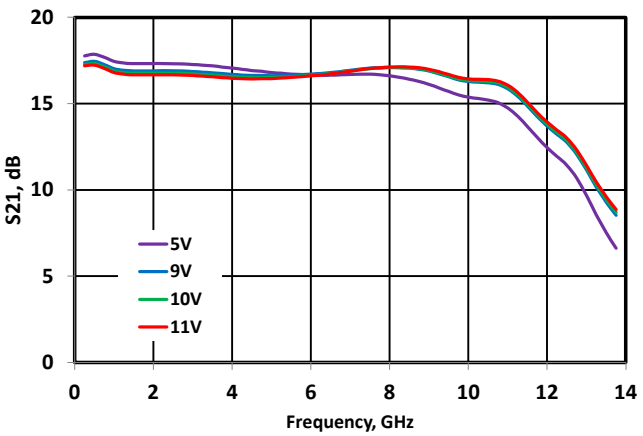


Figure 43 - Gain vs. V_{DD} @ 350mA

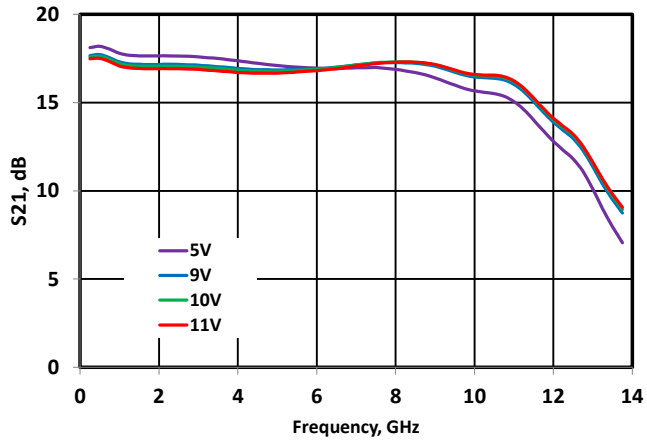


Figure 44 - Gain vs. V_{DD} @ 400mA

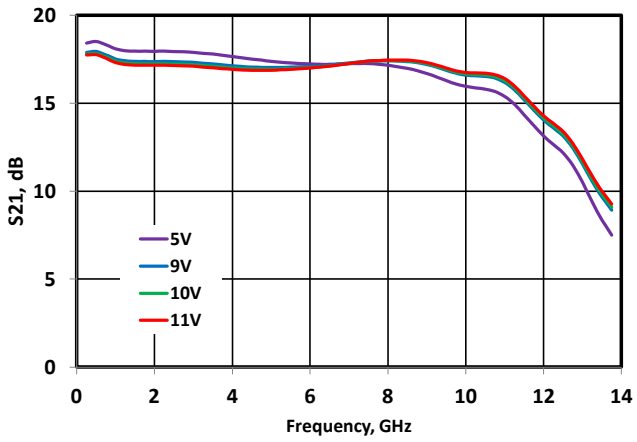


Figure 45 - NF vs. V_{DD} @ 200mA

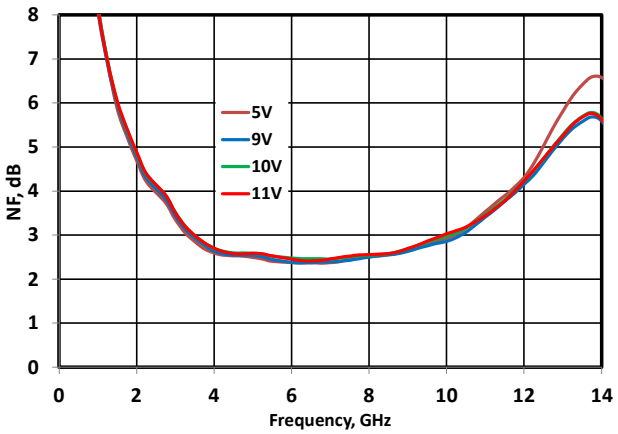


Figure 46 - NF vs. V_{DD} @ 300mA

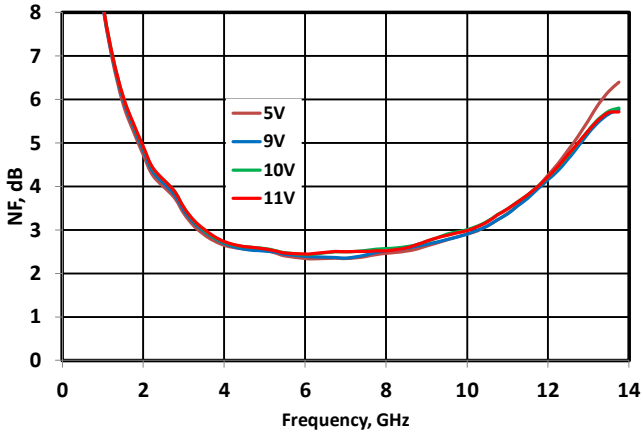


Figure 47 - NF vs. V_{DD} @ 350mA

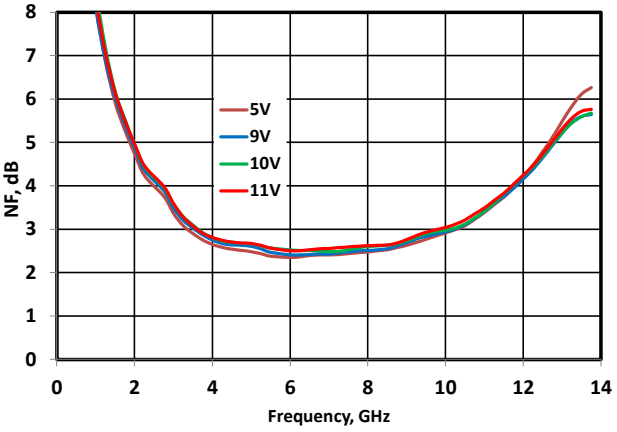


Figure 48 - NF vs. V_{DD} @ 400mA

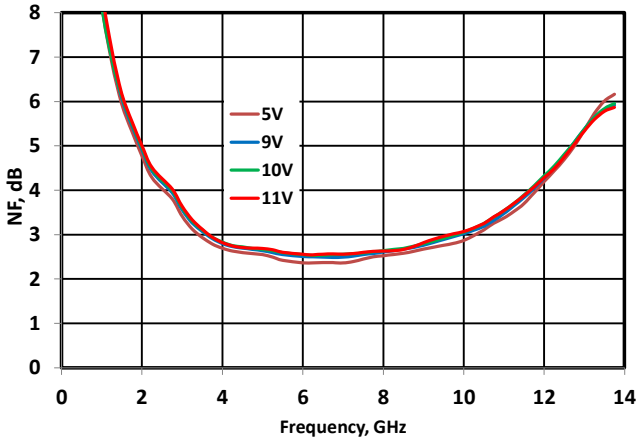


Figure 49 - P1dB vs. V_{DD}/I_{DD}

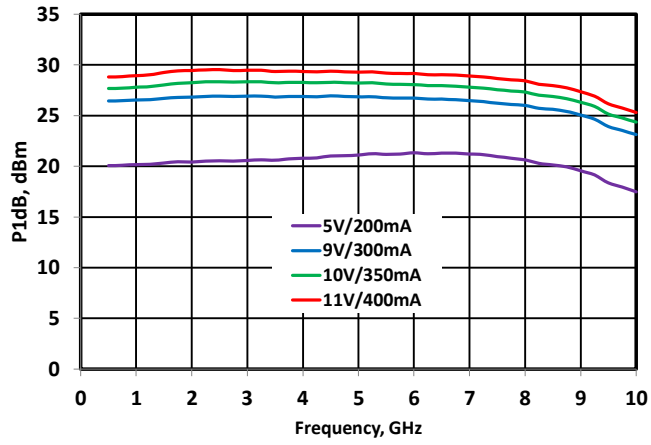


Figure 50 - Psat vs. V_{DD}/I_{DD}

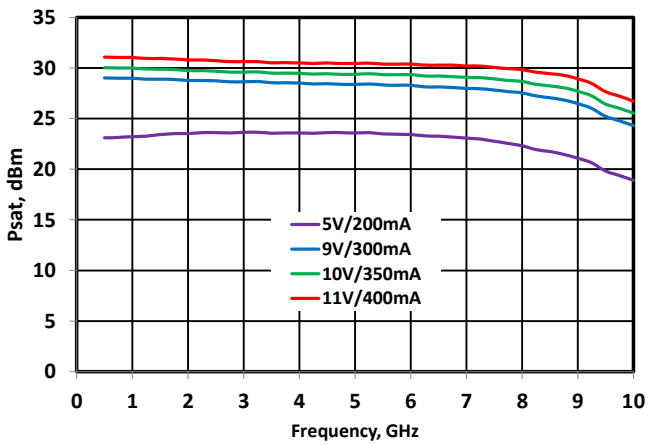


Figure 51 - OIP3 vs. V_{DD}/I_{DD}

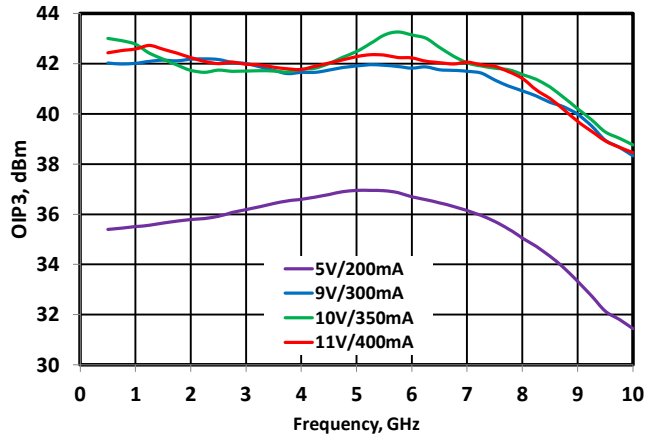


Figure 52 - OIP2 Low at Δ=10MHz vs. V_{DD}/I_{DD}

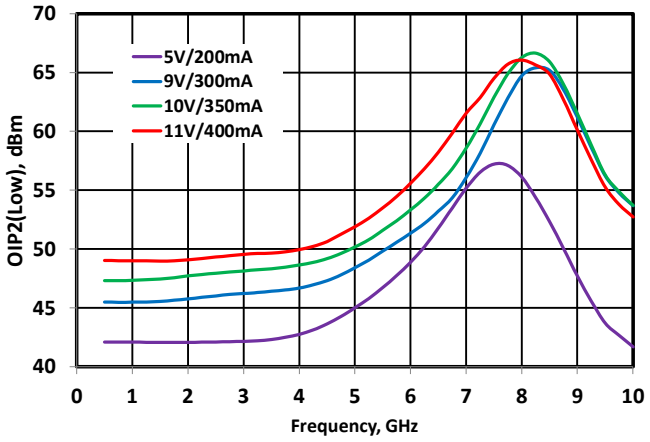
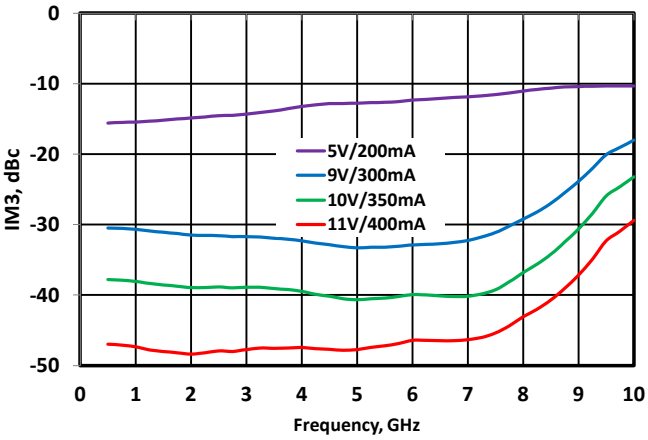


Figure 53 - IM3 vs. V_{DD}/I_{DD}, 20dBm(per tone)



1.1.3 Typical Performances vs. Output Power

The following graphs show the typical performance curves of the MMA053AA device at 25 °C vs. Output Power conditions, measurements performed using application circuit shown on **Error! Reference source not found.** below.

Figure 54 - IM2 vs. Power @ 5V/200mA

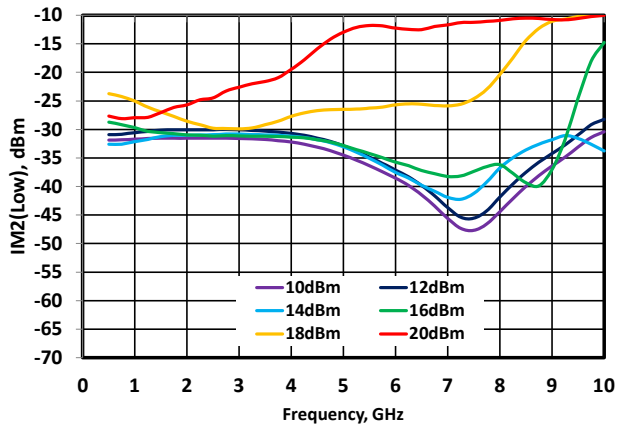


Figure 55 - IM2 vs. Power @ 9V/300mA

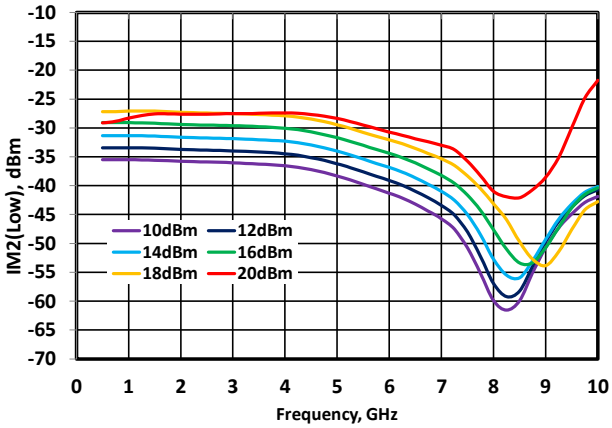


Figure 56 - IM2 vs. Power @ 10V/350mA

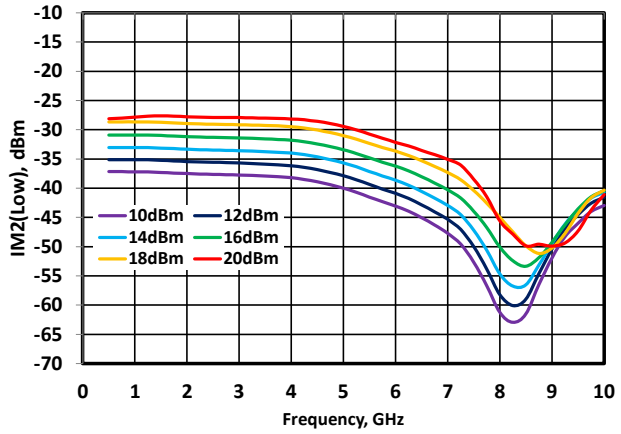


Figure 57 - IM2 vs. Power @ 11V/400mA

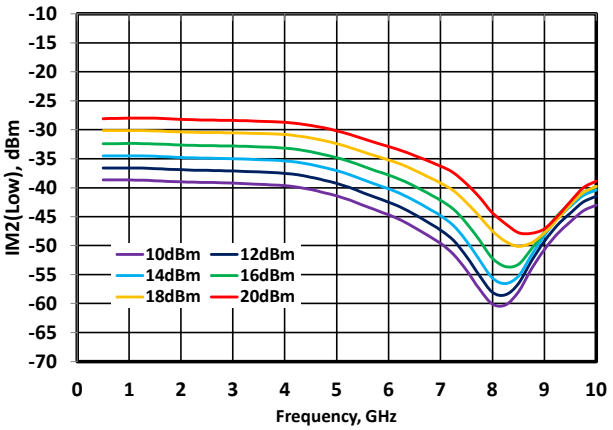


Figure 58 - IM3 vs. Power @ 5V/200mA

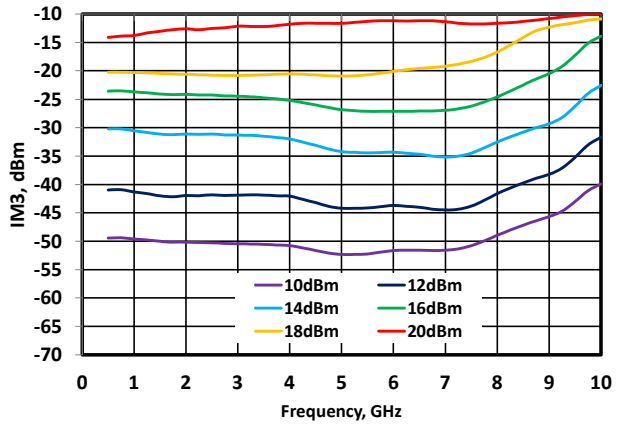


Figure 59 - IM3 vs. Power @ 9V/300mA

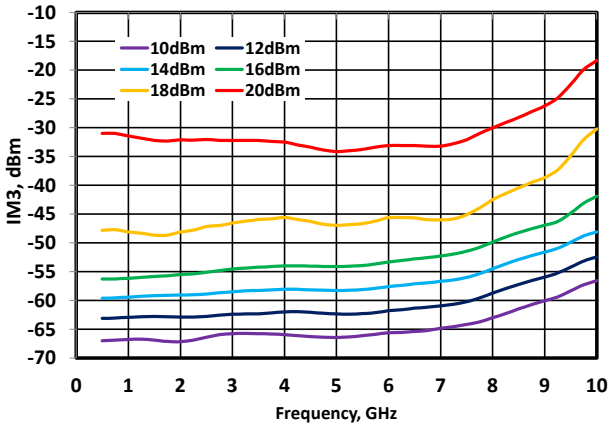


Figure 60 - IM3 vs. Power @ 10V/350mA

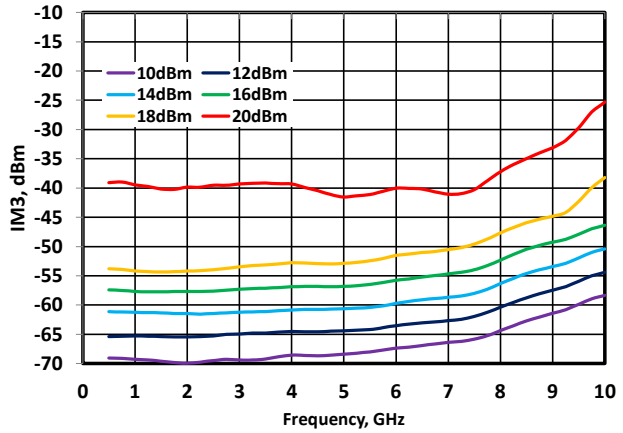


Figure 61 - IM3 vs. Power @ 11V/400mA

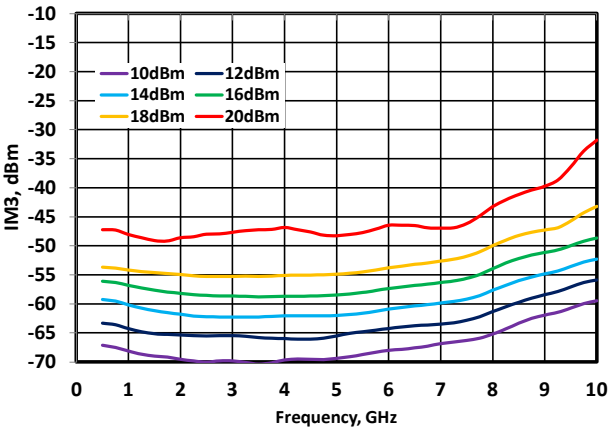


Figure 62 - 2-nd Harmonic vs. Power @ 5V/200mA

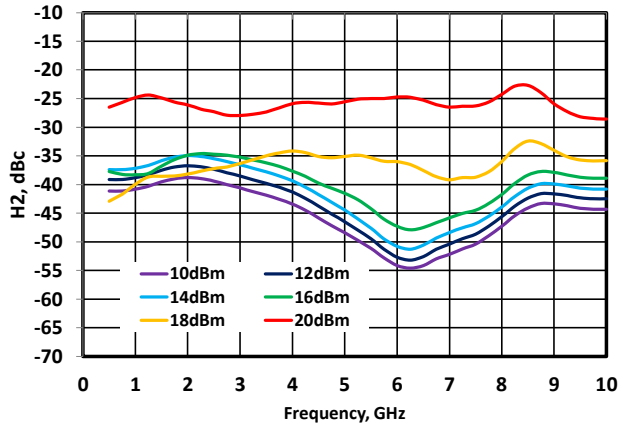


Figure 63 - 2-nd Harmonic vs. Power @ 9V/300mA

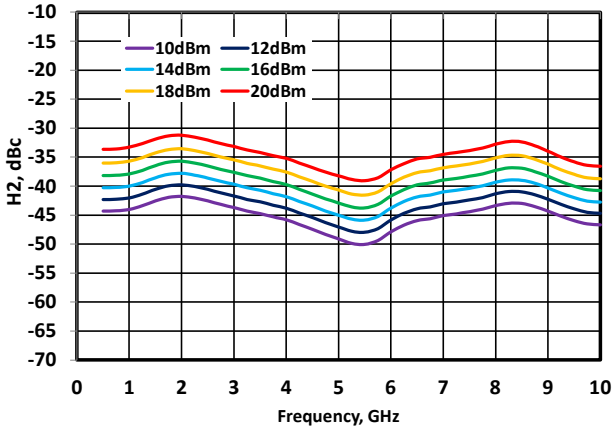


Figure 64 - 2-nd Harmonic vs. Power @ 10V/350mA

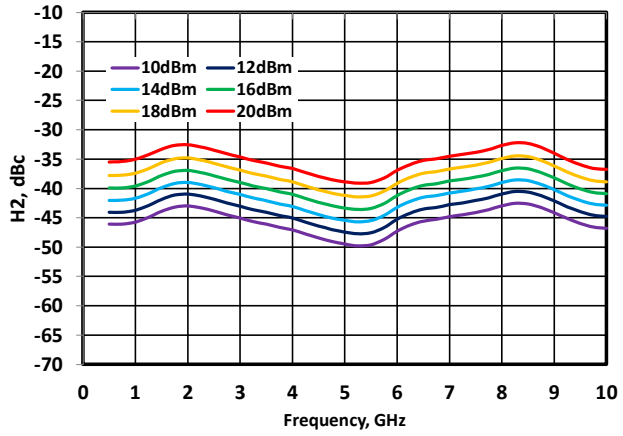


Figure 65 - 2-nd Harmonic vs. Power @ 11V/400mA

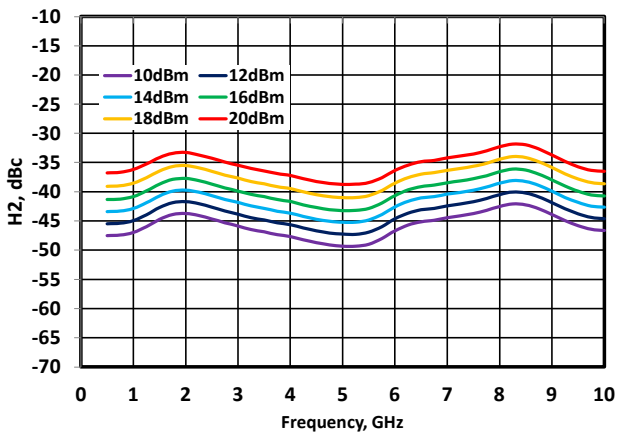
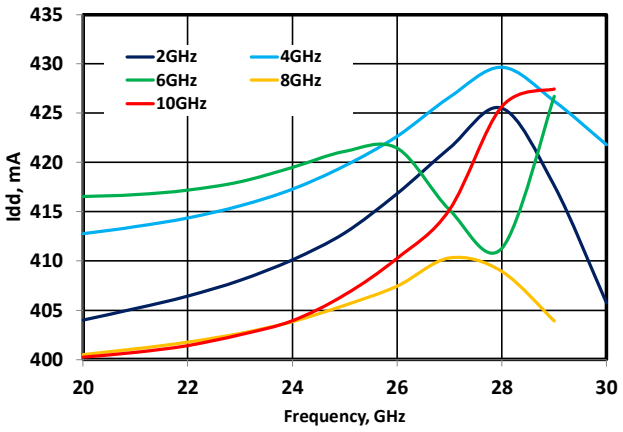


Figure 66 - I_{DD} Current vs. Power, at 11V



2. Package Specifications

The following illustration shows the package outline of the MMA053PP5 device. Dimensions are in millimeters [inches].

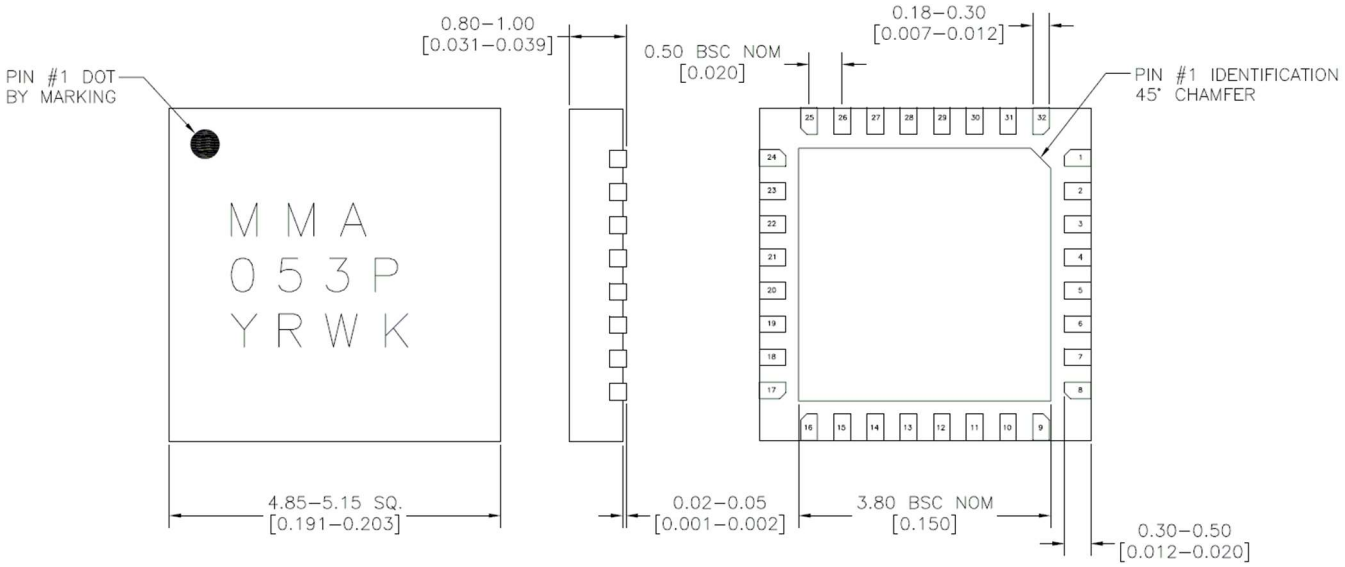


Figure 67 - Die Outline Drawing (mm)

Table 3 - I/O Description

Package	5.0mm X 5.0mm 32L Plastic QFN
Lead Frame	C194 Cu
Plating	Ni/Pd/Au
Package Body Material	RoHS Compliant Low-stress injection molded plastic

Table 4 - I/O Description

Pad Number	Pad Name	Pad Description
5	RF_{IN}	DC-Coupled to Gate 1 and matched to 50 Ohm
21	RF_{OUT}	DC – Coupled to VDD and matched to 50Ω. VDD should be biased through a Bias Tee
13	V_{G1C}	Gate1 Bias. Adjust to achieve required IDD
15, 16	V_{G1A}, V_{G1B}	Low-frequency termination. Connect bypass capacitors per application circuit below.
2	V_{GG}	Low-Frequency termination. Connect bypass capacitor per application circuit below
29, 30	V_{DB} ,V_{DA}	DC linked to VDD internally (not to be used for VDD bias). External Bypass capacitors are required to extend RF match and gain flatness below 2GHz
4, 6, 20, 22, Middle Pad	Ground	Connect to ground per recommended layout
1, 3, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19, 23, 24, 25, 26, 27, 28, 31, 32	N/C	These pins are not connected internally, but they may be connected to external RF/DC Ground on PCB.

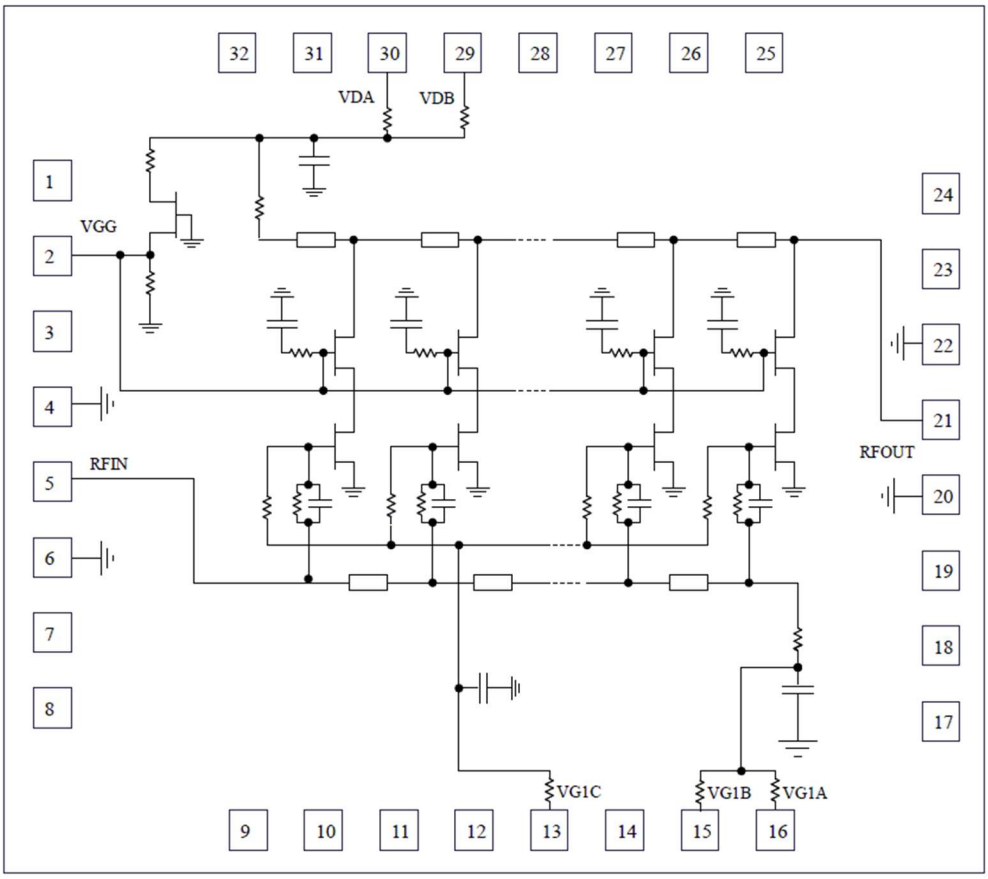


Figure 68 - Amplifier Functional Schematic

3. Application Ciruits: Eval PCB

The following illustration shows the application circuit of the MMA053PP5E device. Note that there is no internal DC blocking capacitor on the input or the output, and a bias tee must be used on pin # 21 for biasing VDD

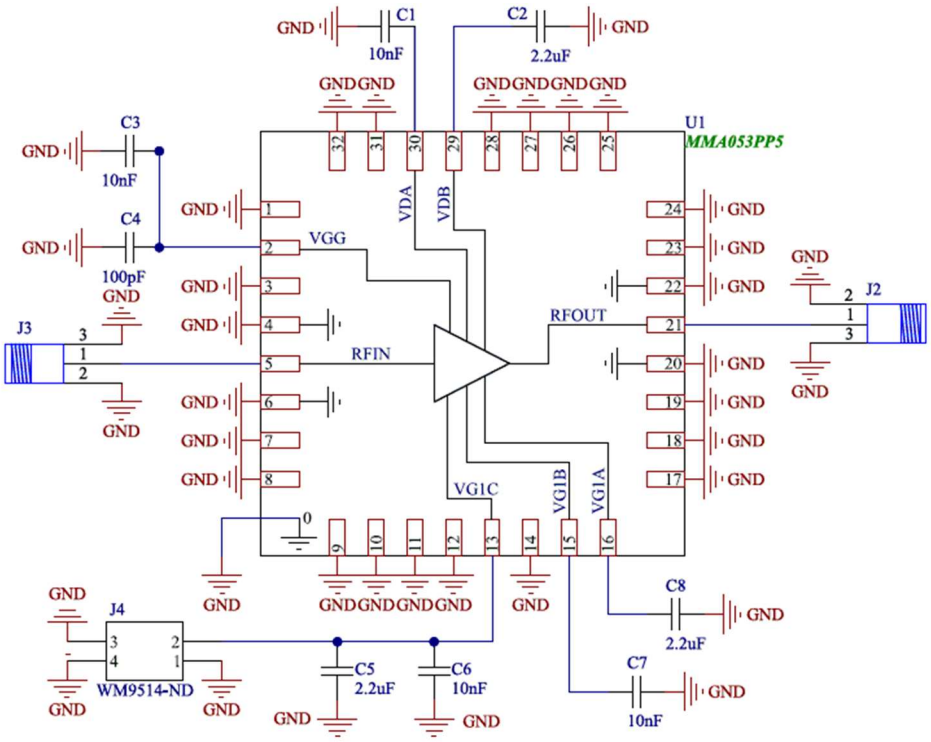


Figure 69 - MMA053PP5 Evaluation PCB

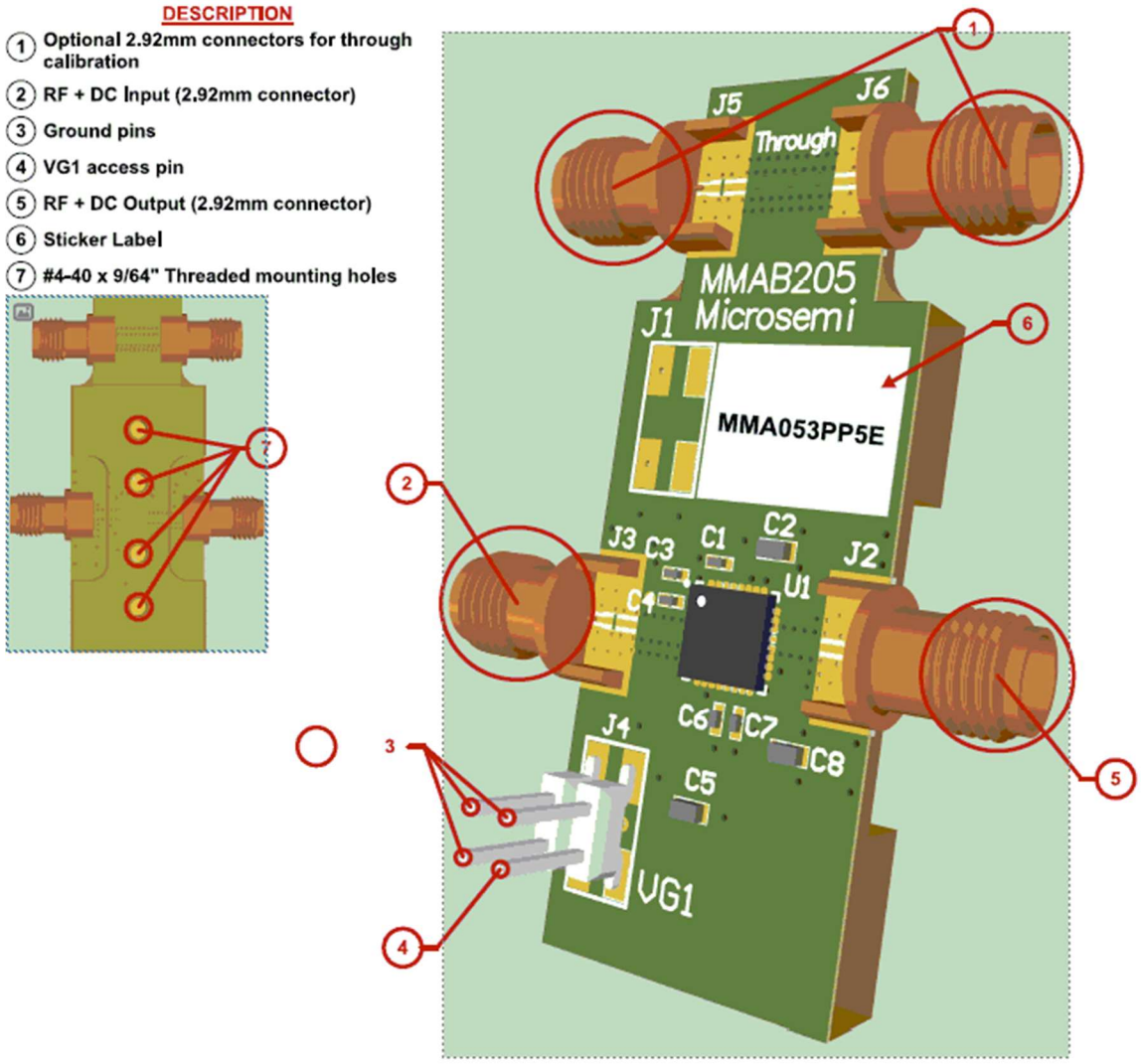


Figure 70 - Evaluation PCB

Table 3.1 Bill of Materials

Item	Designation	Description	Manufacturer Part Number	Qty
1	U1	Power Amplifier QFN 5x5	MMA053PP5	1
2	C1, C3, C6, C7	10000pF +/-10% 50V Ceramic Capacitor X7R 0402	GRM155R71H103KA88D	4
3	C2, C5, C8	2.2uF +/-10% 16V Ceramic Capacitor X5R 0603	0603YD225KAT2A	3
4	C4	100pF +/-5% 50V Ceramic Capacitor C0G, NP0 0402	GRM1555C1H101JA01D	1
5	J2, J3, J5, J6	Connector, 2.92mm Jack PCB Edge Mount 0.12" pin	145-0701-841	4
6	J4	Header, 2-Pin, Dual row	15-91-2040	1

Table 3.2 MMA053PP5E Bias Sequence

Step	Bias Sequence
1	Make sure all DC and RF connections are attached before activating any DC voltage power supplies.
2	Make sure ESD precaution jumper from VG1 to GND on J4 header is removed.
3	DC supply for VDD should be fed through an external bias-T on the RF + DC output port (J2).
	Note: DC supply for VG1 could be attached either through an external bias-T on the RF + DC input port (J3) or through the marked pin on J4..
4	Set VG1 at -1.0V.
5	Set VDD according to your applications plan with current compliance at 600mA.
6	Power supply sequencing should always be VG1 then VDD (VDD is always last on and first off).
7	Adjust VG1 gradually increasing voltage by 0.01V steps until IDD reaches desired application range.
	Note: If external bias-T used on the RF + DC Output (J2) is showing a very low cut-off frequency, precautions should be made to avoid fast changes of the IDD current otherwise DC spikes, caused by transitions, could exceed the VDD maximum level and damage the part.
	⚠ CAUTION Thermal management required. PCB assembly must be mounted on adequate heat-sink via threaded holes found on backside of base-plate (see Description note #7).

4. Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

5. Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA053AA	Die
MMA053PP5	Package Part
MMA053PP5E	Evaluation PCB

5.1 Packing Information

Part Number	Description
MMA053PP5-TR	Tape and Reel

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