Dual, low-offset, low noise operational amplifier

OP227

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace

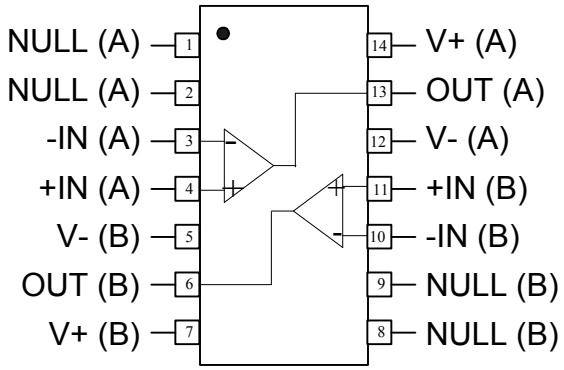
This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete datasheet for commercial product grades can be found at www.analog.com/OP227

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
OP227-903Y	Dual, low-offset, low noise operational amplifier
OP227R903Y	Radiation Tested, Dual, low-offset, low noise operational amplifier
OP227-903M	Dual, low-offset, low noise operational amplifier
OP227R903M	Radiation Tested, Dual, low-offset, low noise operational amplifier

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
Y	GDIP1-T14	14-Lead ceramic dual-in-line package (CERDIP)
M	GDFP1-F14	14-Lead ceramic flat pack (CERPAK)



NOTES:
1. Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B
2. V-(A) and V-(B) are internally connected via substrate resistance.

Figure 1 - Terminal connections.

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3.0 Absolute Maximum Ratings. 1/

Supply voltage (V_{CC}) ..... ±22 V dc
Input voltage range (V_{IN}) ..... ±22 V dc
Output short circuit duration ..... Indefinite
Differential input current 2/ ..... ±25 mA
Differential input voltage range ..... ±0.7 V dc
Lead temperature (soldering, 60 seconds) ..... +300°C
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) 3/ ..... 500 mW

NOTES:

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7 V, the input current should be limited to 25 mA.
3/ For T greater than 106°C, derate linearly at 11.3 mW/°C.

3.1 Thermal Characteristics:

Thermal Resistance, Y (cerdip) Package
Junction-to-Case (Θ_{JC}) = 29°C/W Max
Junction-to-Ambient (Θ_{JA}) = 91°C/W Max
Thermal Resistance, M (cerpak) Package
Junction-to-Case (Θ_{JC}) = 90°C/W Max
Junction-to-Ambient (Θ_{JA}) = 150°C/W Max

4.0 Electrical Table:

Table I

Parameter See notes at end of table	Symbol	Conditions Note 1	Sub-group	Limit Min	Limit Max	Units
Input offset voltage	V_{IO}		1		80	µV
			2, 3		180	
		M, D, L, R	1		160	
Average input offset drift 2/ 4/	TCV_{IO}		1, 2, 3		1.0	µV/°C
Input offset current	I_{IO}		1		±35	nA
			2,3		±50	
		M, D, L, R	1		±120	
Input bias current	I_{IB}		1		±40	
			2, 3		±60	
		M, D, L, R	1		±1200	
Power supply rejection ratio 4/	PSRR	V_S = ±4V to ±18V	1		10	µV/V
		V_S = ±4.5V to ±18V	2, 3		16	
Common mode rejection ratio 4/	CMRR	V_{CM} = ±11V	1	114		dB
		V_{CM} = ±10V	2, 3	108		
Large signal voltage gain	A_{VOL}	V_O = ±10V, R_L = 2KΩ	4	1000		V/mV
			5, 6	600		
		M, D, L, R	4	500		
		V_O = ±10V, R_L = 600Ω	4	800		
Input voltage range 4/	IVR		1	±11		V
			2, 3	±10		
Output voltage swing 4/	V_O	RL = 2KΩ	4	±12		
			5, 6	±11.5		
		RL = 600Ω	4	±10		
Slew rate 2/ 4/	SR	RL = 2KΩ	7	1.7		V/µS
Input noise voltage 4/	e_N	f_O = 1 to 100Hz	7		50	nV_{RMS}
Gain bandwidth product 2/ 4/	GBW	f = 100kHz	7	5.0		MHz
Input offset voltage match 4/	V_{OS}		1		80	µV
			2, 3		180	
Average non-inverting bias current 4/	I_B+	3/	1		±40	nA
			2, 3		±60	
Non-inverting offset current 4/	$I_{OS}+$	$I_{OS}+ = I_B+A - I_B+B$	1		±60	
			2, 3		±90	
Inverting offset current 4/	$I_{OS}-$	$I_{OS}- = I_B-A - I_B-B$	1		±60	
			2, 3		±90	

TABLE I NOTES:

1/ V_S = ±15V, unless otherwise specified

2/ Guaranteed but not tested.

3/ $IB+ = \frac{(I_B + A) + (I_B + B)}{2}$

4/ Not tested post irradiation.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6 1/ 2/
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Delta's excluded from PDA.
2/ See Table III for delta parameters. See table I for conditions.

4.2 Table III. Burn-in/Life Test delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	GROUP C ENDPOINT	DELTA LIMIT	UNITS
VOS	±80	±180	±100	µV
±I_B	±40	±50	±10	nA

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	July 18, 2000
B	Update web address	Feb. 18, 2002
C	Add note 2 to TCVIO, Guaranteed if not tested, ref SMD 86887	Nov. 22, 2002
D	Update web address. Add note 4 to indicate parameters not test post irradiation	May 13, 2003
E	Delete burn-in and radiation bias circuits	Aug. 5, 2003
F	Add OP227-903M & OP227R903M versions	Jul. 29, 2004
G	Update header/footer and add to 1.0 Scope description.	Feb. 25, 2008