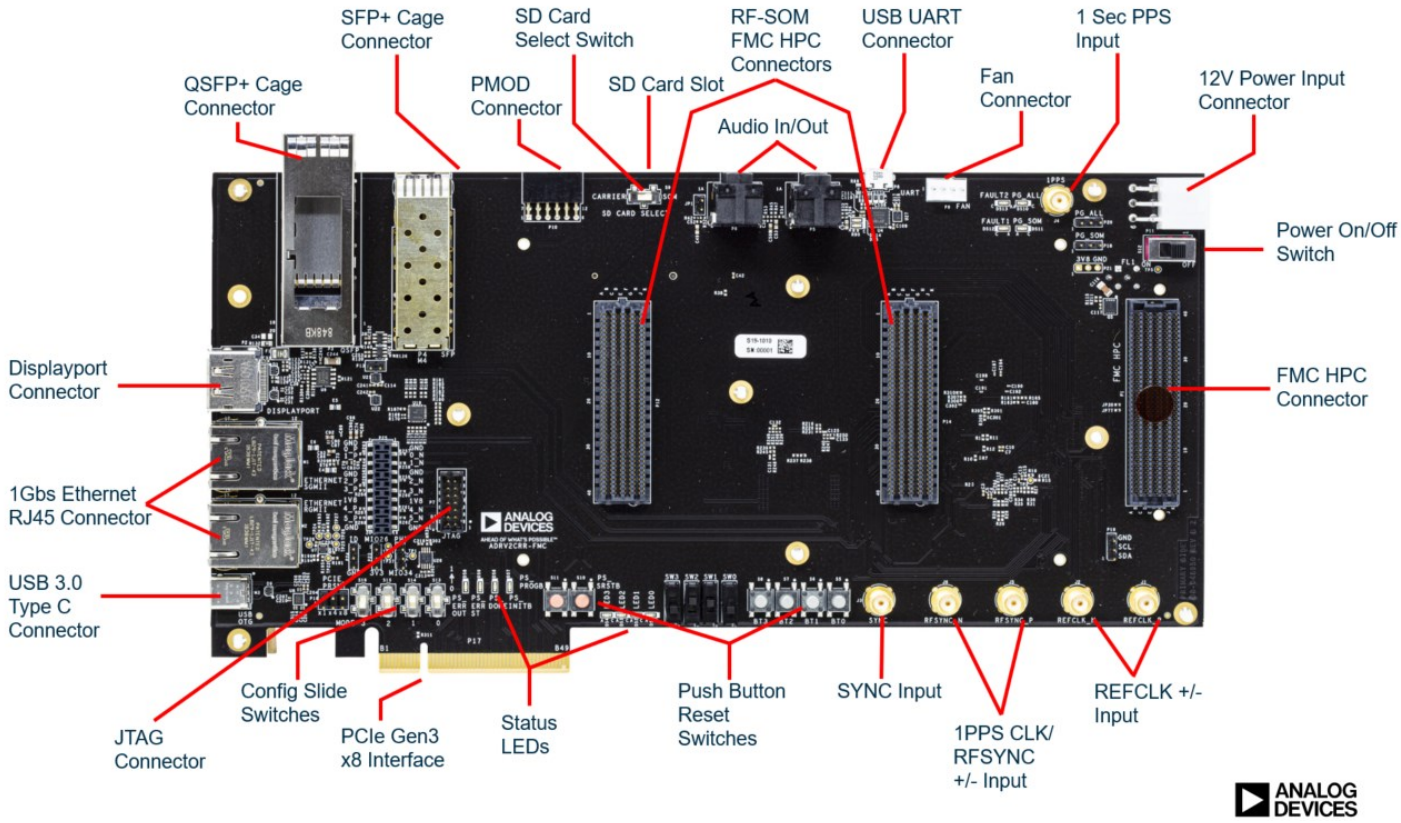
This version (06 Mar 2020 15:33) was ***approved*** by BrianOL.
The Previously approved version (12 Dec 2019 16:25) is available.

ADRV2CRR-FMC Carrier Board Hardware Overview



The ADRV2CRR-FMC is the carrier board to allow users evaluate the functionality of the ADRV9009-ZU11EG RF-SOM. It contains common high speed I/O ports to give flexibility in what connectivity option the user needs. It comes with a power supply that powers up the full system, heatsink that the user fits to the RFSOM heat spreader plate and necessary cables and adapters to get up and running.

Information on getting started and links to access the system software provided is contained on the main RF-SOM Wiki-page.

The following table outlines levels of functionality provided in software for the I/O interfaces on the carrier board.

Interface	Description	Provided by ADI
USB 3.0	USB3 Modes supported: - OTG - Auto detection for Device and Host Mode	USB OTG status Tested with Linux kernel v4.19. The conclusion is that USB is stable and transition from Device mode to Host mode and viceversa are performed correctly. Also USB3 super-speed is detected every time in both device and host mode if a USB3 SS compatible cable is used. It still remains one problem but that is related to the way IIOD is started with the init script from here: https://github.com/analogdevicesinc/linux_image_ADI-scripts/blob/master/iiod_usbd.init The problem appears when the board is booted with USB OTG HOST adapter connected. The IIOD init script won't find the required udc folder in sysfs and will start IIOD without USB context and without creating the Generic USB IIOD gadget. To recover from this problem when device mode is required command "/etc/init.d/iiod restart" should be executed.
PCIe	PCIe tests performed: Production loopback test using xcvrlb ip core clocked at 100MHz ref clock from pcie loopback	ghdl\talise_som: link test using Xilinx PCI Express DMA ip core integrated in the project
SFP+	Tests performed: - Validation was initially performed with IBERT with 12.5 gbps line rate and 312.5 MHz reference clock. The production test uses the axi_xcvrlb and SFP+ / QSFP+ loopbacks which also feature I2C. - production: loopback test using xcvrlb ip core clocked at 312.5MHz ref clock from fmcp loopback - talise_som connected to ubuntu PC with intel sfp+ network adapter; obtained ~1.5 gbps transfer speed	Based on a xilinx example project the xilinx 10g/25g ethernet IP was connected to zynqmp. Together with linux the board was connected via SFP+ (fiber optics) to a ZCU102 with a similar project and then to a linux PC with an intel 10g NIC. A link was established, IP was assigned. In both cases IPERF revealed a ~1.5 gbps data rate. A demo project based on the ADRV9009 was created and is currently waiting to be validated by software.
QSFP+	Tests Perfromed: - Validation was initially performed with IBERT with 12.5 gbps line rate and 312.5 MHz reference clock. The production test uses the axi_xcvrlb and SFP+ / QSFP+ loopbacks which also feature I2C.	Currently there is no software support from Xilinx for 40g/50g ethernet. A Xilinx IP example project was used to simulate the design and then using ILA. After connecting to a linux PC with an Intel 40g NIC the board obtains a link to the PC and communication is established. Wireshark indicates ~1.1 gbps data rate. The data rate may not be relevant since the data transferred was raw (not organized into packets).

The Footprint is located here:

- Compressed 3D Model .DXF file
- Compressed 3D Model .STP file

ADRV2CRR-FMC Hardware

Revision Options

These are X-GRADE options.

- Rev A Schematics
- Rev B Schematics
- Rev C Schematics
- Rev B BOM
- Rev C BOM
- Rev B/C BRD File

Link to Main Page for ADRV9009-ZU11EG