USER GUIDE

UG487: Si86SLxx-EVB User Guide

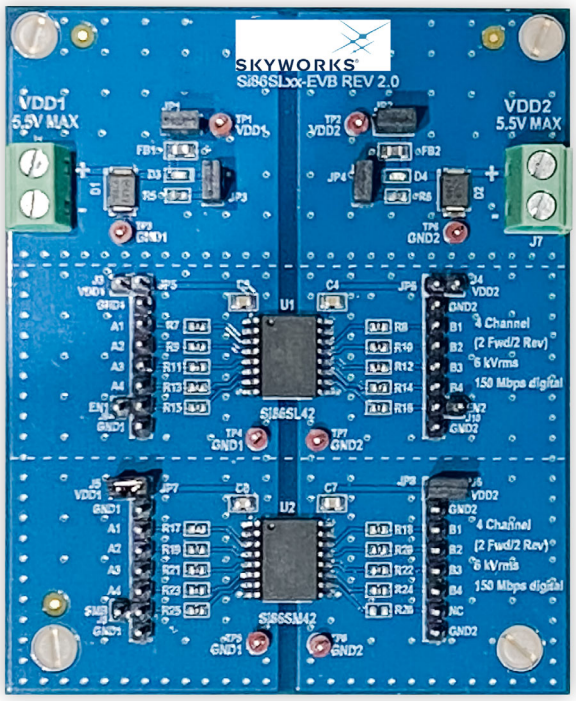
Description

The Si86SLxx-EVB evaluation board allows designers to evaluate Skyworks family of CMOS ultra-low-power isolators, specifically the low-power mode and sleep mode offerings. These isolators are CMOS devices employing RF coupler technology to transmit digital information across an isolation barrier. These products are based on Skyworks' proprietary RF isolation technology, with up to 6.0 kVrms isolation rating. They offer shorter propagation delays, lower power consumption, improved noise immunity, less PCB area, and more stable operation with temperature and age versus optocouplers.

These devices include up to six isolated channels in various forward and reverse configurations, permitting bidirectional data transmission up to 150 Mbps. For the sleep mode devices, an external pin can shut down the active circuits to greatly reduce quiescent current. For more information, refer to the respective family data sheets.

Key Features

- Low Power and Sleep Mode isolators
- Test setup
- Demo tests
- Schematic
- Layout
- Bill of Materials



1. Required Equipment

- Si86SLxx-EVB Rev 2.0
- Two power supplies that support 2.25 to 5.5 V
- Two DMMs in current mode
- 0 V to +5.5 V signal source, up to 150 Mbps or 75 MHz capable, 50% duty cycle (the standard isolator devices can toggle at up to 150 Mbps rate; the signal source/oscillator need not be that fast.)
- Oscilloscope
- Various cables and probes

2. Test Setup

The board comes with jumpers applied to JP3 and JP4, which will allow LEDs D3 and D4 to illuminate indicating that power is active at J1 and J2.

Adjust the two power supplies to 5 V out. Disable the outputs or turn them off.

Connect the power supply low outputs together. This is your system ground. This ground is common because you will use an oscilloscope with probe ground leads which are common. The two supply grounds may be separated if you have separate oscilloscopes for the left and right sides of the EVB.

Connect one power supply low output to GND1 at J1 pin 2, and the power supply high output to a DMM current input. Connect the DMM current output to VDD1 of the EVB, at J1 pin 1.

Connect the other power supply low output to GND2 at J2 pin 1, and the power supply high output to the other DMM current input. Connect the DMM current output to VDD2 of the EVB, at J2 pin 2.

Enable or turn on the power supplies. You may verify 5 V outputs at TP1 and TP2. Verify that LEDs D3 and D4 both turn on. You may remove the jumpers at JP3 and JP4 to disable the LEDs if you want to measure VDD current in the devices.

Set up the signal source with the low side to system ground, or to the input side ground depending on which side has the input being stimulated. Ground test points are provided on each side of the board for this purpose.

Each device section has headers for VDD1 and VDD2 connection to the board supply. Jumpers are provided for these headers to energize one device at a time.

2.1. Digital Isolator Considerations

The Si86SLxx-EVB evaluation board (see Figure 1) provides a means of evaluating the Si86SL42 with low-power mode and Si86SM42 with sleep-mode digital isolator devices. After power (2.25 to 5.5 V) has been supplied to the board, connect a digital input signal (5.5 Vpeak max, with desired clock frequency up to 150 Mbps) to the desired input channel. To view the isolated channel's data transmission, connect a scope probe to the output channel of interest. There are various inputs and outputs on either side of the board depending on the device one chooses to evaluate, as indicated by the silk screen. The board can be used to measure propagation delay, pulse-width distortion, channel-channel matching, pulse-width skew, and various other parameters.

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the values of the on-chip series termination resistor and the channel resistance of the output driver FET. When driving loads where transmission line effects are a factor, output pins should be terminated with 50 Ω controlled impedance PCB traces.

The figure below illustrates the Si86SL42 transmitting a 500 kHz (3 Vpeak) signal through the Si86SL42. VDD1 and VDD2 are powered with 3 V. Channel 1 illustrates the input, and Channel 2 illustrates the output.

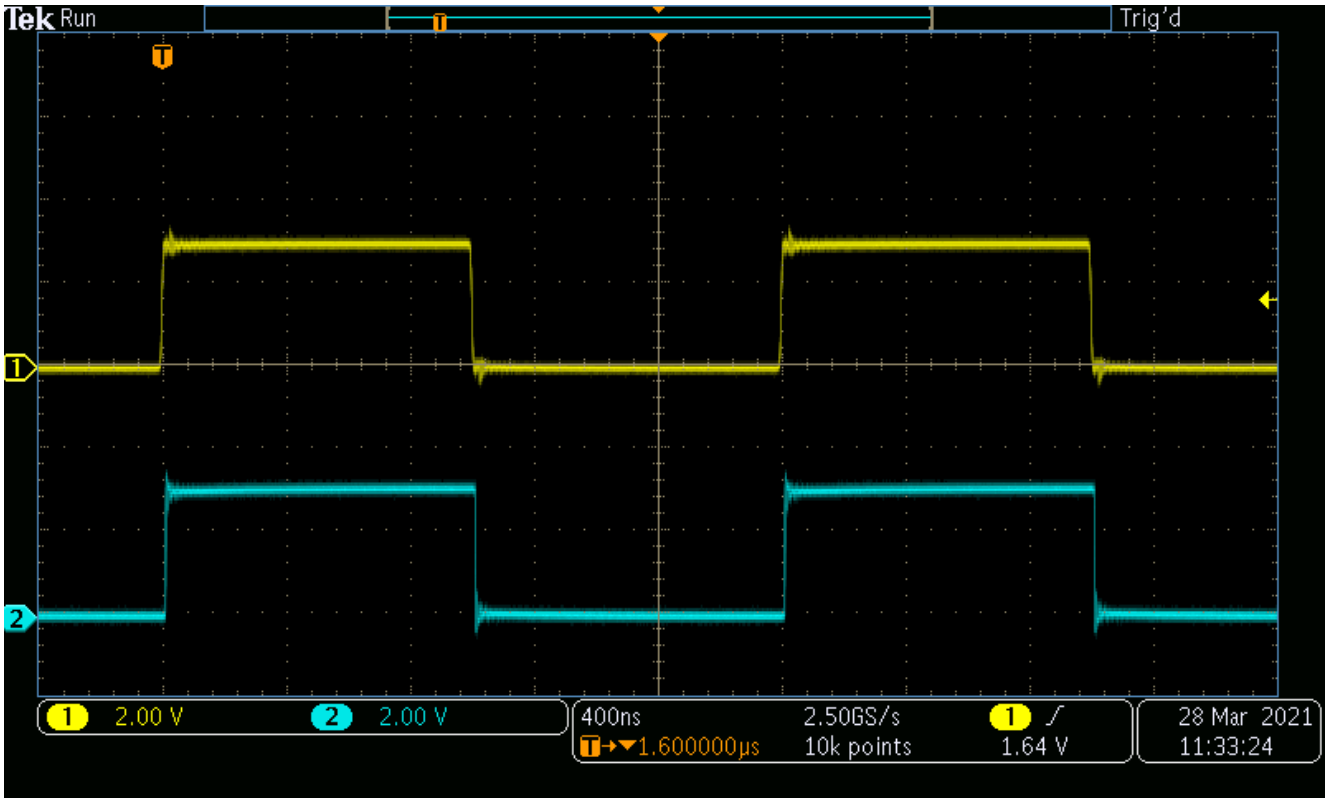


Figure 1. Si86SL42 Transmitting a 500 kHz (3 Vpeak) Signal through the Si86SL42

3. Si86SL42BE-IS2 (U1 Device) Setup and Demo Test

The Si86SL42BE-IS2 is a two forward channel and two reverse channel digital low power isolator device with two enable pins in a 16-pin wide-body small outline package. EN1/EN2 enable pins control the state of all outputs on the same side as the pin. The Si86SLx devices are optimized for lower-power operation compared to the Si86S6x options. Typically, they consume 0.25 mA/ch less current in quiescent mode. The pinouts are no different than the Si86S6x options. This mode is always turned for these devices. The architecture is tuned in favor of power savings rather than higher performance in terms of timing specifications.

The board can be used to measure propagation delay, pulse-width distortion, channel-channel matching, pulse-width skew, and various other parameters.

Apply jumpers to J3 and J4 to connect the VDD supplies to the device. Verify an increase in VDDx current in both current meters.

When the EN pins on either side are high or left unconnected, the channels are active. To disable one side or the other, apply a jumper at J9 or J10.

To test the channels, apply a signal at each input separately or together. Channels operate independently and simultaneously. The output states should reflect their respective inputs.

Table 1. U1 Channels

Input	Output
A1 (left side)	B1 (right side)
A2 (left side)	B2 (right side)
B3 (right side)	A3 (left side)
B4 (right side)	A4 (left side)

4. Si86SM42BE-IS2 (U2 Device) Setup and Demo Test

The Si86SM42BE-IS2 is a two forward channel and two reverse channel digital low power isolator device with one sleep mode pin in a 16-pin wide-body small outline package. The sleep mode feature is very useful for power savings without compromising on performance. Instead of trading off data rate or CMTI performance for power savings, these options provide an SMB pin that can be used to put the device in sleep mode when not in operation. For example, the Si86SM42 is a four-channel device with two forward channels and two reverse channels.
The left, “A”, or main side of the device has an SMB pin which when driven high (or left unconnected) enables the device but when driven low puts the device into sleep mode with 750 µA per side. In this mode, one isolation channel is always active to read the status of the SMB pin and to restart the entire device when SMB is driven high or left open, including the isolated side.

Apply jumpers to J5 and J6 to connect the VDD supplies. Verify an increase in VDDx current in both current meters.

When the SMB pin is high or left unconnected, the channels are active. To disable the channels, apply a jumper at J8.

To test the channels when the device is not in sleep mode, apply a signal at each input separately or together. Channels operate independently and simultaneously. The output states should reflect their respective inputs.

Table 2. U2 Channels

Input	Output
A1 (left side)	B1 (right side)
A2 (left side)	B2 (right side)
B3 (right side)	A3 (left side)
B4 (right side)	A4 (left side)

5. Additional Board Features

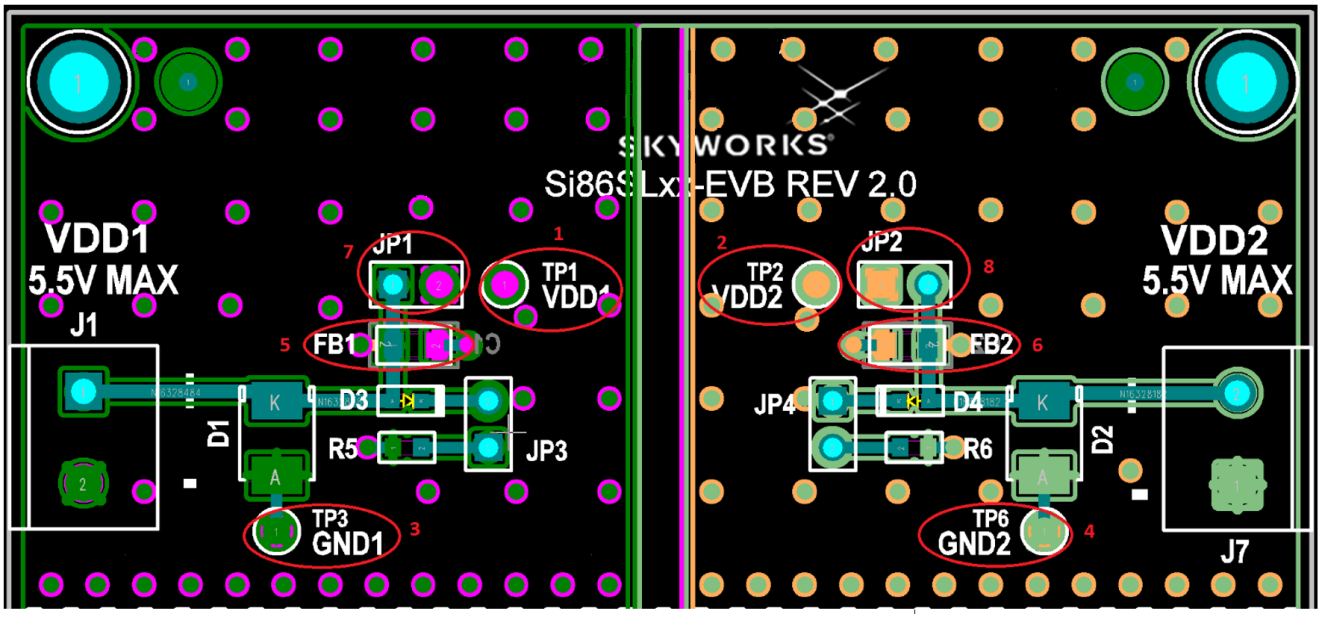


Figure 2. Board Features (Top End of Board)

1. **VDD Attachments:** If you prefer to attach VDD on either side using clip leads instead of stripped wires, you may use the test point, such as TP1 (1) for VDD1, TP3 (3) for GND1, TP2 (2) for VDD2, TP6 (4) for GND2. The indicator LEDs will still illuminate.
2. **Ferrite Beads:** Each VDD path at the top of the board contains a ferrite bead (5, 6). This may be shorted out with a jumper (7, 8), for instance at JP1. Alternatively, the ferrite bead may be replaced with a current sensing resistor, and its voltage measured across the header. A third use of the header would be to remove the ferrite bead and use the jumper to route the supply through a current meter and back to the board.
3. **Pin Series Resistors:** Each signal pin has a 0 Ω resistor in series. These may be replaced by a different value to limit input current or to provide termination.

6. Schematics

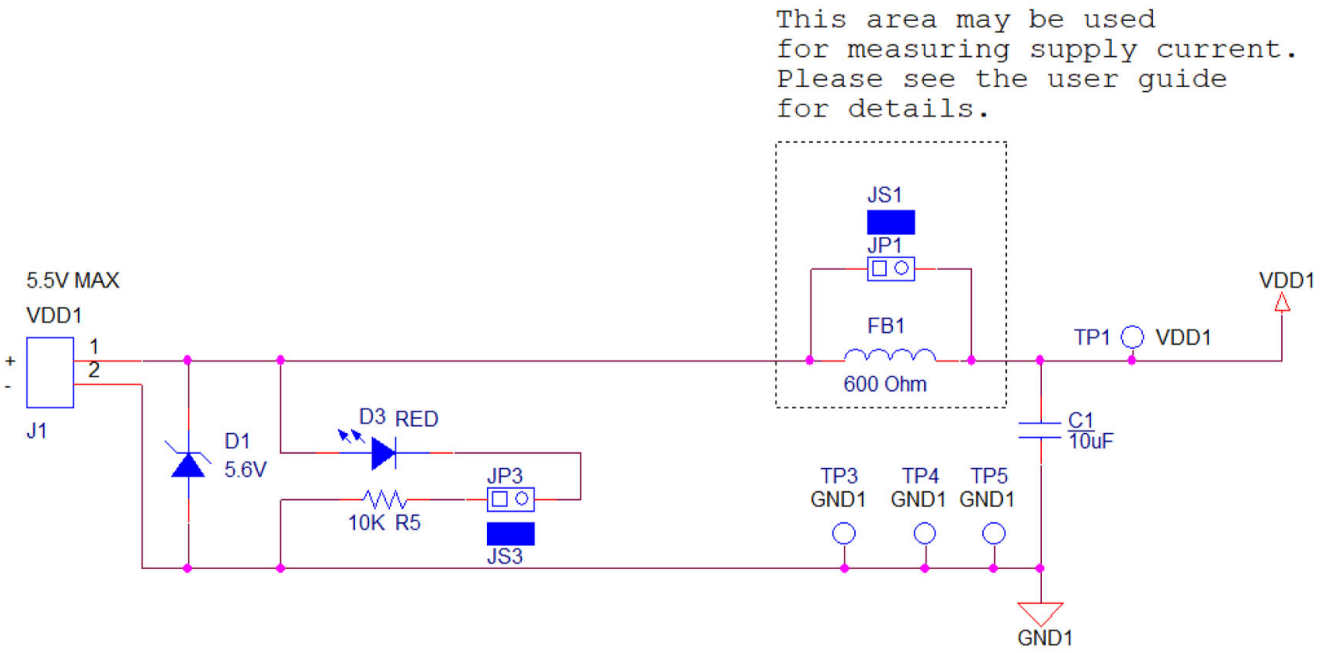


Figure 3. VDD1 Connection

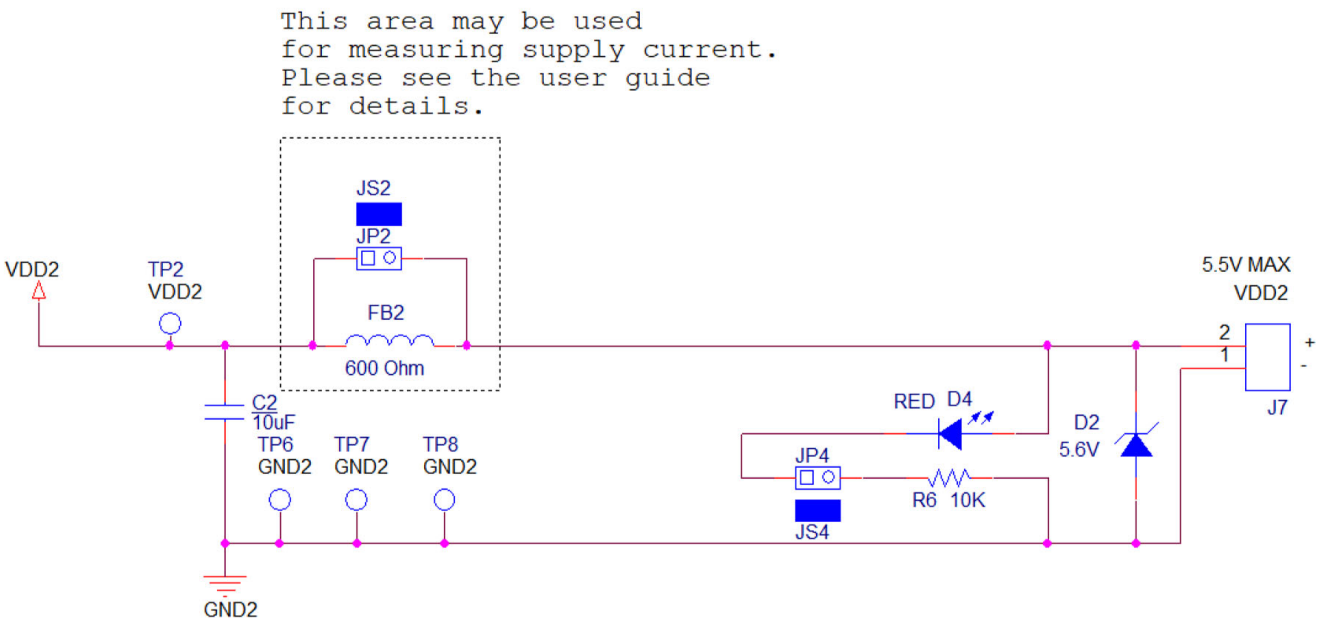


Figure 4. VDD2 Connection

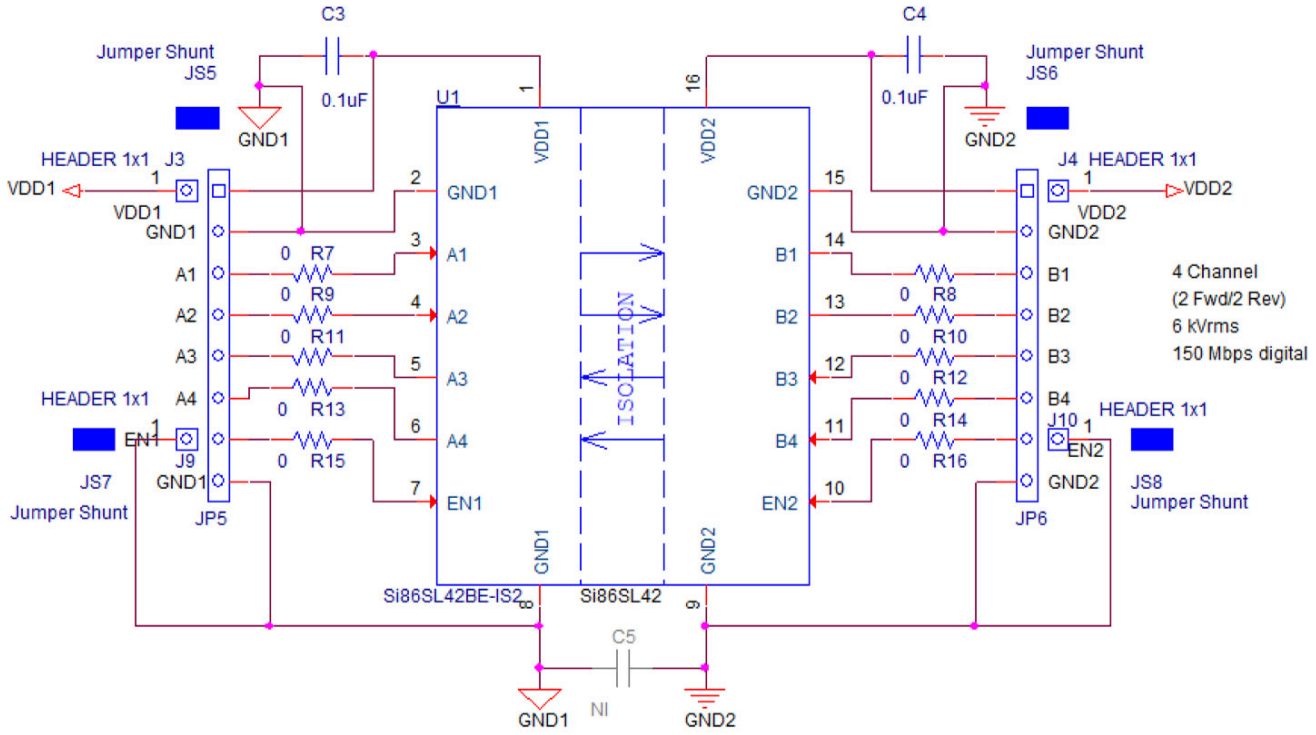


Figure 5. U1 Circuit

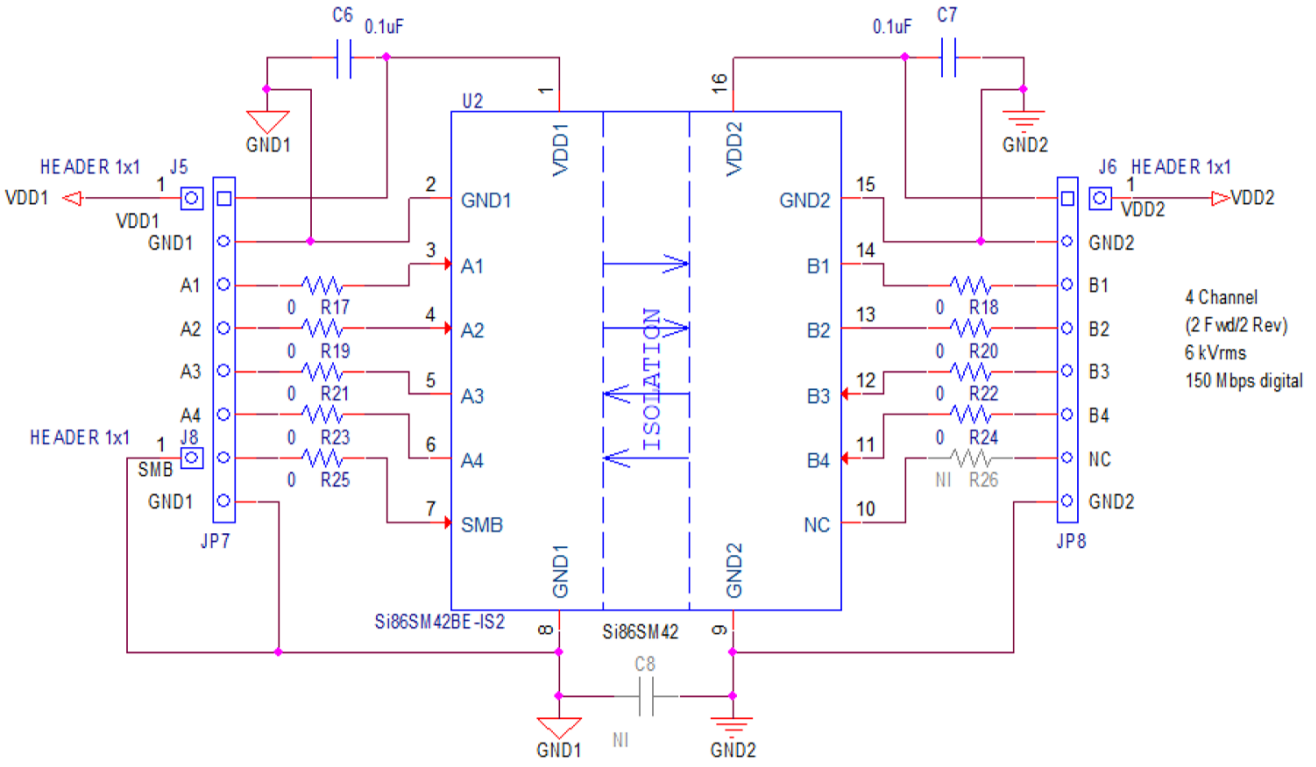


Figure 6. U2 Circuit

7. Layout

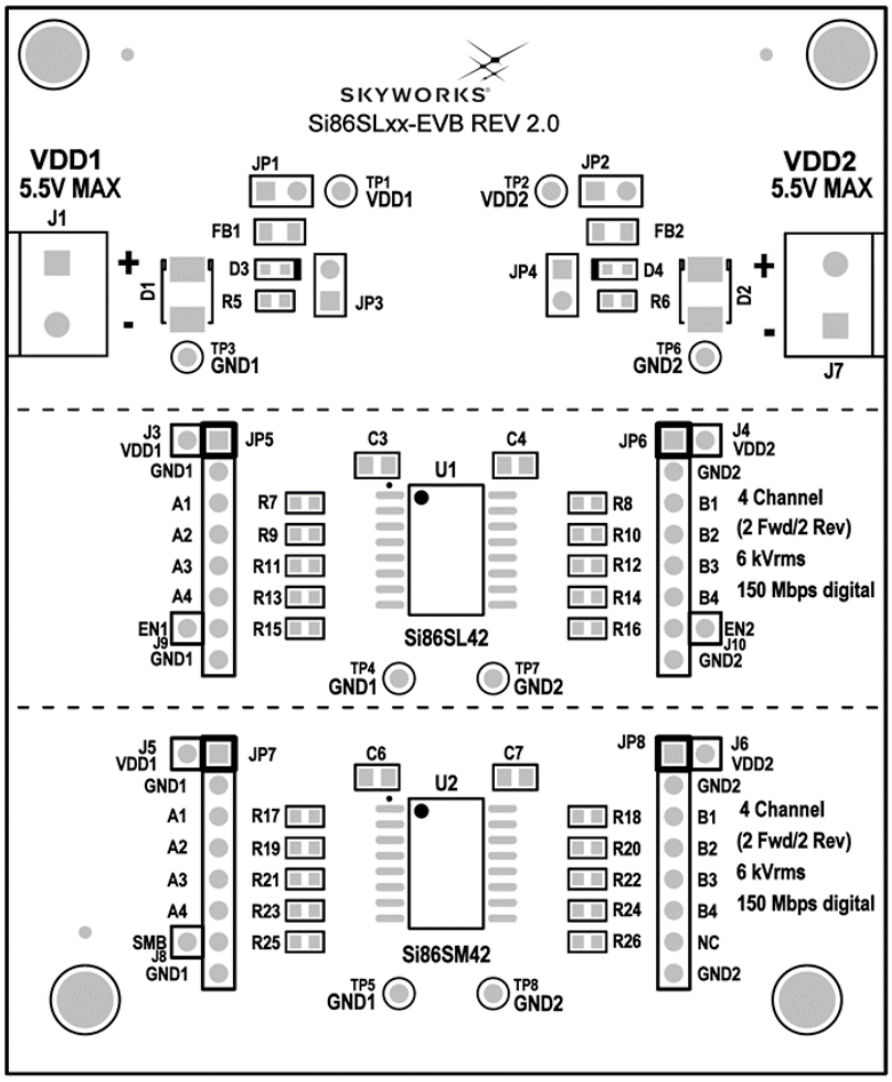


Figure 7. Primary Silkscreen

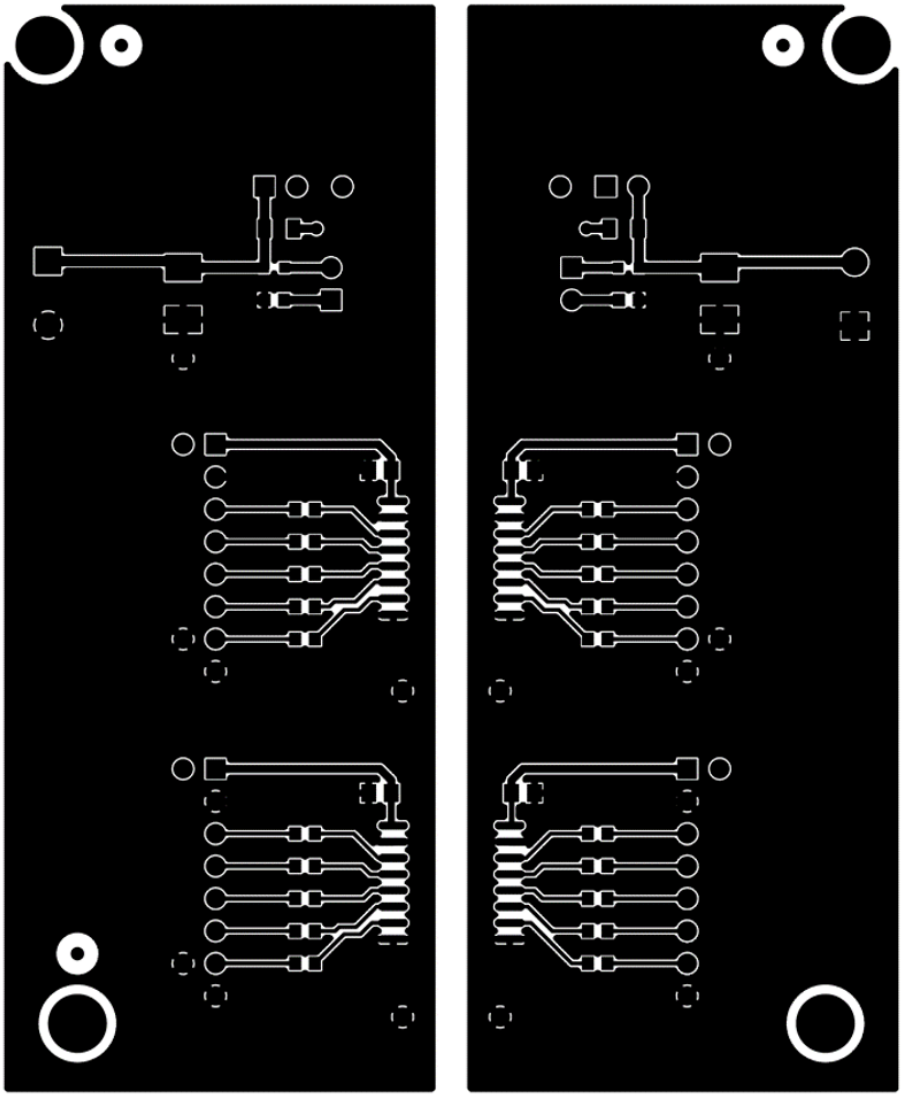


Figure 8. Top Interconnect Layer

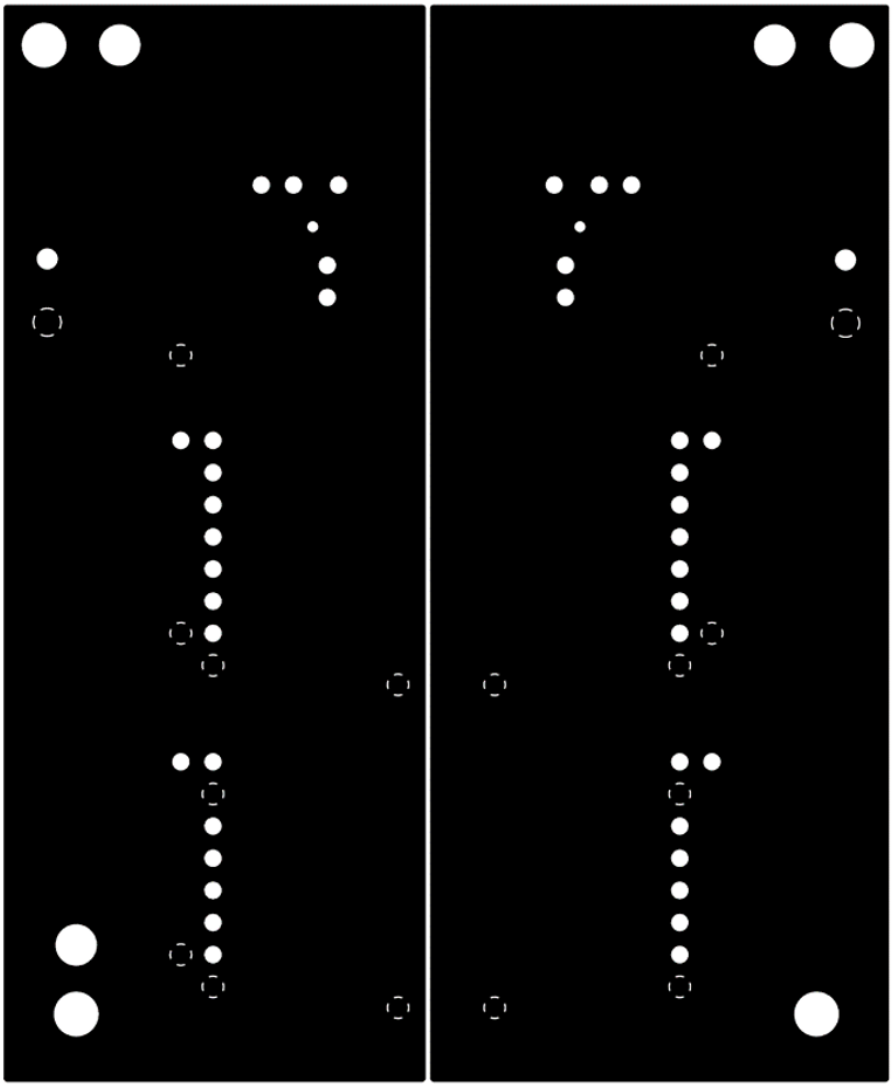


Figure 9. Ground Layer (2nd)

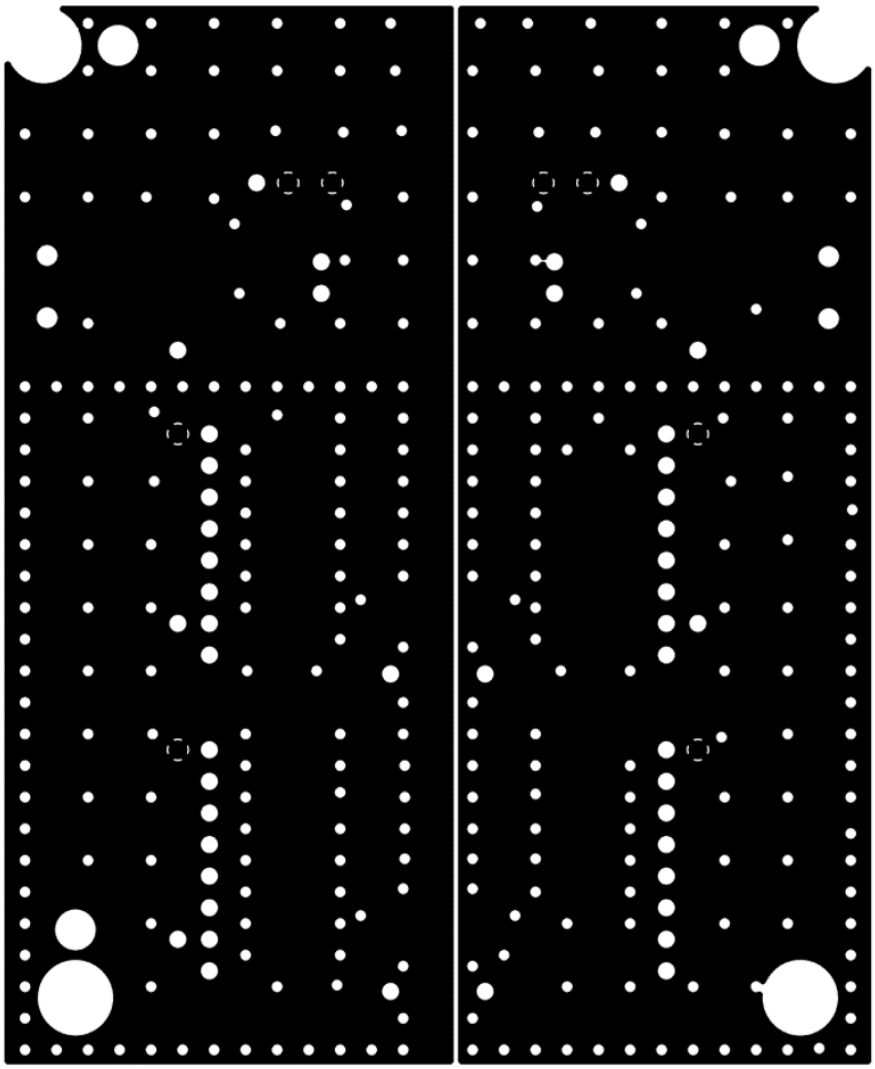


Figure 10. Power Layer (3rd)

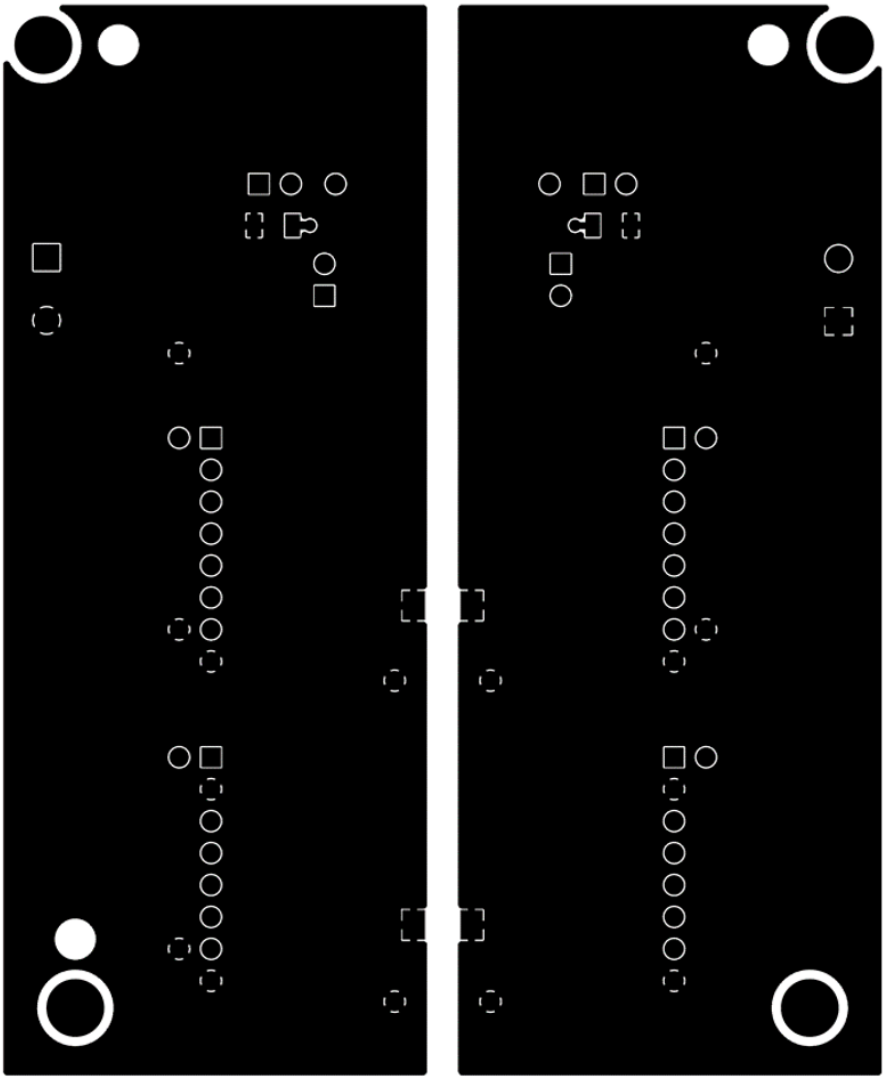


Figure 11. Bottom Side Interconnect

8. Bill of Materials

Table 3. Si86SLxx-EVB Bill of Materials

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr	Mfr PN
2	C1, C2	10 µF		10 V	±10%	X7R	C1206	Venkel	C1206X7R100-106K
4	C3, C4, C6, C7	0.1 µF		16 V	±10%	X7R	C0805	Venkel	C0805X7R160-104K
2	D1, D2	5.6 V	3 W	5.6 V	5%	Zener	DO-214AA	On Semi	1SMB5919BT3
2	D3, D4	Red					LED0603-KA	Lite-On Technology Corp	LTST-C190KRKT
2	FB1, FB2	600 Ω	200 mA			SMT	L0805	Murata	BLM21AG601SN1
4	JP1, JP2, JP3, JP4	Header 1X2				Header	CONN1X2	Samtec	TSW-102-07-T-S
4	JP5 ,JP6, JP7, JP8	Header 1x8				Header	CONN-1X8	Samtec	TSW-108-07-T-S
8	JS1, JS2, JS3, JS4, JS5, JS6, JS7, JS8	Jumper Shunt				Shunt	N/A	Samtec	SNT-100-BK-T
2	J1,J7	CONN TRBLK 2				Term Black	CONN-1X2-TB	Phoenix Contact	1729018
7	J3, J4, J5, J6, J8, J9, J10	Header 1x1				Header	HDR1X1	Samtec	TSW-101-07-T-S
4	MH1, MH2, MH3, MH4	Apr-40				Screw	MH-125NP	Richco Plastic Co.	NSS-4-4-01
1	PCB1	Si86SLxx-EVB Rev 2.0				Bare PCB	N/A	Skyworks Solutions, Inc.	Si86SLxx-EVB REV 2.0
2	R5, R6	10 kΩ	1/10 W		±1%	Thick Film	R0603	Venkel	CR0603-10W-1002F
20	R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26	0	1 A			Thick Film	R0603	Venkel	CR0603-16W-000
4	SO1, SO2, SO3, SO4	Standoff				Standoff		Keystone Electronics	1902D
8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Red				Loop	Testpoint	Kobiconn	151-207-RC
1	U1	Si86SL42BE-IS2	6 kVrms			Isolator	SO16N10.3P1.27	Skyworks Solutions, Inc.	Si86SL42BE-IS2
1	U2	Si86SM42BE-IS2	6 kVrms			Isolator	SO16N10.3P1.27	Skyworks Solutions, Inc.	Si86SM42BE-IS2
Not Installed Components									
2	C5, C8	1000 pF	X2/Y3	250 V	±10%	Y3	C1808	Yageo	SC1808KKX7RTBB102

9. Ordering Guide

Table 4. Ordering Guide

Ordering Part Number (OPN)	Description
Si86SLxx-KIT	Si86SLxx Digital Isolator Evaluation Board Kit