UXN40M7KE Prescaler Evaluation Board

The UXN40M7KE is the evaluation board for the Centellax UXN40M7K 40 GHz Divide-by-1 to 127 programmable integer dividers. (See Figure 1).

Note: Supply voltage must be positive +3.3V.

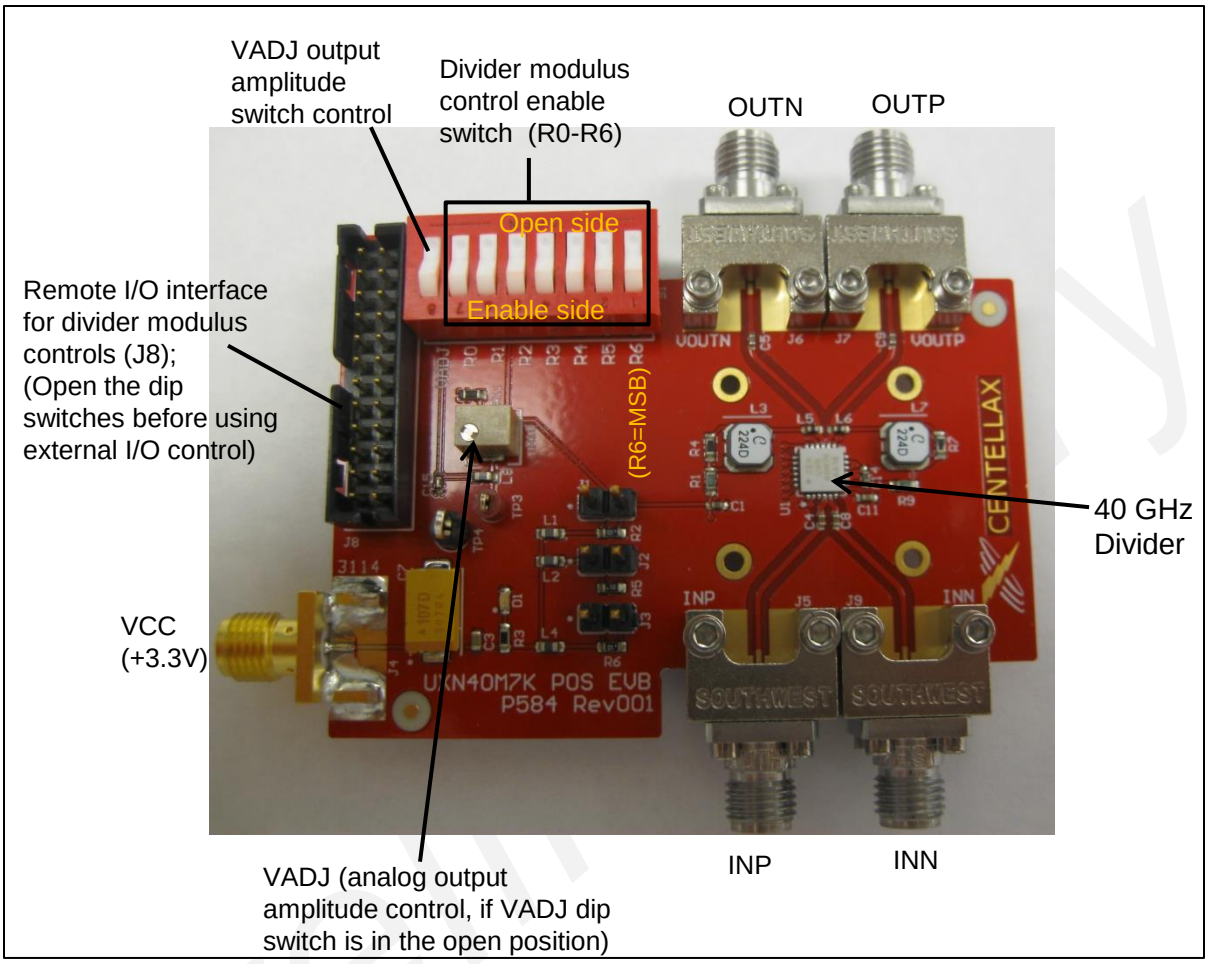


Figure 1: Evaluation board (P584)

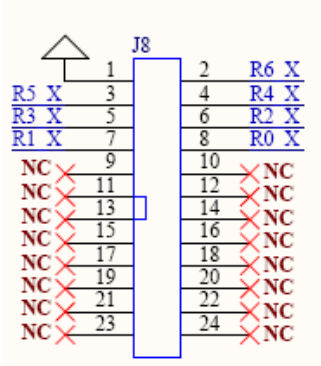


Figure 2: (J8) I/O pin configuration

Turn on Sequence

1. **Please take caution of static damage as the evaluation board and the prescaler device are both sensitive to static discharge.**
2. If RF inputs/outputs are used in single-ended configuration, terminate unused inputs/outputs with 50 ohm loads.
3. Apply a +3.3V supply (VCC) to the evaluation board (J4, SMA (f) connector).
4. Use on-board dip switches (S1) to set the divide ratios. Note all zeros is a default divide by 1.

Switch Settings (S1, Open = 0, Close = 1)	Division Ratio Output
Divider Modulus Control **R6 R5 R4 R3 R2 R1 R0 (R6=MSB)**	
0000001	1
1000000	1/64
1111111	1/127

5. Optional: The divide ratio of the prescaler device can also be programmed through (J8), (24-pin Molex connector interface (mfg pn 87831-2420)), using an external programming device, (see Figure 2). If using an external programming device, set the on-board dip switches (S1: R0-R6) to the open position first before making connection to the external programming device.

   Note: Do not use both divider modulus control interfaces at the same time (i.e., dip switches and external logic control interface through J8 connector).

   Input voltage levels for control lines R0-R6:

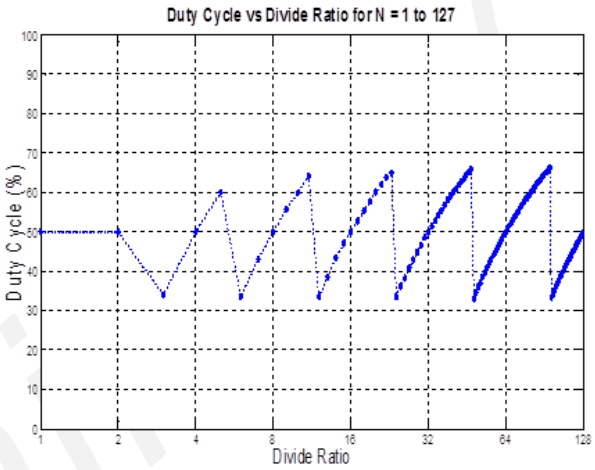
Logic Level	Minimum	Typical	Maximum
1 (High)	VCC-1.3V	VCC	VCC
0 (Low)	VEE	VEE	VEE + 0.8V

6. Apply RF signal at the input (INP/INN, 2.9 mm (f) connectors).
7. Set the “VADJ” toggle switch (part of the S1 dip switch) to the disable position (open). Adjust VADJ potentiometer to control desired output amplitude.
8. Or for maximum output swing, set the dip switch of VADJ to the close position. (I.e., set the VADJ voltage level to the same voltage as VCC). Note: While in a logic 1 on the dip switch of VADJ, the VADJ potentiometer will have no effect on the output swing voltage.

Turn on Sequence (continue)

9. Check the divided RF output signal (VOUTP/VOUTN, 2.9 mm (f) connectors) on a spectrum analyzer or oscilloscope.
10. The output waveform duty cycle vs. divide ratio, and the pin functions are shown in the tables and plot below.
11. Refer to the UXN40M7K datasheet for performance specifications.

Divide Ratio	Pulse Width (Input Cycles)	Duty Cycle (%)
2	1	50
3	1	33
4	2	50
5	3	60
6	2	33
7	3	43
8	4	50
9	5	55
10	6	60
11	7	63
12	4	33
13	5	38
14	6	43
15	7	47
16	8	50



Pin Function		Operational Notes
1 (R1)	Divide Modulus Control	Defaults to logic 0, connect to VCC for logic 1
2 (R0)	Divide Modulus Control (LSB)	Defaults to logic 0, connect to VCC for logic 1
3, 8, 9, 12, 17, (VEE)	RF and DC Ground	0V
4 (INP)	Divider Input	Positive terminal of differential input
5 (INN)	Divider Input	Negative terminal of differential input
6 (VCM)	Common Mode Input	Refer to functional block diagram
7, 10, 11, 13, 16, 19 (VCC)	Positive Supply Voltage	Nominally +3.3 V
14 (OUTP)	Divider Output	Positive terminal of differential output
15 (OUTN)	Divider Output	Negative terminal of differential output
18 (VADJ)	Output Amplitude Control	Tie to VCC for max swing.
20 (R6)	Divide Modulus Control (MSB)	Defaults to logic 0, connect to VCC for logic 1
21 (R5)	Divide Modulus Control	Defaults to logic 0, connect to VCC for logic 1
22 (R4)	Divide Modulus Control	Defaults to logic 0, connect to VCC for logic 1
23 (R3)	Divide Modulus Control	Defaults to logic 0, connect to VCC for logic 1
24 (R2)	Divide Modulus Control	Defaults to logic 0, connect to VCC for logic 1
Paddle	Package Paddle	Tie to heatsink,

UXN40M7KE Evaluation Board Schematic

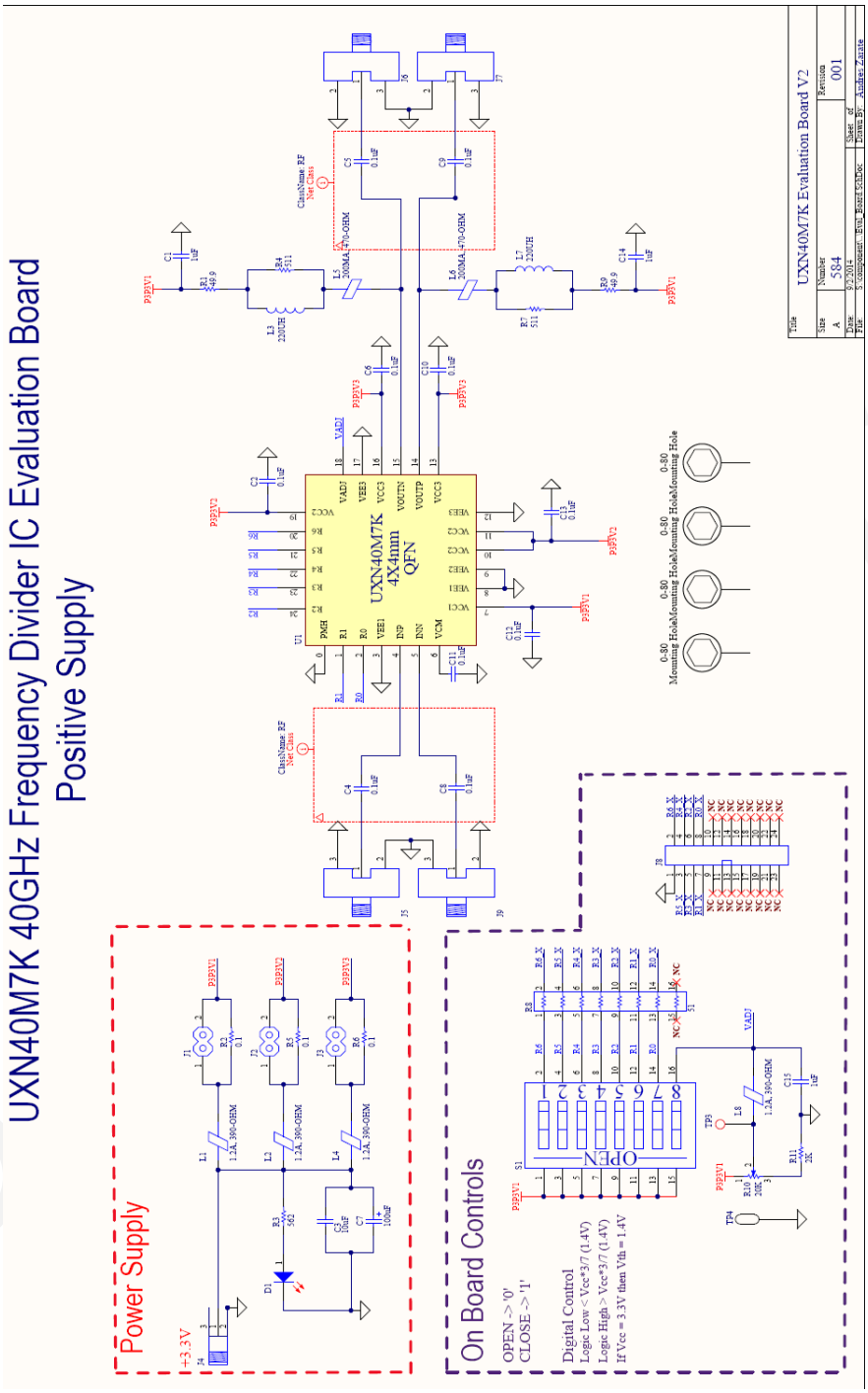


Figure 3: Schematic of the UXN40M7KE evaluation PC board