WST33H0NC

2.4-2.5 GHz, 300 W GaN Transistor

Description

The WST33H0NC is a 300W packaged, partially-matched transistor utilizing the high performance, 50V, 0.25um GaN on SiC production process. The WST33H0NC operates from 2.4-2.5 GHz and targets microwave heating applications. Under class-C operation, the WST33H0NC typically achieves 300 W of saturated output power with 14 dB of large signal gain and 75% drain efficiency via a 2.4-2.5 GHz reference design.

Available in a thermally-enhanced, Cu-based package, the WST33H0NC provides superior performance under CW operation allowing customers to improve SWaP-C benchmarks in their next-generation systems.

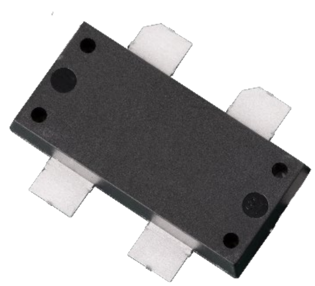


Figure 1. WST33H0NC

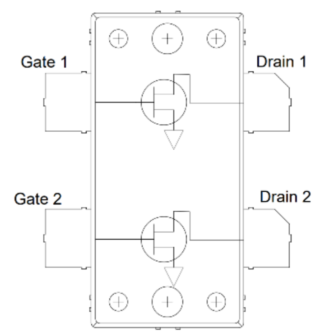


Figure 2. Functional Block Diagram

Features

- Psat: 300 W
- DE: 75 %
- LSG: 17 dB
- S21: 26 dB
- S11: -5 dB
- S22: -6 dB
- CW operation

Note: Features are typical class-C performance via a 2.4-2.5 GHz reference design under 25°C, CW operation (WST33H0NC-AMP1). Please reference performance charts for additional information.

Applications

- Microwave Heating
- Industrial, Scientific and Medical

RoHS compliant

Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain to Source Voltage	V_{DSS}	V	150	
Gate Voltage	V_G	V	-8,+2	
Drain Current	I_D	A	49.0	
Gate Current	I_G	mA	51.2	
Input Power	P_{in}	dBm	42 dBm	
Dissipated Power	P_{diss}	W	250	85°C
Storage Temperature	T_{stg}	°C	-65, +150	
Mounting Temperature	T_J	°C	260	30 seconds
Junction Temperature	T_J	°C	275	MTTF > 1E6
Output Mismatch Stress[1]	VSWR	Ψ	20:1	

1 Pulsed 100 uS, 20 %

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	Vd	V	50	
Gate Voltage	Vg	V	-4.0	
Drain Current	Idq	mA	0	Class C, Vg -4.0
Input Power	Pin	dBm	39	
Case Temperature	Tcase	°C	-40 to 85	

RF Specifications (WST33H0NC-AMP1)

Test conditions unless otherwise noted: Vd=50V, CW, Pin = 39dBm, Vg=-4V, T_{base}=25 °C

Parameter	Units	Min	Typical	Max	Conditions
Frequency	GHz	2.4		2.5	
Output Power	dBm		55		
Drain Efficiency	%		75		
LSG	dB		17		
Small-Signal Gain (S21)	dB		26		Pin = -20 dBm
Input Return Loss (S11)	dB		-5		Pin = -20 dBm
Output Return Loss (S22)	dB		-6		Pin = -20 dBm

Notes:
1. Final testing and screening for all transistor sales is performed using the WST33H0NC-AMP1 at 2.4-2.5 GHz.
2. Test and screening under class-C operation for peak efficiency. User may operate under different operating class depending on specific system requirements.

Test conditions unless otherwise noted: Vd=50V, CW, Pin = 39dBm, Vg=-4V, T_{base}=25 °C

Figure 3: Pout v. Frequency v. Temperature

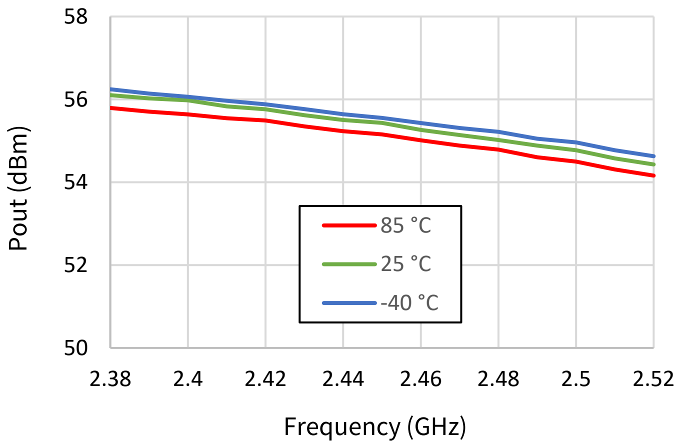


Figure 4: DE v. Frequency v. Temperature

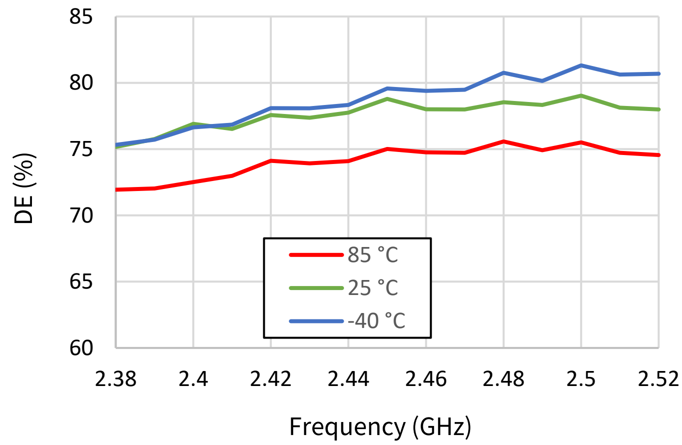


Figure 5: Id v. Frequency v. Temperature

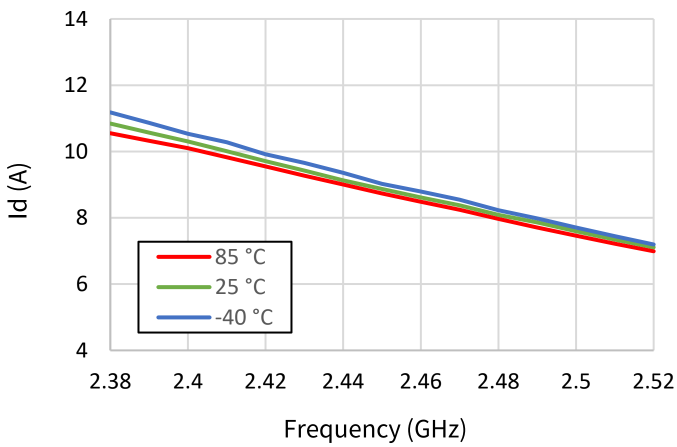


Figure 6: Ig v. Frequency v. Temperature

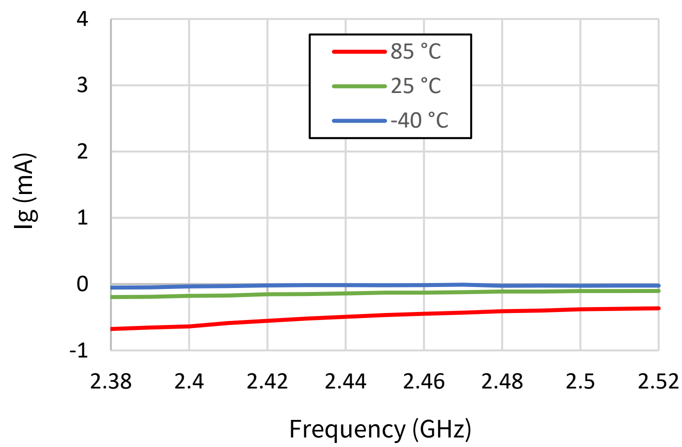
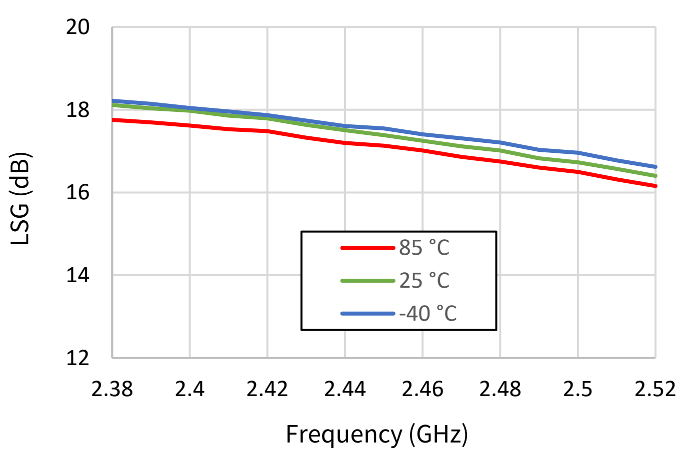


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=50V, CW, Pin = 39dBm, Vg=-4V, T_{base}=25 °C

Figure 8: Pout v. Frequency v. Vd

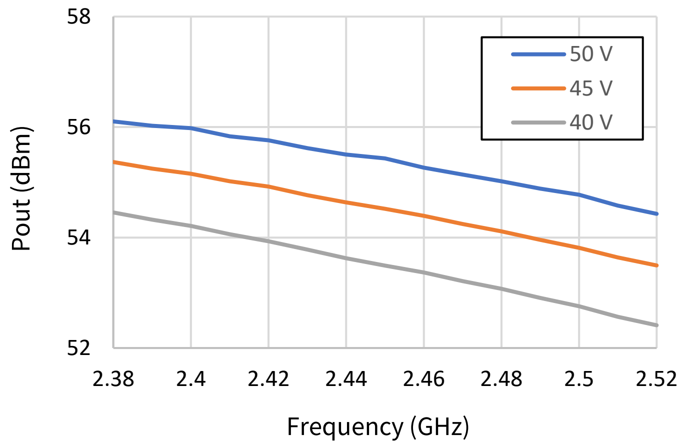


Figure 9: DE v. Frequency v. Vd

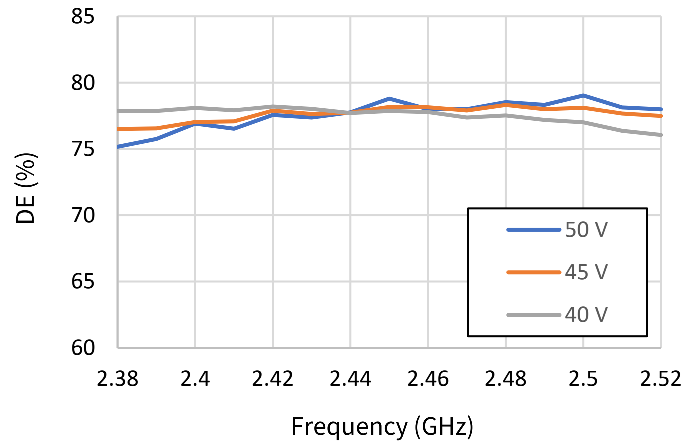


Figure 10: Id v. Frequency v. Vd

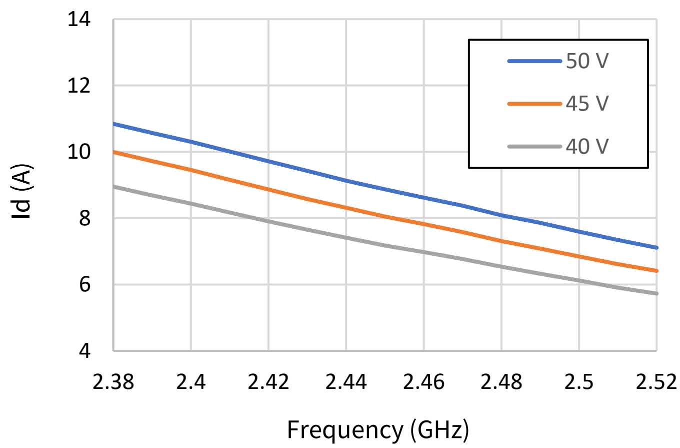


Figure 11: Ig v. Frequency v. Vd

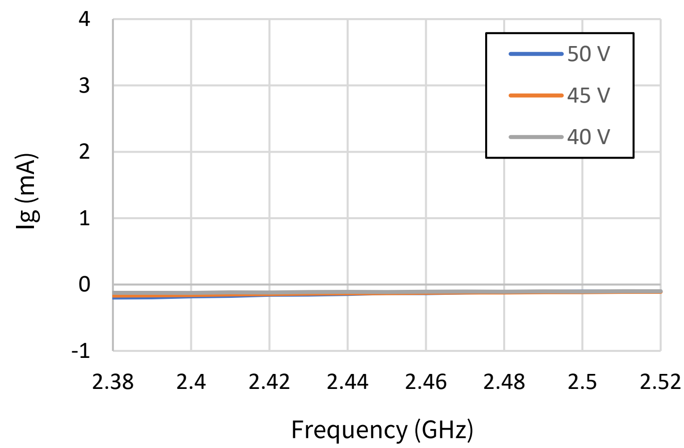
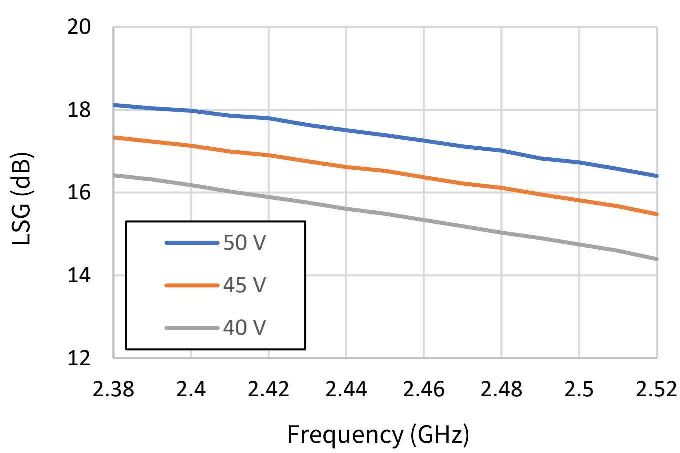


Figure 12: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=50V, CW, Pin = 39dBm, Vg=-4V, T_{base}=25 °C

Figure 13: Pout v. Frequency v. Idq

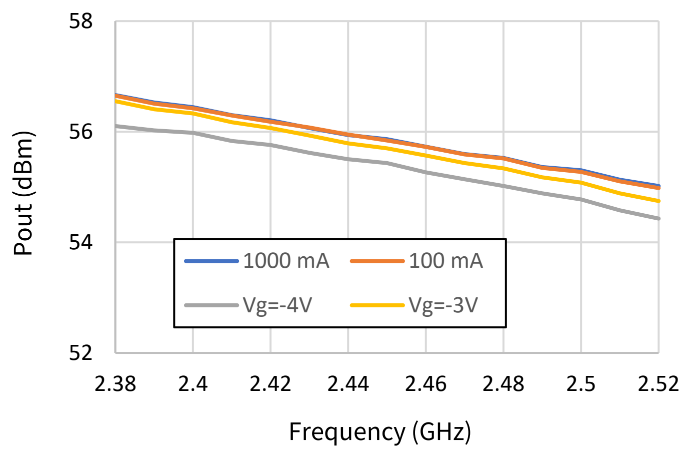


Figure 14: DE v. Frequency v. Idq

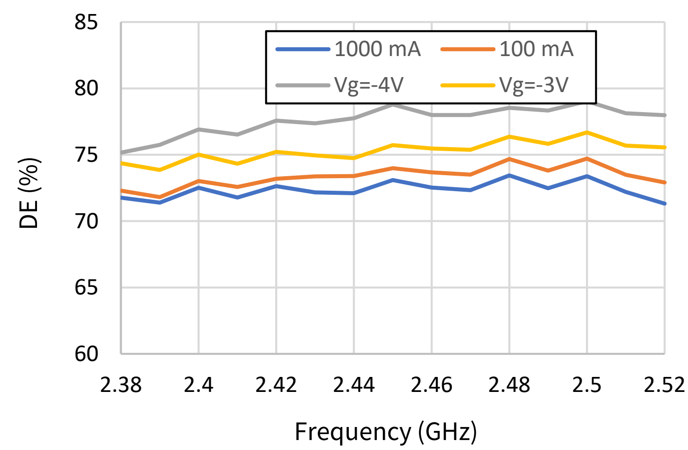


Figure 15: Id v. Frequency v. Idq

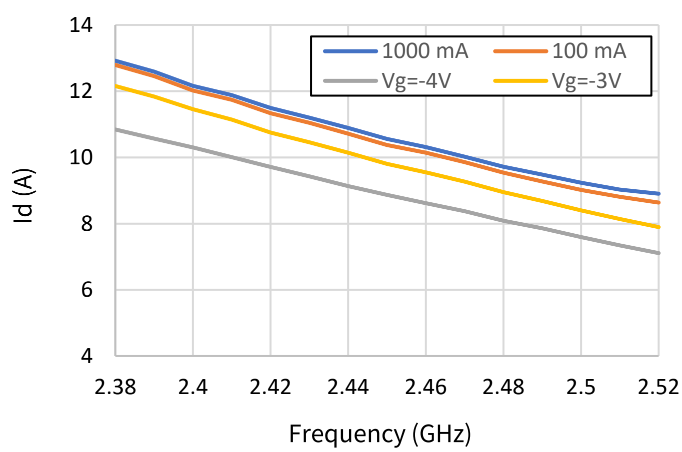


Figure 16: Ig v. Frequency v. Idq

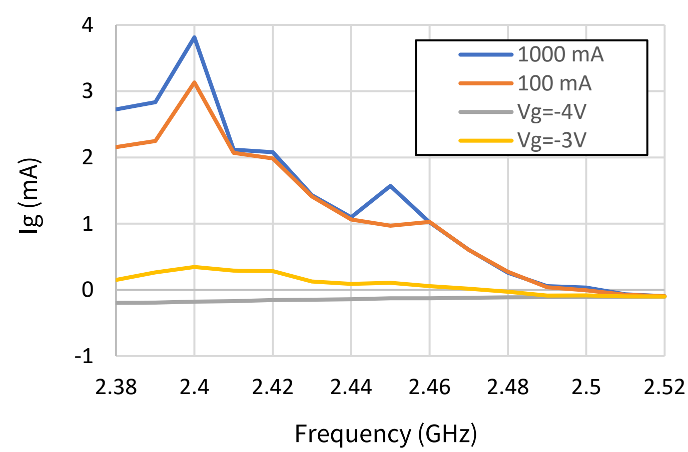
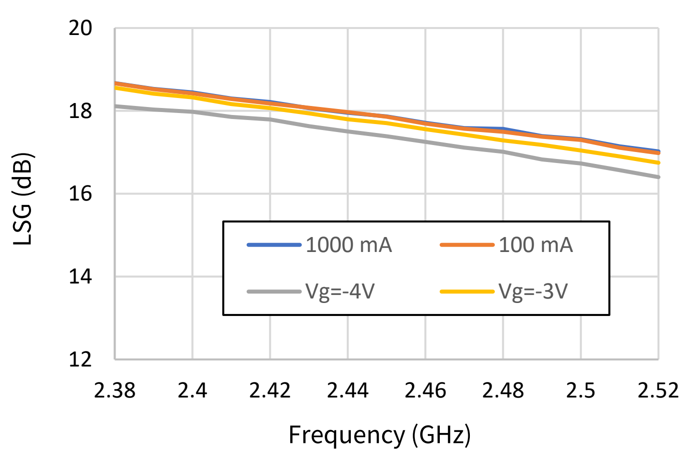


Figure 17: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=50V, CW, Pin = 39dBm, Vg=-4V, T_{base}=25 °C

Figure 18: Pout v. Pin v. Frequency

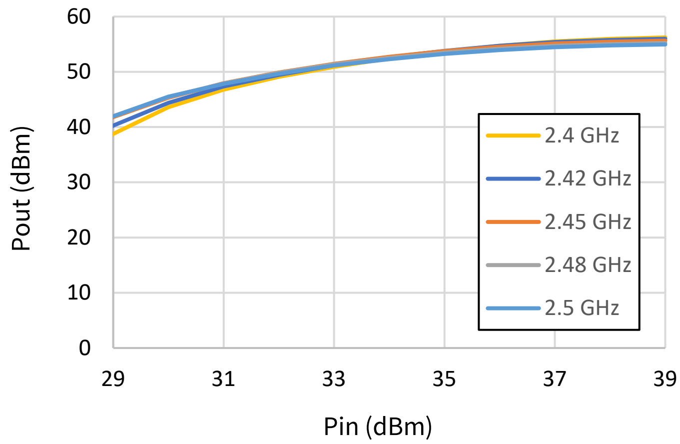


Figure 19: DE v. Pin v. Frequency

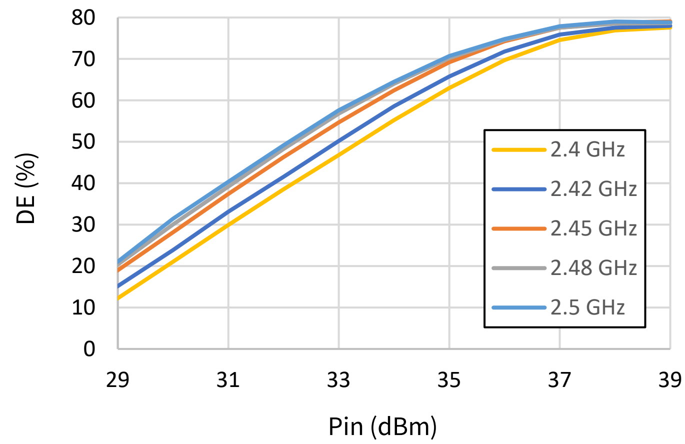


Figure 20: Id v. Pin v. Frequency

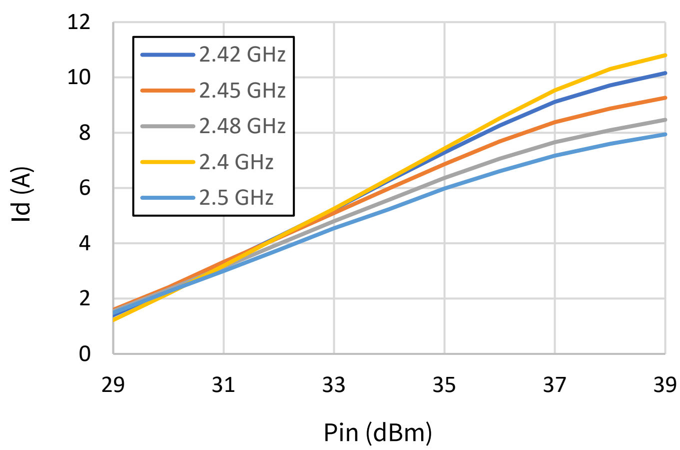


Figure 21: Ig v. Pin v. Frequency

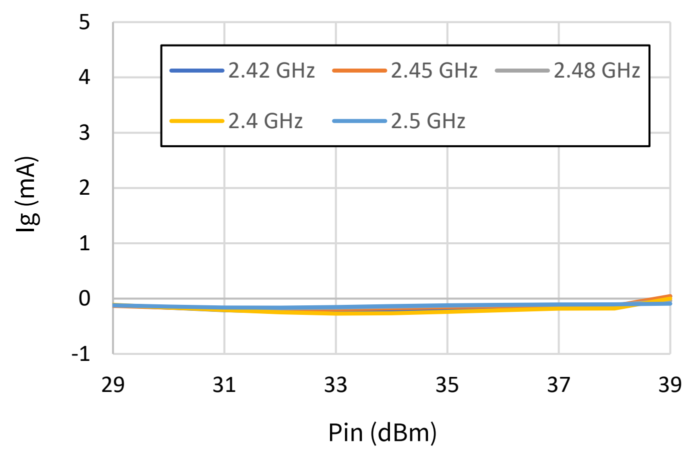
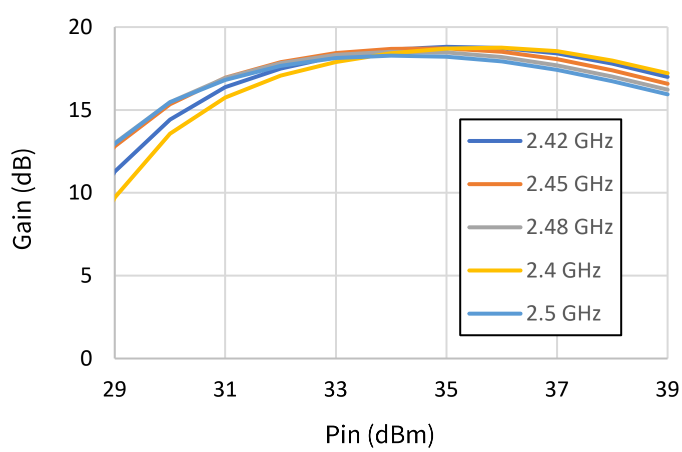


Figure 22: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: Vd=50V, CW, Pin = 39dBm, Vg=-4V, T_{base}=25 °C

Figure 23: Pout v. Pin v. Temperature

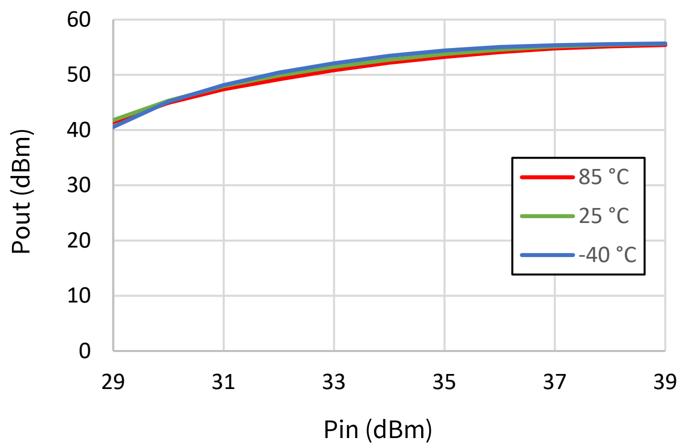


Figure 24: DE v. Pin v. Temperature

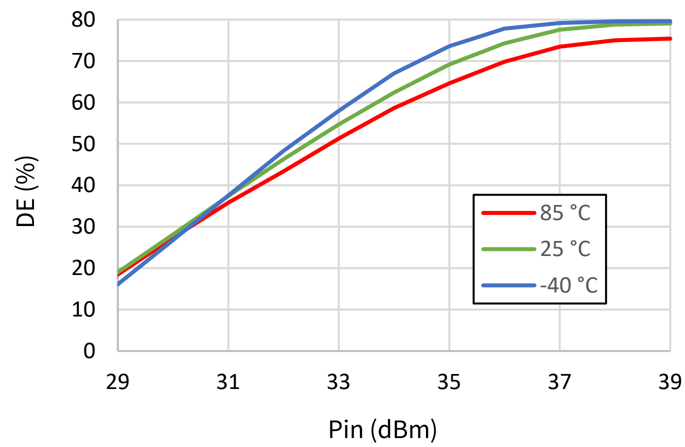


Figure 25: Id v. Pin v. Temperature

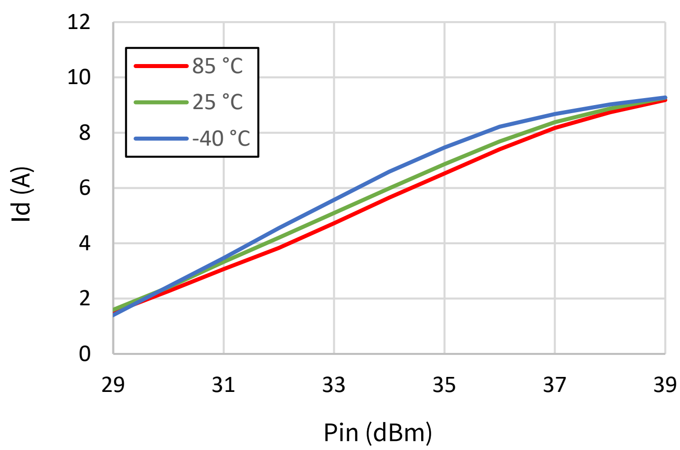


Figure 26: Ig v. Pin v. Temperature

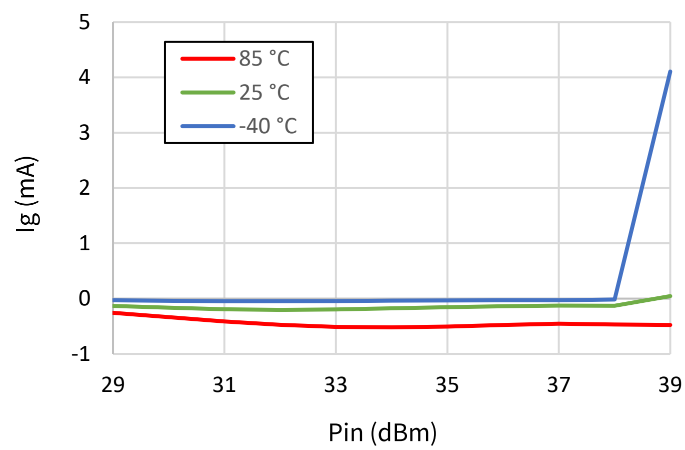
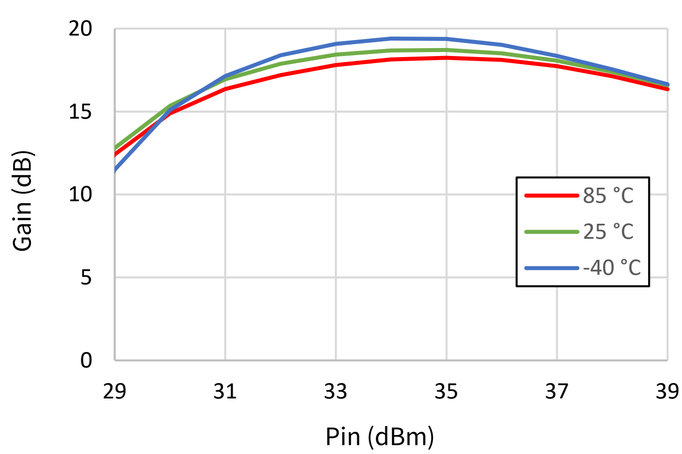


Figure 27: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=50V, CW, Pin = 39dBm, Vg=-4V, T_{base}=25 °C

Figure 28: Pout v. Pin v. Vd

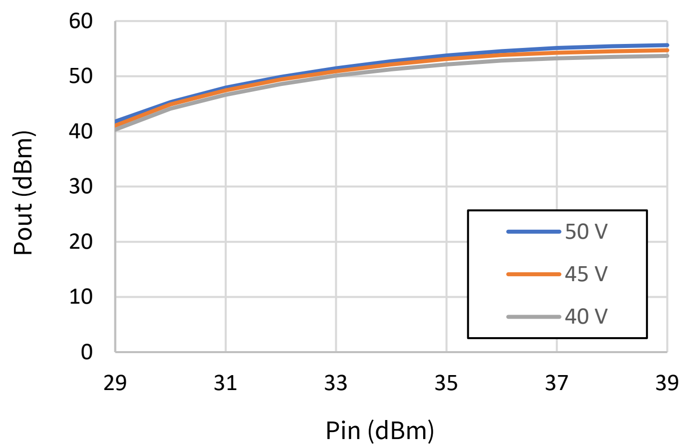


Figure 29: DE v. Pin v. Vd

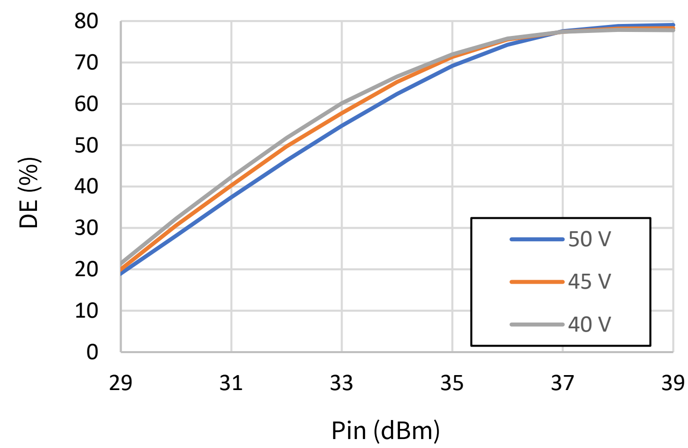


Figure 30: Id v. Pin v. Vd

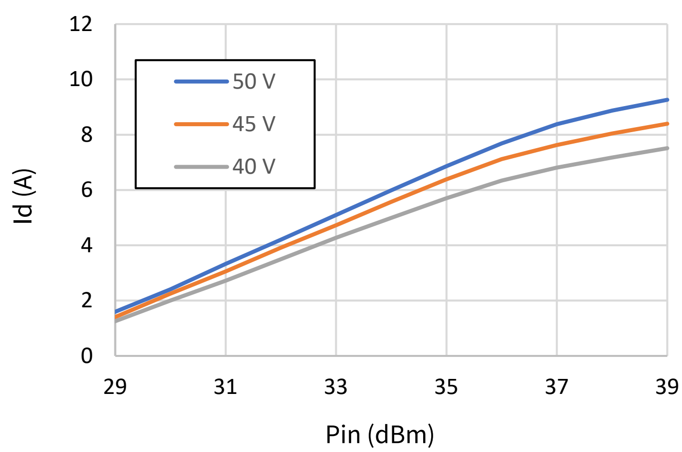


Figure 31: Ig v. Pin v. Vd

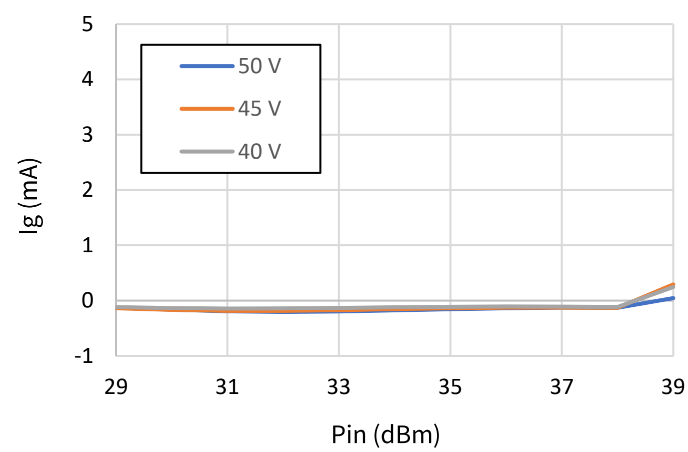
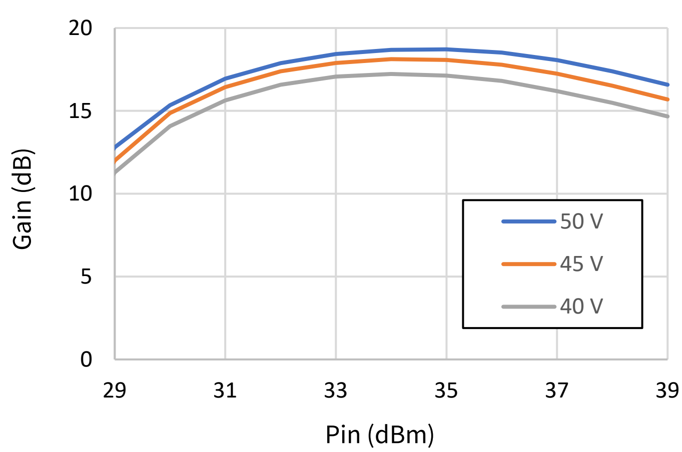


Figure 32: Gain v. Pin v. Vd



Test conditions unless otherwise noted: Vd=50V, CW, Pin = 39dBm, Vg=-4V, T_{base}=25 °C

Figure 33: Pout v. Pin v. Idq

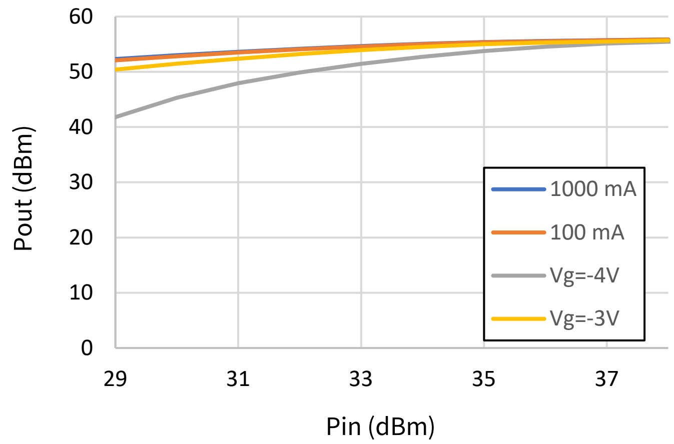


Figure 34: DE v. Pin v. Idq

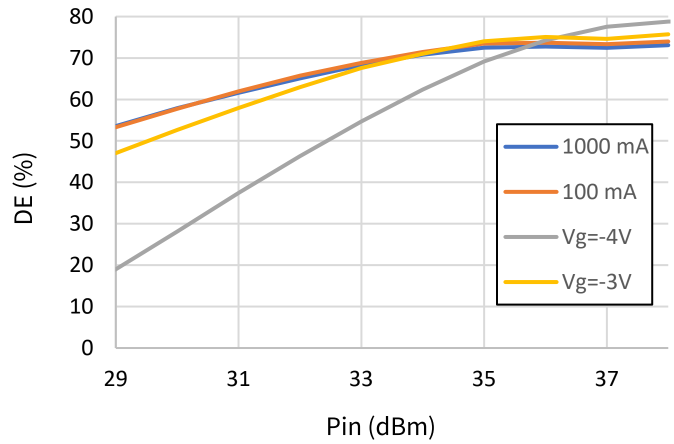


Figure 35: Id v. Pin v. Idq

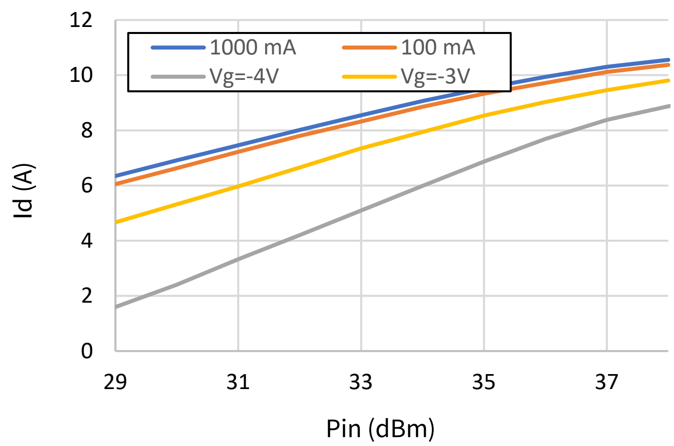


Figure 36: Ig v. Pin v. Idq

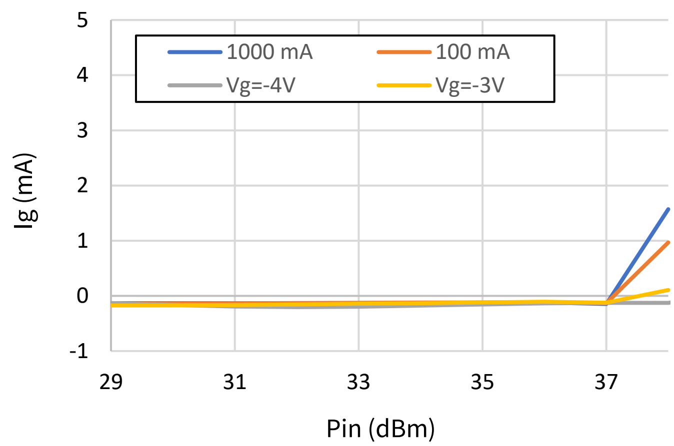
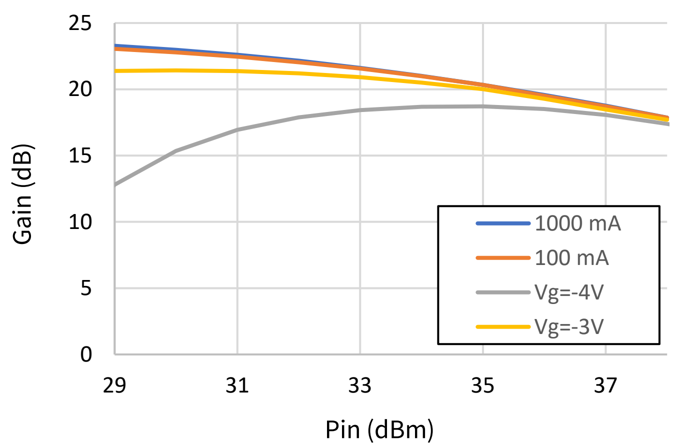


Figure 37: Gain v. Pin v. Idq



Test conditions unless otherwise noted: Vd=50V, CW, Pin = -20dBm, Idq=1000mA, T_{base}=25 °C

Figure 38: S21 v. Frequency v. Temperature

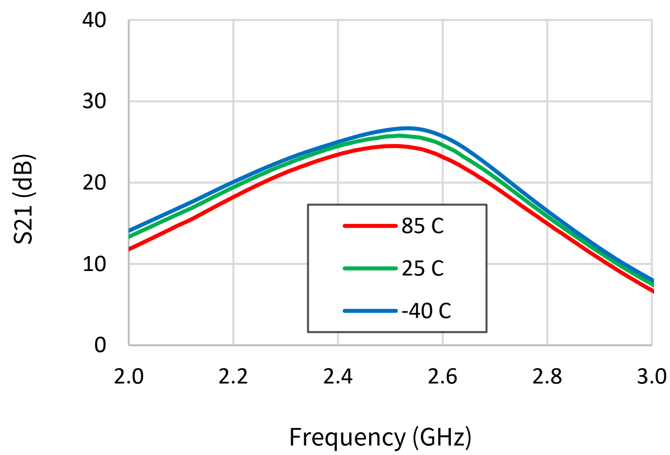


Figure 39: S21 v. Frequency v. Vd

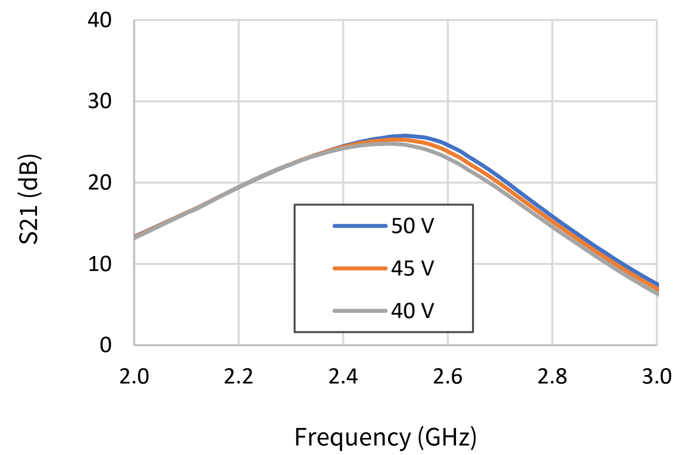


Figure 40: S11 v. Frequency v. Temperature

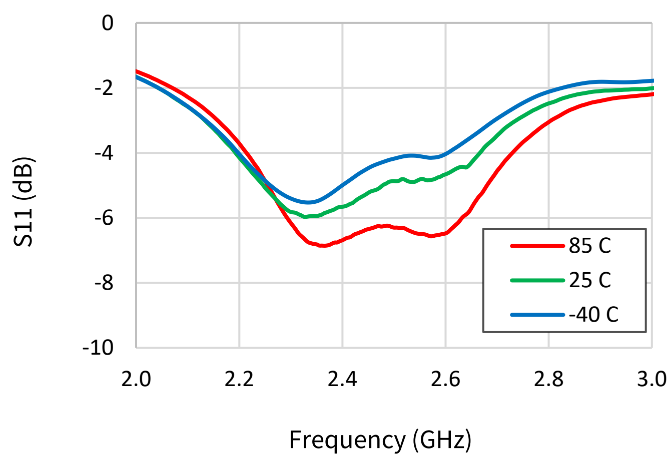


Figure 41: S11 v. Frequency v. Vd

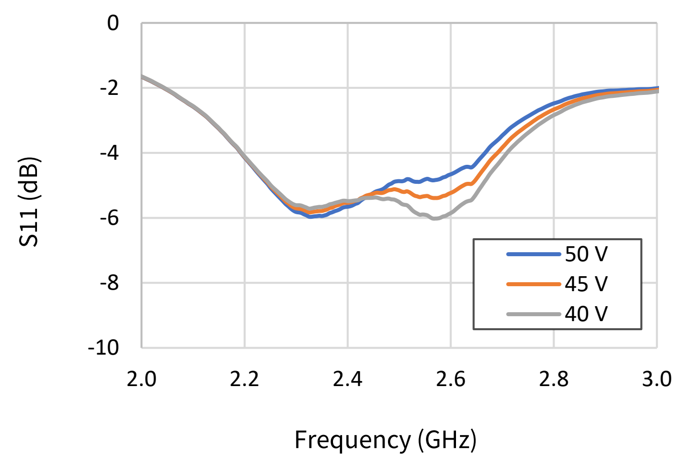


Figure 42: S22 v. Frequency v. Temperature

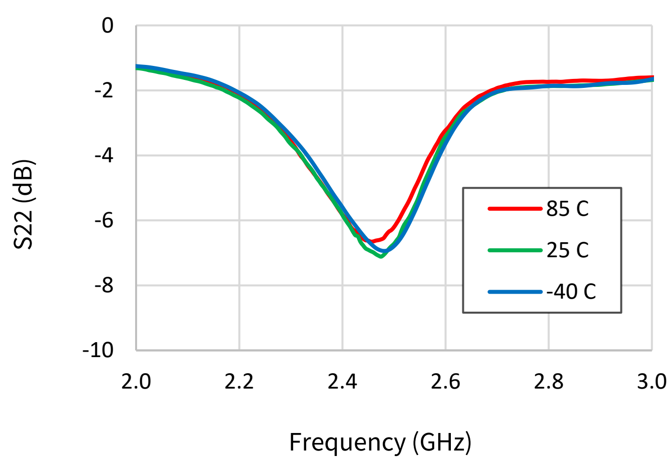
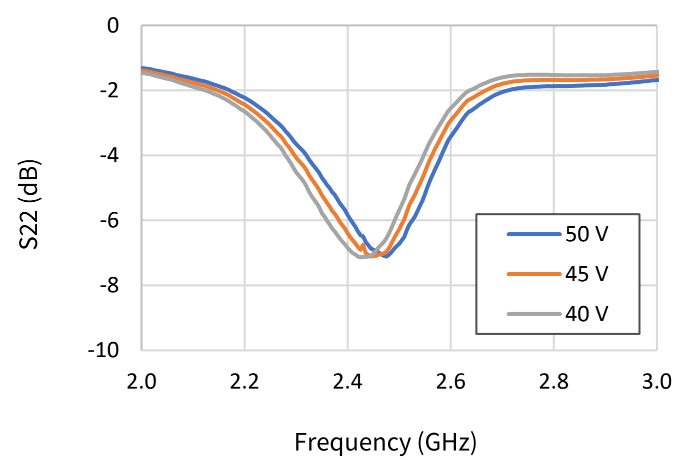


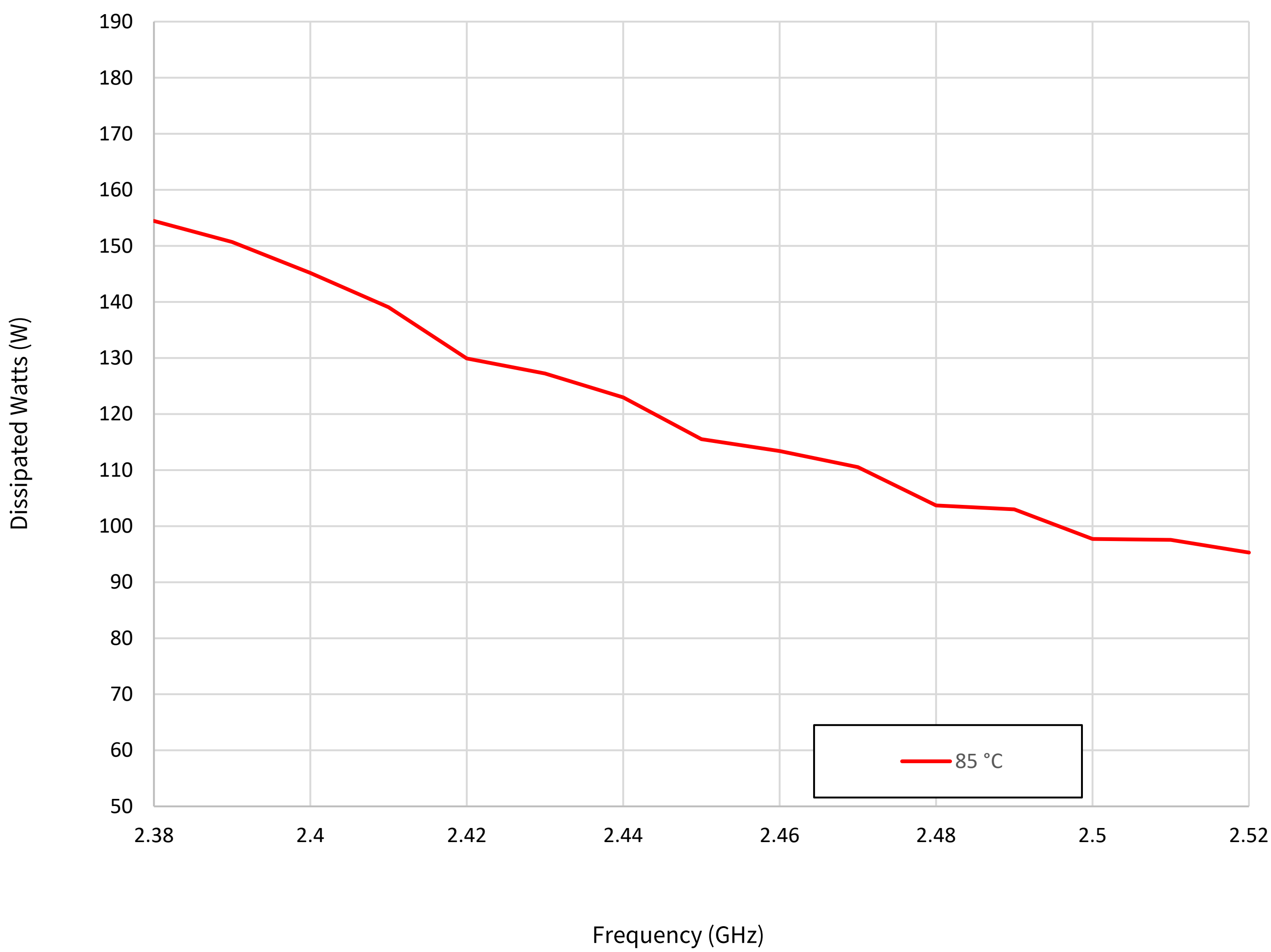
Figure 43: S22 v. Frequency v. Vd



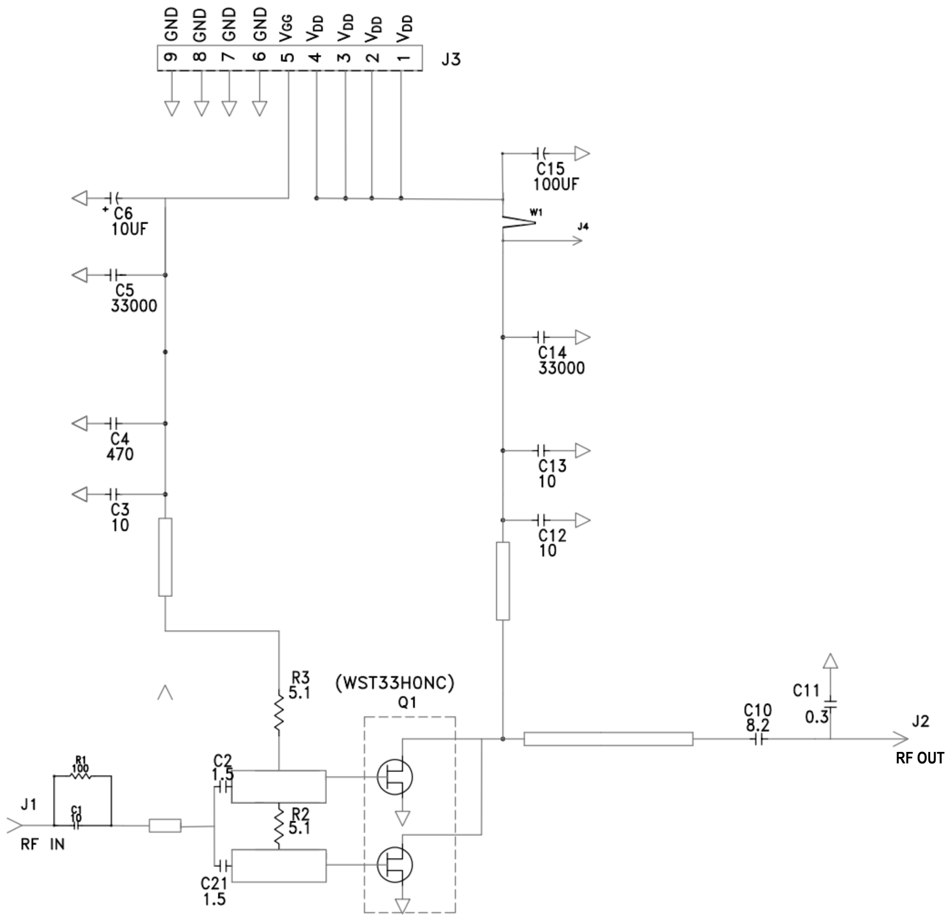
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	179°C	V_d = 50 V, I_{drive} = 10.6 A, P_{in} = 39 dBm, P_{out} = 56.1 dBm, P_{diss} = 145 W, T_{case} = 85°C, CW, Vg=-4V
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65°C/W	

Power Dissipation v. Frequency (Tcase = 85°C)



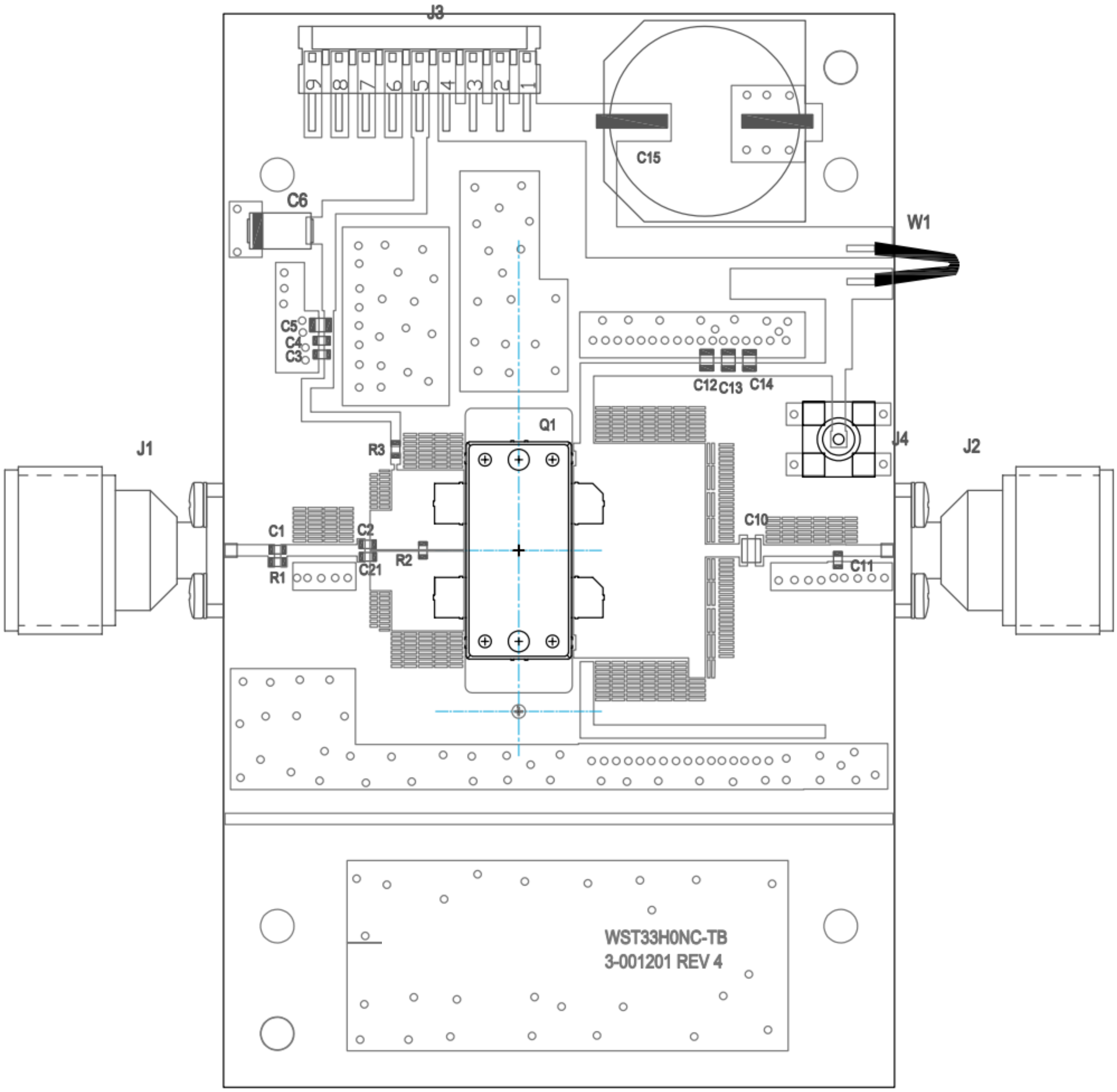
WST33H0NC-AMP1 Evaluation Board Schematic Drawing



WST33H0NC-AMP1 Evaluation Board Bill of Materials

Reference Designator	Description	Qty
C5,C14	CAP, 33000PF, 0805,100V, X7R	2
R1	RES,1/16W,0603,1%,100 OHMS	1
C12,C13	CAP, 10pF, +/- 1%, 250V, 0805, ATC600F	2
C15	CAP, 100 UF, 20%, 160V, ELEC	1
W1	WIRE, 18 AWG ~ 1.75”	1
J1,J2	CONN,N,FEM,W/.500 SMA FLNG	2
J3	HEADER RT>PLZ .1CEN LK 9POS	1
J4	CONN, SMB, STRAIGHT JACK RECEPTACLE	1
C2,C21	CAP, 1.5pF, +/-0.1pF, 0603, ATC600S	2
R3,R2	RES,1/16W,0603,1%,5.1 OHMS	2
C1,C3	CAP, 10.0pF, +/-5%, 0603, ATC600S	2
C4	CAP, 470PF, 5%,100V, 0603	1
C6	CAP 10UF 16V TANTALUM, 2312	1
C10	CAP, 8.2pF, +/-5%,500V, 0709, ATC 800R	1
C11	CAP, 0.3pF, +/-0.05pF, 0603, ATC600S	1
Q1	WST33H0NC, GaN Transistor	1
	PCB, WST33H0NC, RO6035HTC, 20 mil	1
	BASEPLATE, CU, 2.5 X 4.0 X 0.5 IN	1

WST33H0NC-AMP1 Evaluation Board Assembly Drawing



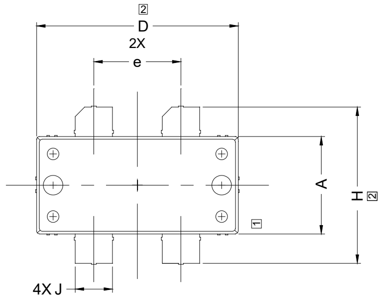
Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (Vg)
3. Apply nominal drain voltage (Vd)
4. Adjust Vg to obtain desired quiescent drain current (Idq)
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (Vg=-5V)
3. Turn off drain voltage (Vd)
4. Turn off gate voltage (Vg)

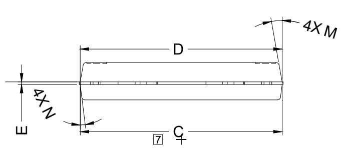
Product Dimensions



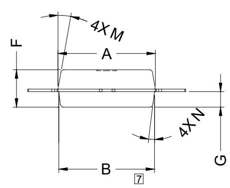
TOP VIEW

Remarks:

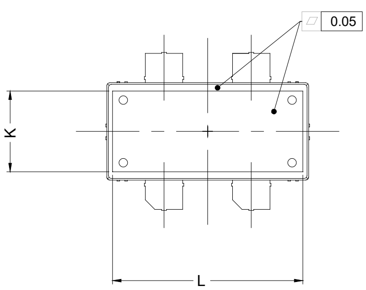
1. Interpret dimensions and tolerances per ASME Y14.5M-1994
2. Mold/Dam Bar/Metal protrusion of 0.30mm max per side not included.
3. Metal protrusions are connected to source and shall not exceed 0.10mm max.
4. Fillets and radii:- Unless otherwise noted all radii are 0.30mm max.
5. Molded package Ra 1.2-1.6um.
6. All metal surfaces are tin plated, except area of cut.
7. Does not include Mold/Dam Bar and Metal protrusion.



FRONT VIEW

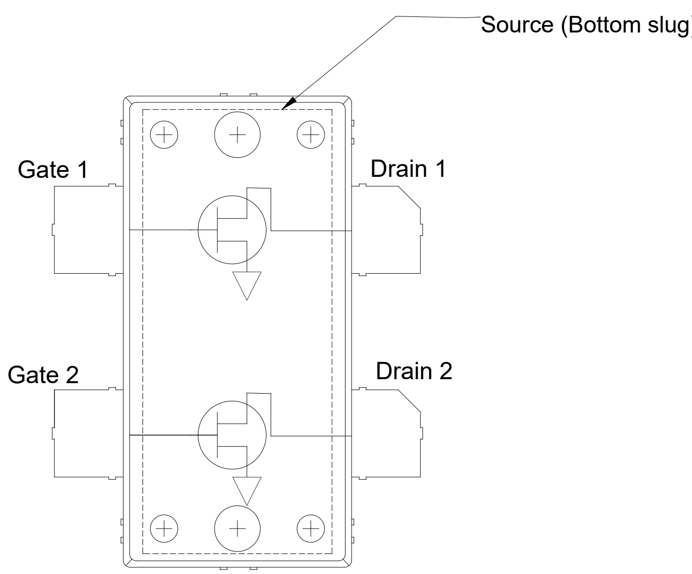


RIGHT SIDE VIEW



BOTTOM VIEW

DIM	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.390	0.392	0.394	9.91	9.96	10.01
B	0.383	0.385	0.387	9.73	9.78	9.83
C	0.808	0.810	0.812	20.52	20.57	20.62
D	0.808	0.810	0.812	20.52	20.57	20.62
E	0.007	0.010	0.013	0.17	0.25	0.33
F	0.148	0.150	0.152	3.76	3.81	3.86
G	0.060	0.062	0.064	1.52	1.57	1.62
H	0.624	0.628	0.632	15.86	15.96	16.06
J	0.148	0.150	0.152	3.76	3.81	3.86
K	-	0.325	-	-	8.25	-
L	-	0.764	-	-	19.40	-
M	-	10 °±1°	-	-	10 °±1°	-
N	-	7 °±1°	-	-	7 °±1°	-
e	-	0.350	-	-	8.89	-



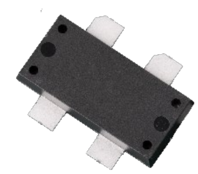
Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Classification Level	Test Methodology
Human Body Model	HBM	TBD	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Moisture Sensitivity Level (MSL)

Rating	Time	Conditions
MSL 3	168 hours	30°C / 60% RH

Product Ordering Information

Part Number	Description	MOQ Increment	Image
WST33H0NC	2.4 – 2.5 GHz, 300W GaN Transistor	250 (T&R)	
WST33H0NC-AMP1	2.4 – 2.5 GHz Evaluation Board	1 Each	

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